AAT2114A

2.5A Low-Noise, Fast Transient 3MHz Step-Down Regulator

General Description

The AAT2114A SwitchReg™ step-down converter delivers up to 2.5A to support the adjustable 1.0V to V_{IN} output from the 2.7V to 5.5V input source. The 3MHz switching frequency allows a high-bandwidth design that minimizes the external LC component requirements.

The AAT2114A high-frequency converter consumes only 70μA no-load quiescent current. The internally compensated, high-frequency, current-mode control scheme provides excellent transient response, minimal output ripple, and reduced spectral noise. Additionally, the AAT2114A provides tight output accuracy across the entire load and input voltage operating ranges.

The regulator maintains high efficiency by integrating the high-side and low-side MOSFETs and designing the gate drivers to minimize dead-time switching losses. The regulator also reduces the switching frequency under light load conditions, minimizing power loss over the entire load range.

For system fault protection, the AAT2114A includes over-temperature and short-circuit current-limit protection to safeguard the AAT2114A and system components from overload conditions.

The compact 3mm x 3mm QFN package footprint, minimal LC requirements, and high efficiency make the AAT2114A an ideal choice for low-power portable applications operating from a Li-ion/polymer battery.

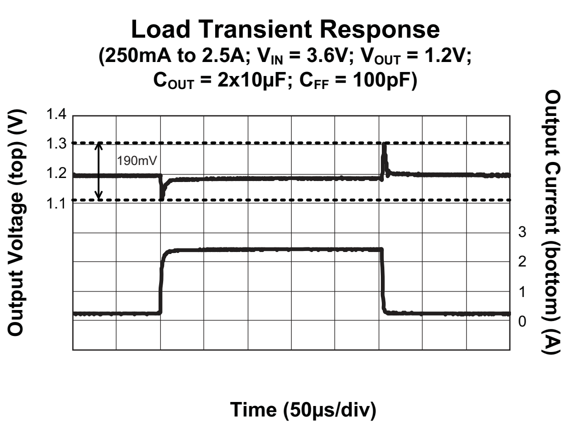
Features

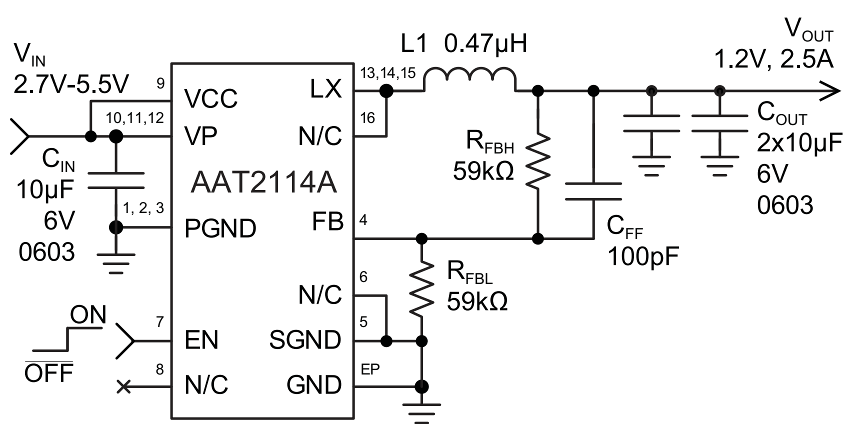
- 2.5A Maximum Output Current
- 3MHz Switching Frequency
  - Stable With 20μF Output Capacitor
- 2.7V to 5.5V Input Voltage Range
- Adjustable 1.0V to V_{IN} Output Voltage
- Up to 95% Efficiency
- Excellent Current-Mode Transient Response
- Low-Noise Light-Load Architecture
- 70μA No Load Quiescent Current
- No External Compensation Required
- Internal Soft Start
- Over-Temperature and Current-Limit Protection
- <1μA Shutdown Current
- -40°C to +85°C Temperature Range
- 16-Pin, 3mm x 3mm QFN Package

Applications

- Cellular Phones
- Digital Cameras
- MP3/Portable Media Players
- Wireless Cards

Typical Application



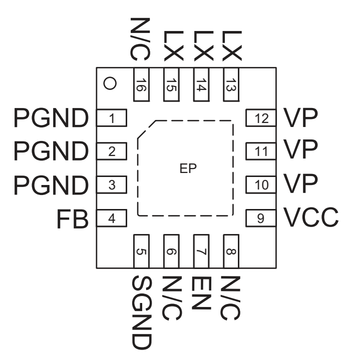


Pin Descriptions

Pin #	Name	Function
1, 2, 3	PGND	Power Ground. PGND is internally connected to the source of the low-side N-channel MOSFET. Connect to the input capacitor and output capacitor return.
4	FB	Feedback Input. FB senses the output voltage for regulation control. Connect a resistive divider network from the output to FB to SGND to set the output voltage accordingly. The adjustable FB regulation threshold is 0.6V.
5	SGND	Signal/Analog Ground. SGND is internally connected to the analog ground of the control circuitry. Connect the return of the feedback components to this ground.
6, 8, 16	N/C	Not Internally Connected. This pin is not internally connected and may be either left open or shorted to an adjacent pin.
7	EN	Enable Input. A logic high enables the AAT2114A regulator. A logic low forces the AAT2114A into shutdown mode, placing the output into a high-impedance state and reducing the quiescent current to less than 1μA. Do NOT leave EN floating.
9	VCC	Bias Input Supply. VCC supplies power to the analog and logic signal control circuitry of the AAT2114A.
10, 11, 12	VP	Input Power Supply. Connect VP to the input power source. Bypass VP to PGND with a 10μF or greater ceramic capacitor. VP internally connects to the source of the high-side P-channel MOSFET and MOSFET drivers as shown in the Functional Block Diagram.
13, 14, 15	LX	Inductor Switching Node. LX is internally connected to the source of the high-side P-Channel MOSFET and the drain of the low-side N-channel MOSFET. Externally connected to the power inductor as shown in the Typical Application Circuit.
EP	GND	Thermal/Substrate Ground. GND is internally connected to the substrate of the controller and serves as the lowest thermal impedance path. Connect directly to the system ground plane to keep the thermal impedance low.

Pin Configuration

QFN33-16
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_P	VP to PGND	-0.3 to +6	V
V_{CC}	VCC to SGND	-0.3 to +6	V
V_{LX}	LX to PGND	-0.3 to (V_P + 0.3)	V
V_{EN}	EN to SGND	-0.3 to (V_{CC} + 0.3)	V
V_{FB}	FB to SGND	-0.3 to (V_{CC} + 0.3)	V
V_{GND}	SGND to GND, PGND to GND	-0.3 to +0.3	V
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec.)	300	°C
T_A	Ambient Temperature Range	-40 to +85	°C

Thermal Characteristics

Symbol	Description	Value	Units
QFN33-16 Thermal Impedance[2]			
θ_{JA}	Maximum Junction-to-Ambient Thermal Resistance	43	°C/W
P_D	Maximum Power Dissipation[3]	2.3	W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on a FR4 demo board in still air. The exposed pad must be mounted to the PCB.
3. Derate 23mW/°C above 25°C.

Electrical Characteristics[1]

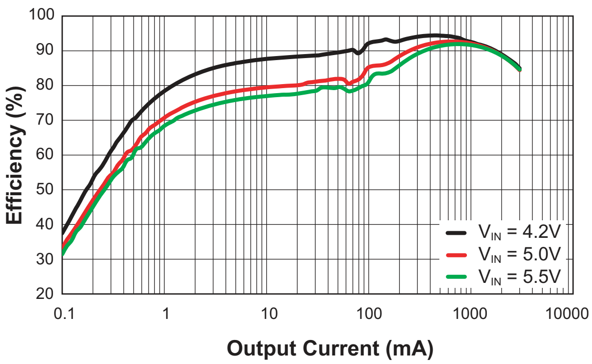
Typical Application Circuit: C_{IN} = 10μF, C_{OUT} = 2x 10μF, L = 0.47μH. V_P = 3.6V, VCC = EN = VP, SGND = PGND = GND. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range	VP, VCC	2.7		5.5	V
V_{OUT}	Output Voltage Range		1.0		V_{IN}	V
V_{UVLO}	Input Under-Voltage Lockout	V_{CC} Rising			2.7	V
		Hysteresis		0.1		V
I_Q	No Load Supply Current	No Load Current; Not Switching		70	140	μA
I_{SHDN}	Shutdown Current	EN = GND, V_P = 5.5V, LX = GND			1	μA
V_{FB}	FB Regulation Threshold	No Load, T_A = +25°C, V_{IN} = 5V	591	600	609	mV
I_{FB}	FB Leakage Current	V_{FB} = 1.0V		5	200	nA
$\Delta V_{OUT}/I_{OUT}$	Load Regulation[2]	0.25 to 2.5A Load		1	2	%
$\Delta V_{OUT}/V_{IN}$	Line Regulation	V_{IN} = 2.7V to 5.5V		0.5		%/V
I_{LIMPK}	High-Side P-Channel MOSFET Current Limit		3			A
$R_{DS(ON)HI}$	High-Side P-Channel MOSFET On-Resistance			120		mΩ
$R_{DS(ON)LO}$	Low-Side N-Channel MOSFET On-Resistance			100		mΩ
f_{OSC}	Internal Oscillator Frequency	V_{IN} = 3.3V	2.2	3.0	3.8	MHz
t_{SS}	Soft-Start Period			60		μs
T_{SHDN}	Over-Temperature Shutdown Threshold	Hysteresis = 15°C		140		°C
V_{EN}	EN Input Logic Threshold		0.4		1.4	V
I_{EN}	EN Input Current	V_{IN} = V_{EN} = 0V or 5.5V	-1.0		+1.0	μA

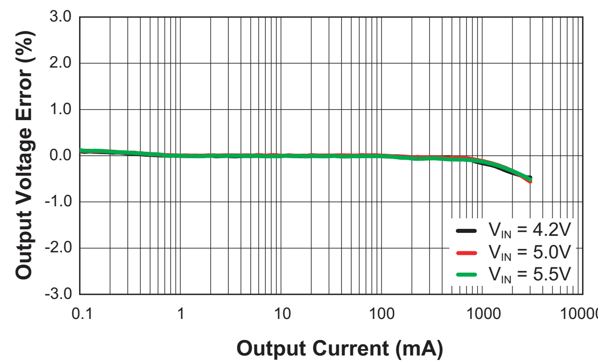
1. The AAT2114A is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.
2. Guaranteed by design.

Typical Characteristics

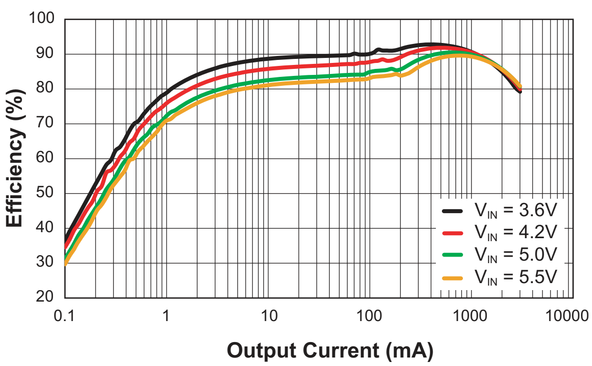
Efficiency vs. Load
(V_{OUT} = 3.3V; L = 1.5µH)



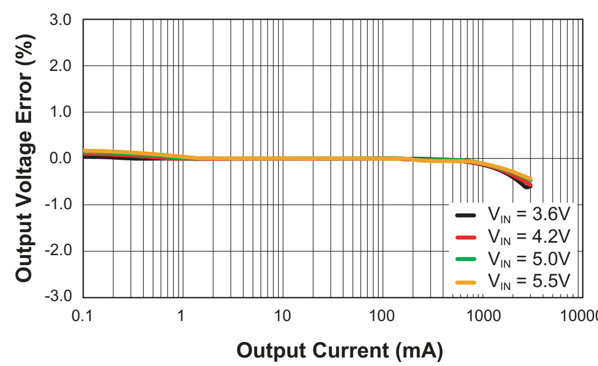
Load Regulation
(V_{OUT} = 3.3V; L = 1.5µH)



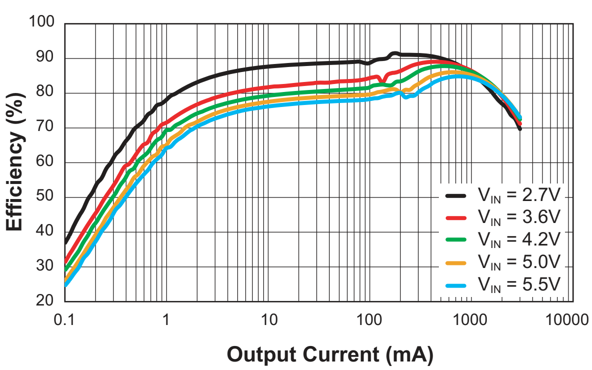
Efficiency vs. Load
(V_{OUT} = 2.5V; L = 1µH)



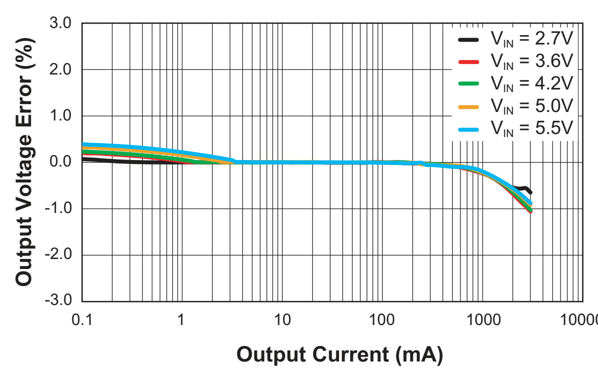
Load Regulation
(V_{OUT} = 2.5V; L = 1µH)



Efficiency vs. Load
(V_{OUT} = 1.8V; L = 0.86µH)

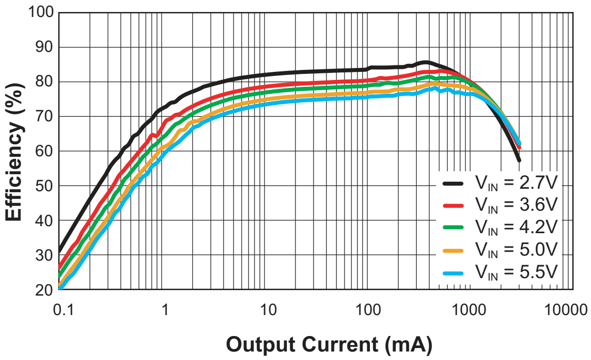


Load Regulation
(V_{OUT} = 1.8V; L = 0.86µH)

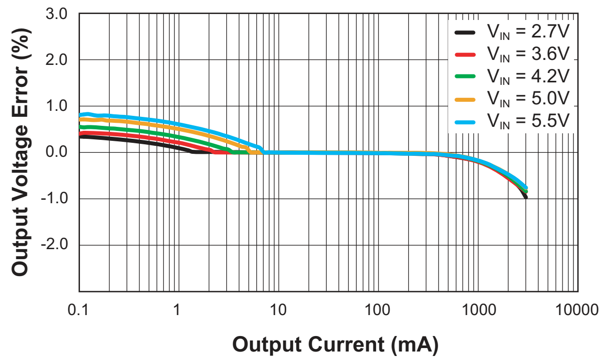


Typical Characteristics

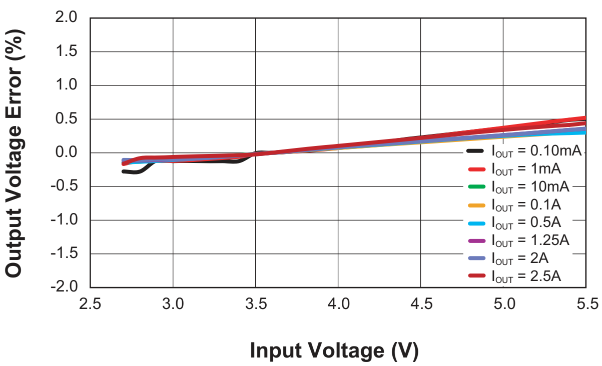
Efficiency vs. Load
(V_{OUT} = 1.2V; L = 0.47µH)



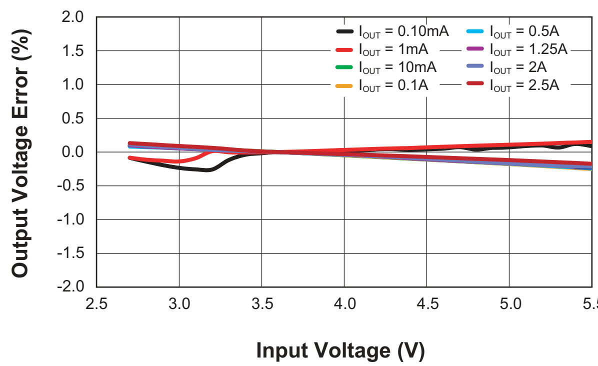
Load Regulation
(V_{OUT} = 1.2V; L = 0.47µH)



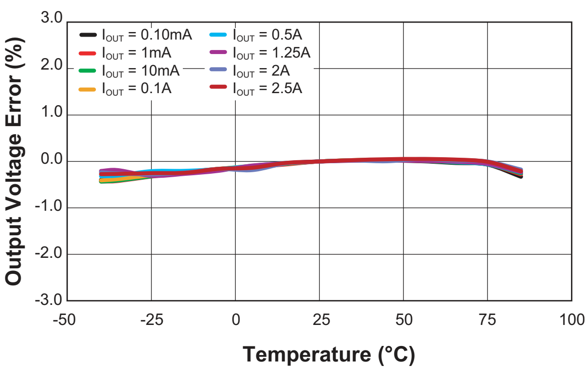
Line Regulation
(V_{OUT} = 1.8V; L = 0.86µH)



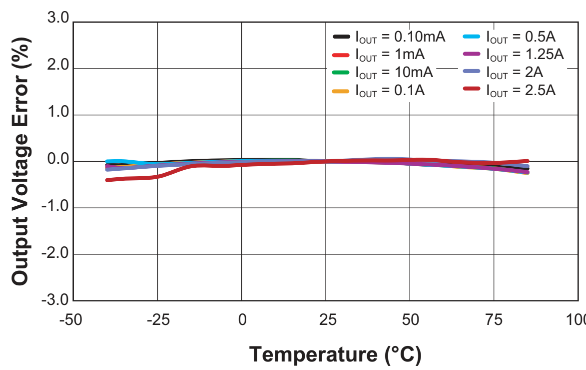
Line Regulation
(V_{OUT} = 1.2V; L = 0.47µH)



Output Voltage Error vs. Temperature
(V_{IN} = 4.2V; V_{OUT} = 3.3V)



Output Voltage Error vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 2.5V)



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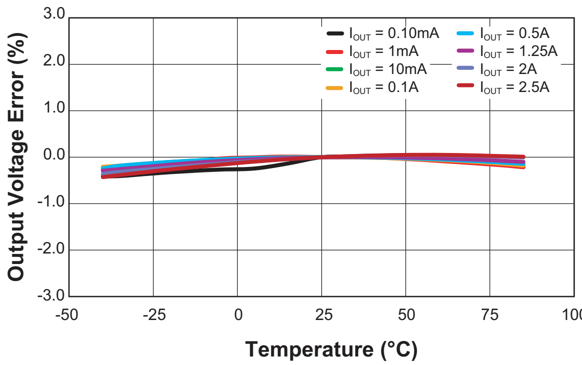
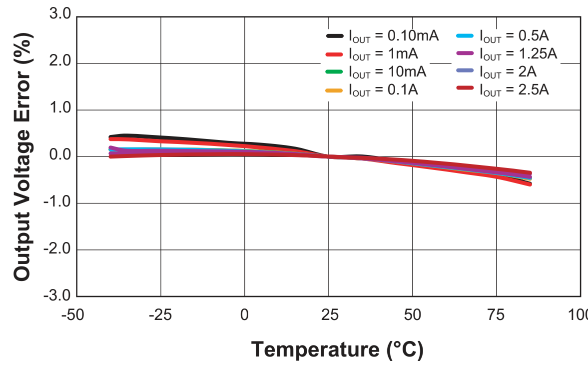
Typical Characteristics

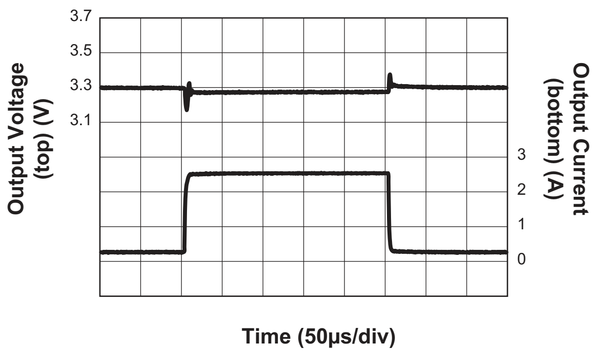
Output Voltage Error vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.8V)



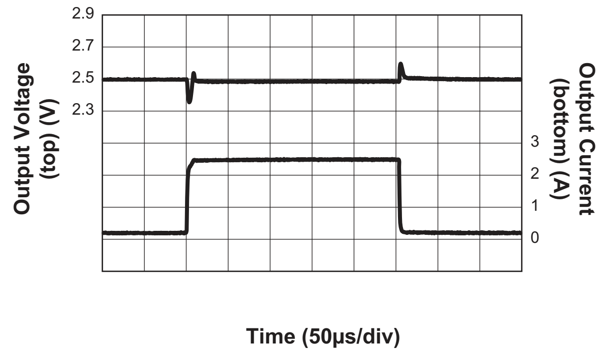
Output Voltage Error vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.2V)



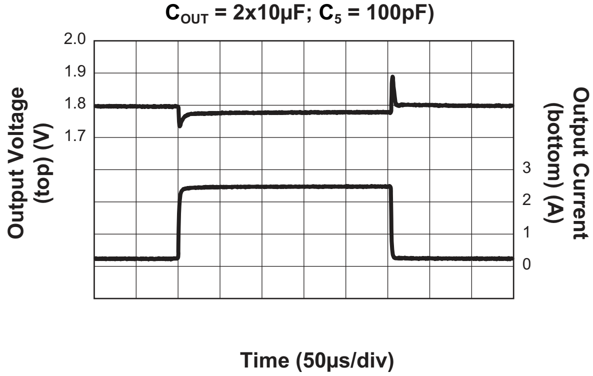
Load Transient Response
(250mA to 2.5A; V_{IN} = 5.0V; V_{OUT} = 3.3V;
C_{OUT} = 2x10µF; C_5 = 100pF)



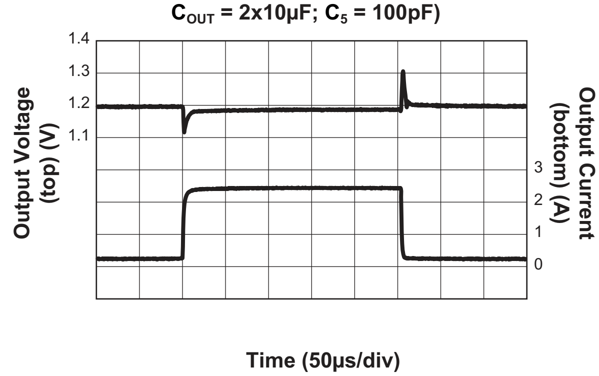
Load Transient Response
(250mA to 2.5A; V_{IN} = 3.6V; V_{OUT} = 2.5V;
C_{OUT} = 2x10µF; C_5 = 100pF)



Load Transient Response
(250mA to 2.5A; V_{IN} = 3.6V; V_{OUT} = 1.8V;
C_{OUT} = 2x10µF; C_5 = 100pF)

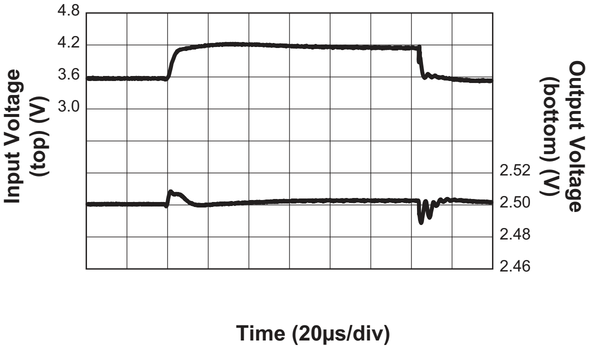


Load Transient Response
(250mA to 2.5A; V_{IN} = 3.6V; V_{OUT} = 1.2V;
C_{OUT} = 2x10µF; C_5 = 100pF)

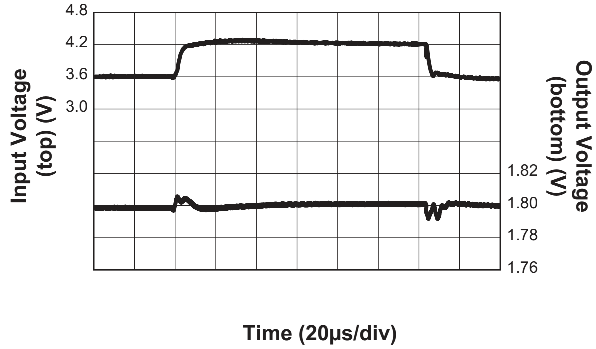


Typical Characteristics

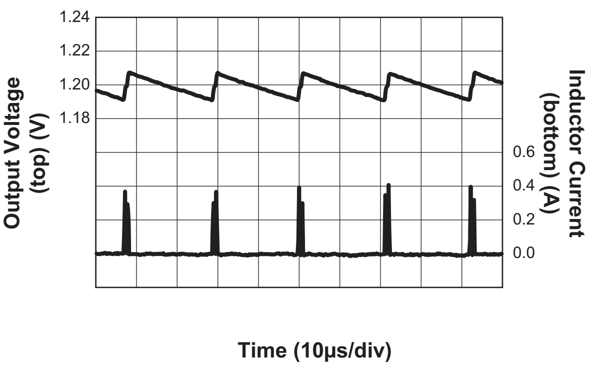
Line Transient Response
(V_{IN} = 3.6V to 4.2V; V_{OUT} = 2.5V; I_{OUT} = 2.5A; C_{OUT} = 2x10µF; C_5 = 100pF)



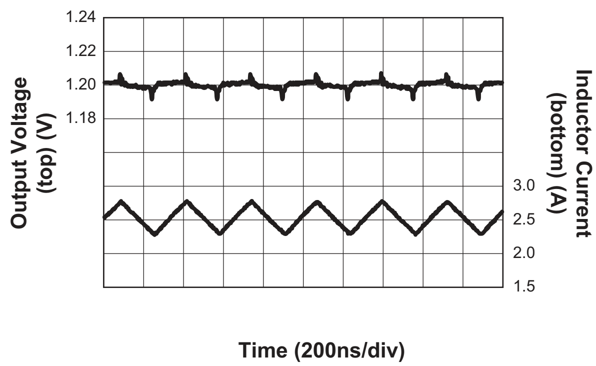
Line Transient Response
(V_{IN} = 3.6V to 4.2V; V_{OUT} = 1.8V; I_{OUT} = 2.5A; C_{OUT} = 2x10µF; C_5 = 100pF)



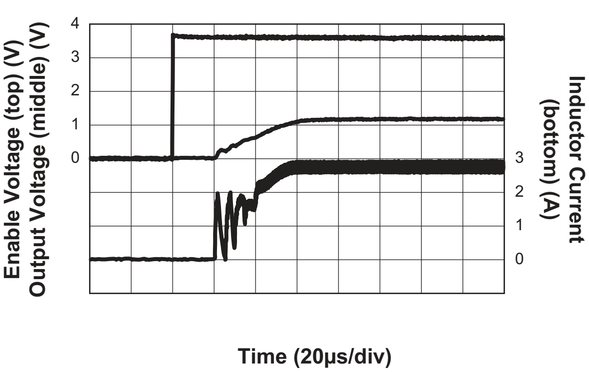
Output Ripple
(V_{IN} = 3.6V; V_{OUT} = 1.2V; I_{OUT} = 10mA)



Output Ripple
(V_{IN} = 3.6V; V_{OUT} = 1.2V; I_{OUT} = 2.5A)

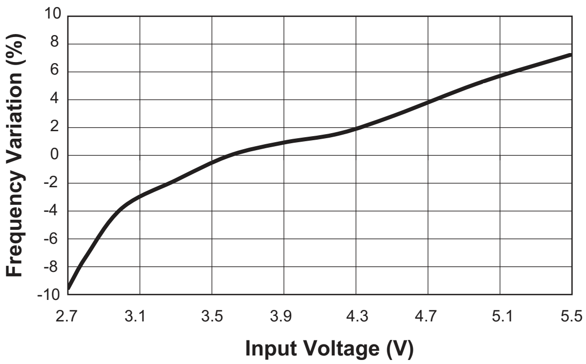


Enable Soft Start
(V_{IN} = 3.6V; V_{OUT} = 1.2V; I_{OUT} = 2.5A)

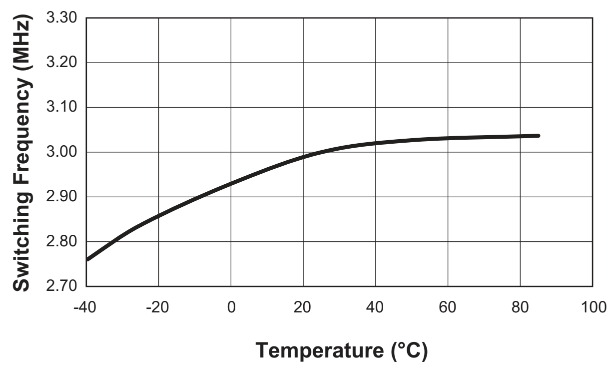


Typical Characteristics

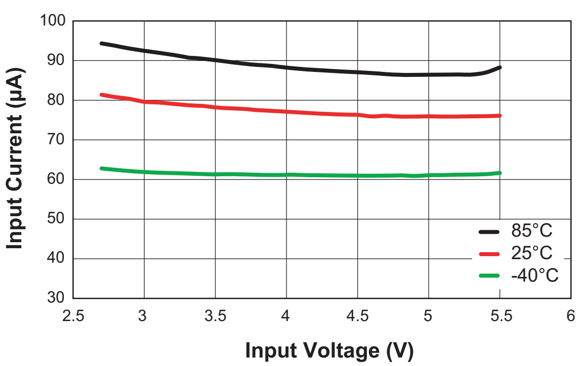
Switching Frequency vs. Input Voltage
(V_{OUT} = 1.2V; I_{OUT} = 2.5A)



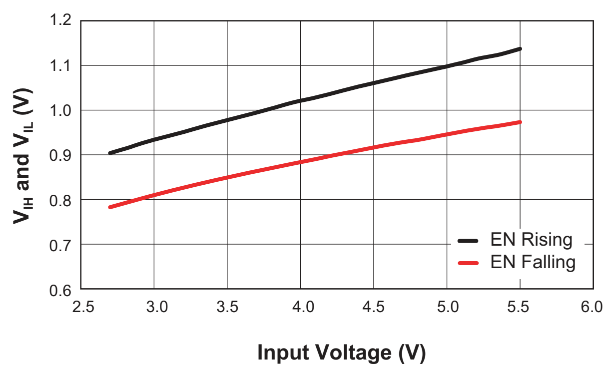
Switching Frequency vs. Temperature
(V_{IN} = 3.6V; I_{OUT} = 2.5A; V_{OUT} = 1.2A)



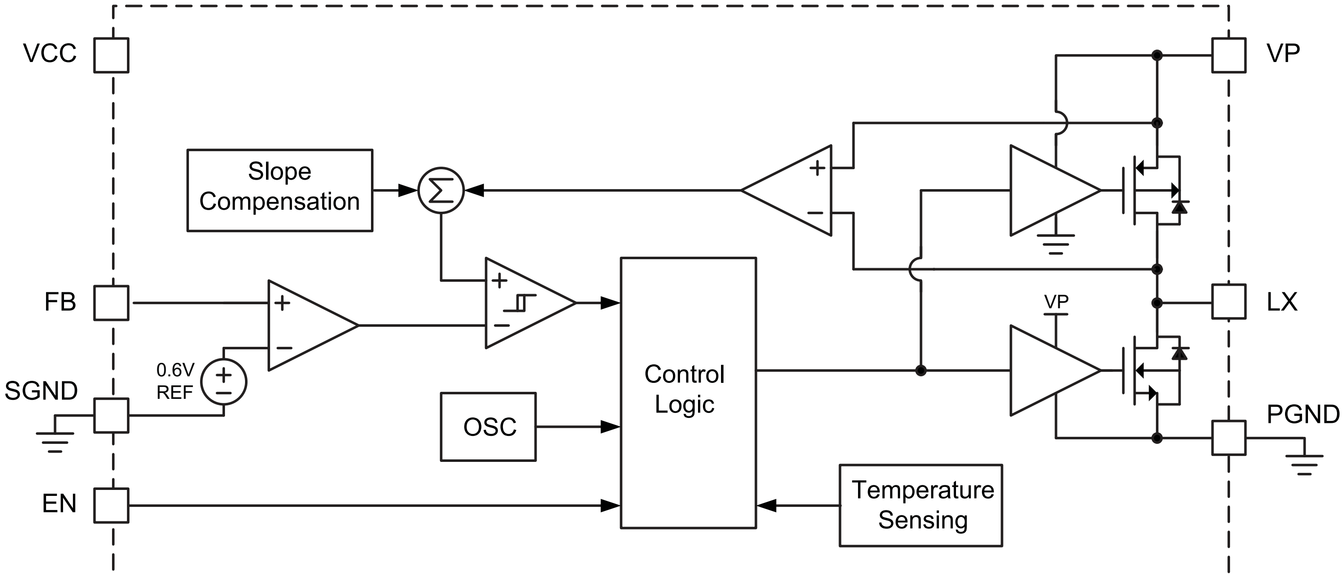
Input Current vs. Input Voltage
(V_{EN} = V_{IN}; V_{OUT} = 1.2V; Closed Loop Switching)



Enable Threshold vs. Input Voltage



Functional Block Diagram



Functional Description

The AAT2114A is a high performance 2.5A monolithic step-down converter operating at a 3MHz switching frequency. It minimizes external component size, optimizes efficiency over the complete load range, and produces reduced ripple and spectral noise. Apart from the small bypass input capacitor, only a small L-C filter is required at the output. Typically, a 0.47µH inductor and a 22µF ceramic capacitor are recommended for a 1.2V output (see table of recommended values).

Light load operation maintains high efficiency, low ripple and low spectral noise even at lower currents (typically <150mA).

The current limit of 4A (typical) protects the IC and system components from short-circuit damage. Typical no load quiescent current is 70µA.

Thermal protection completely disables switching when the maximum junction temperature is detected. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault condition is removed, the output voltage automatically recovers.

Peak current mode control and optimized internal compensation provide high loop bandwidth and excellent response to input voltage and fast load transient events. Soft start eliminates output voltage overshoot when the enable or the input voltage is applied. Under-voltage lockout prevents spurious start-up events.

Control Loop

The AAT2114A is a peak current mode step-down converter. The current through the P-channel MOSFET (high side) is sensed for current loop control, as well as short circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak current mode loop appears as a voltage-programmed current source in parallel with the output capacitor.

The output of the voltage error amplifier programs the current mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. Internal loop compensation determines the transconductance voltage error amplifier output. The 0.6V reference voltage is internally set to program the converter output voltage greater than or equal to 1.0V.

Soft Start/Enable

Soft start limits the current surge seen at the input and eliminates output voltage overshoot. When pulled low, the enable input forces the AAT2114A into a low-power, non-switching state. The total input current during shutdown is less than 1µA.

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Current Limit and Over-Temperature Protection

For overload conditions, the peak input current is limited. The on-time is terminated after a current limit has been sensed.

Thermal protection completely disables switching when internal dissipation becomes excessive. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault conditions is removed, the output voltage automatically recovers.

Under-Voltage Lockout

Internal bias of all circuits is controlled via the VCC input. Under-voltage lockout (UVLO) guarantees sufficient V_{IN} bias and proper operation of all internal circuitry prior to activation.

Component Selection

Inductor Selection

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. The inductor value can be calculated by:

$$L1 = \frac{0.47 \cdot V_{OUT}}{1.2}$$

For low cost application and a sufficiently small footprint, the TDK VLS252012T-R47N2R1 shielded chip inductor, which has 47mΩ DCR, is selected for 1.2V output (see Table 1).

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions.

Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR.

Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

Input Capacitor

Select a 10μF to 22μF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C_{IN}. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN(MIN)} = \frac{D \cdot (1 - D)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_{SW}}$$

$$D = \frac{V_O}{V_{IN}}$$

The peak ripple voltage occurs when V_{IN} = 2x V_O (50% duty cycle), resulting in a minimum output capacitance recommendation:

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10μF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6μF. The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{D \cdot (1 - D)}$$

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

V_{OUT} (V)	Inductor Selection
1.2	TDK, VLS252012T-R47N2R1, 0.47μH, I_{SAT} = 3.7A, DCR = 47mΩ
1.8	Sumida, CDRH38D16R/HP, 0.9μH, I_{SAT} = 2.66A, DCR = 20mΩ
2.5	TDK, VLS252012T-1R0N1R7, 1.0μH, I_{SAT} = 2.7A, DCR = 88mΩ
3.3	TDK, VLF5014AT-1R5M1R7, 1.5μH, I_{SAT} = 2.9, DCR = 51mΩ

Table 1: Inductor Selection.

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

occurs when $V_{IN} = 2 \cdot V_O$.

The calculated value varies with the input voltage and is at a maximum when V_{IN} is twice the output voltage V_{OUT}. The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2114A. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

The proper placement of the input capacitor can be seen in the evaluation board layout shown in Figure 2.

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR/ESL bypass ceramic capacitor. This dampens the high Q network and stabilizes the system.

Output Capacitor

The output capacitor limits the output ripple and maintains the output voltage during large load transitions. A 22μF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_O}{V_{DROOP} \cdot F_{SW}}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 20μF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

Adjustable Feedback Network

The output voltage on the AAT2114A is programmed with external resistors R_3 and R_4. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Therefore, the recommended value range for R_4 is 59kΩ for good noise immunity or 221kΩ for reduced no load input current.

The external resistor R_3, combined with an external 100pF feed forward capacitor (C_5 in Figure 1), delivers enhanced transient response for extreme pulsed load applications and reduces ripple in light load conditions. The external resistors set the output voltage according to the following equation:

$$V_O = 0.6V \cdot \left(1 + \frac{R_3}{R_4}\right)$$

or solving for R_3:

$$R_3 = \left(\frac{V_O}{0.6V} - 1\right) \cdot R_4$$

The typical circuit shown in the AAT2114A evaluation schematic is intended to be general purpose and suitable for most applications. In applications where transient load steps are more severe and the restriction on output voltage deviation is more stringent, some simple adjustments can be made. The schematic in Figure 1 shows the configuration for improved transient response in an application where the output is stepped down to 1.2V. The adjustments consist of increasing the value of the feed forward capacitor C_5 to 100pF.

V_{OUT} (V)	R_4 = 59.0kΩ R_3 (kΩ)	R_4 = 221kΩ R_3 (kΩ)
1.0	39.2	147
1.2	59	221
1.5	88.7	332
1.8	118	442
2.5	187	698
3.3	267	1M

Table 2: Feedback Resistors for Various Output Voltages.

Thermal Calculations

There are three types of losses associated with the AAT2114A step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the losses is given by:

$$P_{LOSS(RES)} = I_O^2 \cdot \left[R_{DS(ON)H} \cdot \left(\frac{V_O}{V_{IN}}\right) + R_{DS(ON)L} \cdot \left(\frac{V_{IN} - V_O}{V_{IN}}\right)\right] + (t_{SW} \cdot F_{SW} \cdot I_{OUT} + I_Q) \cdot V_{IN}$$

I_Q is the step-down converter quiescent current. The term t_{SW} is the time to charge up the gate capacitor of the high-side P-channel MOSFET, and used to estimate the full load step-down converter switching losses.

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

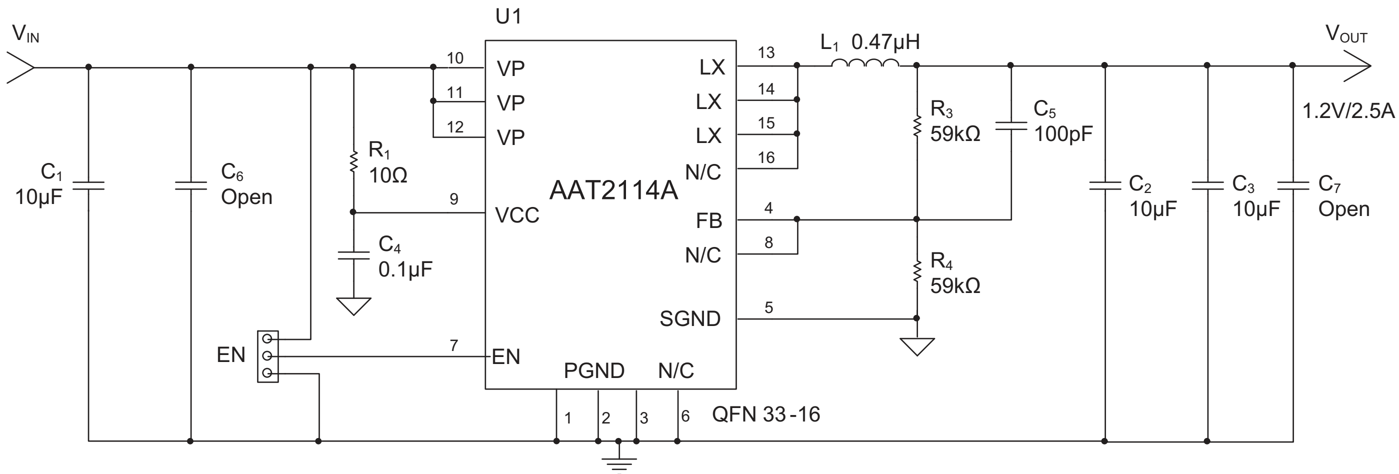
Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the QFN33-16 package, which is 43°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB}$$

Layout Considerations

The suggested PCB layout for the AAT2114A is shown in Figures 2 and 3. The following guidelines should be used to help ensure a proper layout.

1. The input capacitor (C_1) should connect as close as possible to VP and PGND.
2. C_2, C_3 and L_1 should be connected as close as possible. The connection of L_1 to the LX pin should be as short as possible.
3. The feedback trace or FB pin should be separate from any power trace and connect as close as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation.
4. The resistance of the trace from the load return to PGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. Connect unused signal pins to ground to avoid unwanted noise coupling.



U1	AAT2114AIVN, Skyworks, 3MHz Fast Transient, 2.5A Step-Down Converter, QFN33-16, 3x3mm
C1, C2, C3	GRM188R60J106ME47D, Murata, Cap, MLC, 10μF/6.3V, 0603
C4	0.1μF/6.3V, 0402
C5	UMK105CG101JV-F10nF, Taiyo Yuden, 100pF/50V, 0402
L1	252012T-R47N2R1, TDK, 0.47μH, I_{SAT} = 3.7A, DCR = 0.047Ω, 2.5x2x1.2mm, shielded chip inductor
R1	Carbon film resistor, 10Ω, 1%, 0201
R3, R4	Carbon film resistor, 59kΩ, 1%, 0402

Figure 1: AAT2114AIVN Evaluation Board Schematic and Bill of Materials.

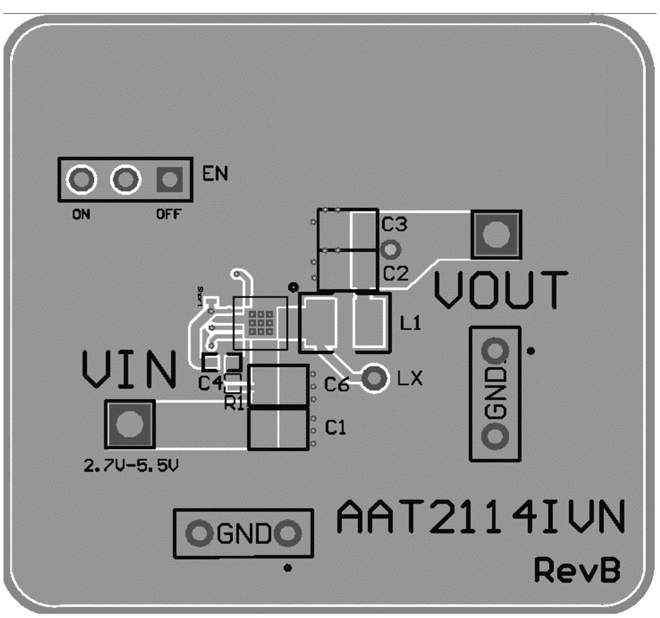


Figure 2: AAT2114AIVN Evaluation Board Top Side Layout.

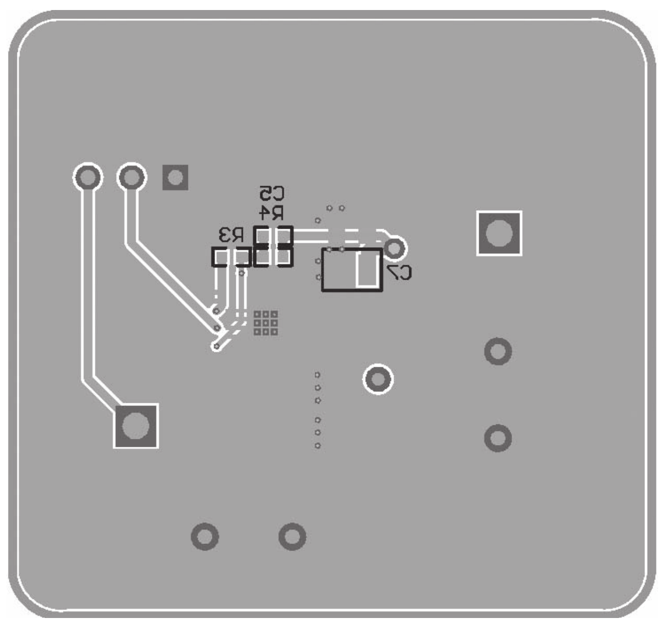


Figure 3: AAT2114AIVN Evaluation Board Bottom Side Layout.

Skyworks Solutions, Inc. • Phone [781] 376-3000 • Fax [781] 376-3100 • sales@skyworksinc.com • www.skyworksinc.com

2.5A Low-Noise, Fast Transient 3MHz Step-Down Regulator

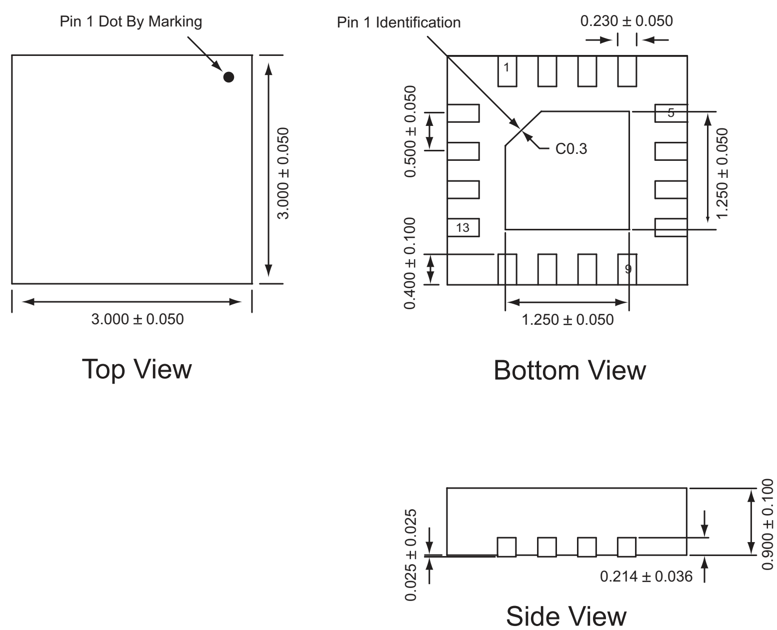
Ordering Information

Package	Output	Marking[1]	Part Number (Tape and Reel)[2]
QFN33-16	Adjustable (V_{FB} = 0.6V)	M7XYY	**AAT2114AIVN-0.6-T1**

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

Package Information

QFN33-16[3]



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.
3. The leadless package family, which includes QFN, TQFN, DFN, TDFN, and STDFN, has exposed copper (unplated) at the end of the lead terminals due to manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.