ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE4070B and NTE4070BT
Integrated Circuit
CMOS, Quad Exclusive OR Gate

Description:

The NTE4070B (14–Lead DIP) and NTE4070BT (SOIC–14) are quad exclusive OR gates constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

Features:

- Quiescent Current = 0.5nA Typ/Pkg at 5 Vdc
- Noise Immunity = 45% of V_{DD} (Typ)
- Supply Voltage Range = 3Vdc to 18Vdc
- All Outputs Buffered
- Capable of Driving Two Low–Power TTL Loads, One Low–Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs

Absolute Maximum Ratings: (Voltages Referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), V_{in} . . . . . –0.5 to V_{DD} + 0.5V
DC Current Drain (Per Pin), I 10mA
Operating Temperature Range, T_{sA} . . . . . –55 to +125°C
Storage Temperature Range, T_{stg} . . . . . –65 to +150°C
Lead Temperature (8–Seconds Soldering), T_L . . . . . 260°C

Note 1. These devices contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation is is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage “0” Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
“1” Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage “0” Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
“1” Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
(V_{OH} = 9.5Vdc)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
(V_{OH} = 13.5Vdc)		15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)		10	–	0.5	–	0.0010	0.5	–	15	µAdc
		15	–	1.0	–	0.0015	1.0	–	30	µAdc
Total Supply Current	I_T	5.0	I_T = (0.3µA/kHz) f + I_{DD}							µAdc
(Dynamic plus Quiescent, Per Package, C_L = 50pF on all outputs, all buffers switching, Note 3, Note 4)		10	I_T = (0.6µA/kHz) f + I_{DD}							µAdc
		15	I_T = (0.8µA/kHz) f + I_{DD}							µAdc

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 1 \times 10^{-3}(C_L - 50)\, V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in volts and f in kHz is input frequency.

Note 3. The formulas given are for the typical characteristics only at +25°C.

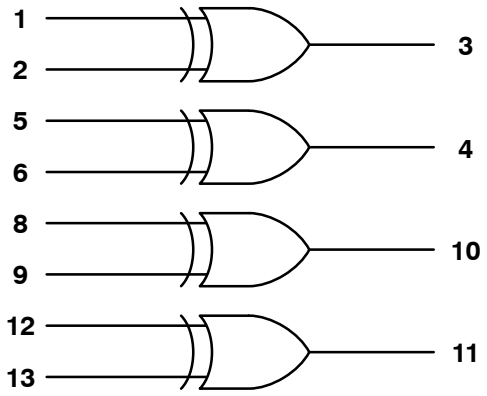
Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Times t_{TLH} ,t_{THL} = (1.35ns/pf) C_L + 33ns	t_{TLH}, t_{THL}	5.0	–	100	200	ns
t_{TLH} ,t_{THL} = (0.60ns/pf) C_L + 20ns		10	–	50	100	ns
t_{TLH} ,t_{THL} = (0.40ns/pf) C_L + 20ns		15	–	40	80	ns
Propagation Delay Time t_{PLH}, t_{PHL} = (0.90ns/pf) C_L + 115ns	t_{PLH}. t_{PHL}	5.0	–	175	350	ns
t_{PLH}, t_{PHL} = (0.36ns/pf) C_L + 47ns		10	–	75	150	ns
t_{PLH}, t_{PHL} = (0.26ns/pf) C_L + 37ns		15	–	50	100	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

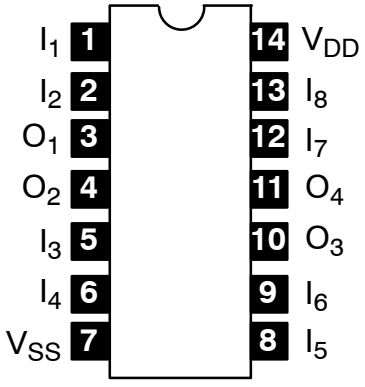
Note 3. The formulas given are for the typical characteristics only at +25°C.

Logic Diagram

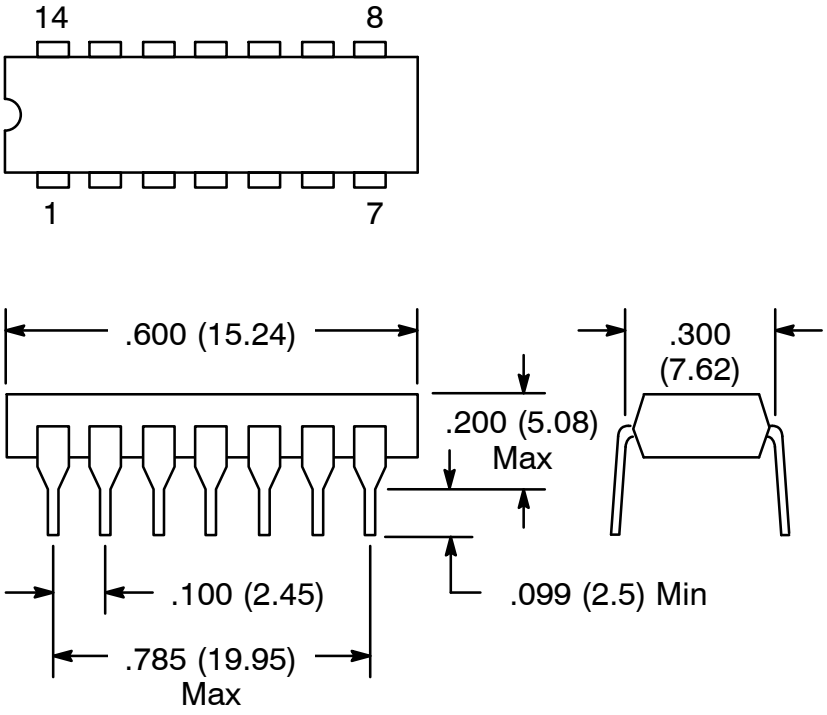


V_{DD} = Pin14
V_{SS} = Pin7

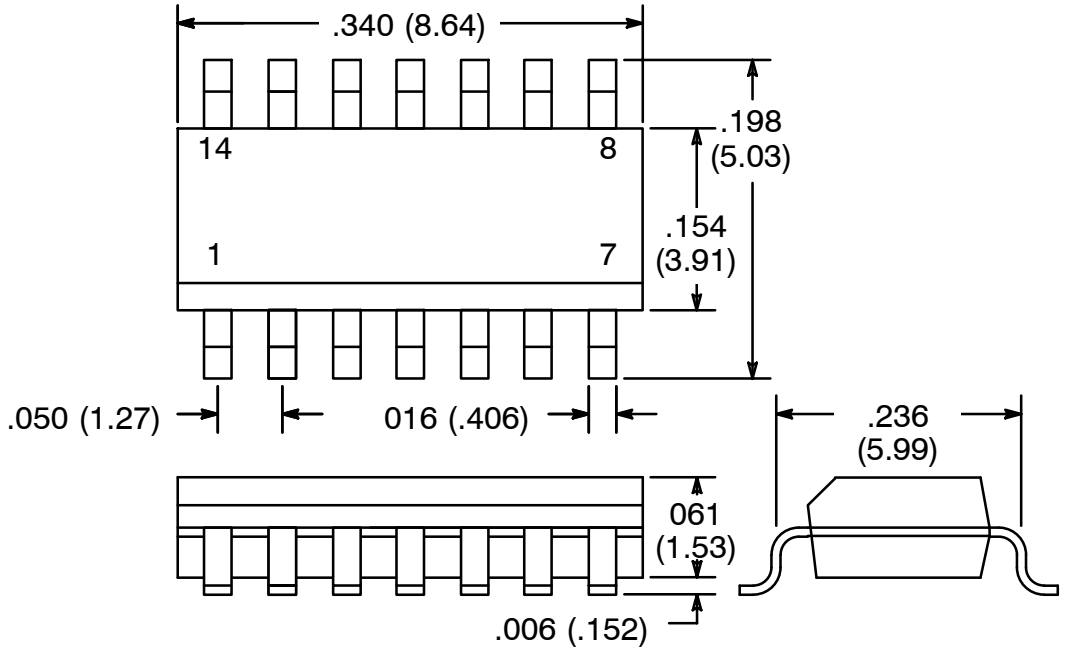
Pin Connection Diagram



NTE4070B



NTE4070BT



NOTE: Pin1 on Beveled Edge