# TDA8024

## Standard smart card interface

Rev. 4.0 — 3 June 2016 Product data sheet

## 1. General description

The TDA8024 is a complete and cost-efficient analog interface for asynchronous 3 V or 5 V smart cards. It can be placed between the card and the microcontroller to perform all supply, protection and control functions. Very few external components are required. The TDA8024AT is a direct replacement for the TDA8004AT.

More information can be obtained from the NXP internet site (www.nxp.com) and from *"Application note AN10141"*.

**CAUTION**

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 2. Features and benefits

- IC card interface
- 3 V or 5 V supply for the IC ($V_{DD}$ and GND)
- Three specifically protected half-duplex bidirectional buffered I/O lines to card contacts C4, C7 and C8
- DC-to-DC converter for $V_{CC}$ generation separately powered from a 5 V ± 20% supply ($V_{DDP}$ and PGND)
- 3 V or 5 V ± 5% regulated card supply voltage ($V_{CC}$) with appropriate decoupling has the following capabilities:
  - $I_{CC}$ < 80 mA at $V_{DDP}$ = 4 V to 6.5 V
  - Handles current spikes of 40 nAs up to 20 MHz
  - Controls rise and fall times
  - Filtered overload detection at approximately 120 mA
- Thermal and short-circuit protection on all card contacts
- Automatic activation and deactivation sequences; initiated by software or by hardware in the event of a short-circuit, card take-off, overheating, $V_{DD}$ or $V_{DDP}$ drop-out
- Enhanced ESD protection on card side (>6 kV)
- 26 MHz integrated crystal oscillator
- Clock generation for cards up to 20 MHz (divided by 1, 2, 4 or 8 through CLKDIV1 and CLKDIV2 signals) with synchronous frequency changes
- Non-inverted control of RST via pin RSTIN
- ISO 7816, GSM11.11 and EMV (payment systems) compatibility

- Supply supervisor for spike-killing during power-on and power-off and Power-on reset (threshold fixed internally or externally by a resistor bridge); not for TDA8024AT
- Built-in debounce on card presence contacts
- One multiplexed status signal $\overline{OFF}$

## 3. Applications

- IC card readers for banking
- Electronic payment
- Identification
- Pay TV

## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Power supplies** | | | | | | |
| $V_{DD}$ | supply voltage | | 2.7 | - | 6.5 | V |
| $V_{DDP}$ | DC-to-DC converter supply voltage | $V_{CC}$ = 5 V; $\|I_{CC}\|$ < 80 mA | 4.0 | 5.0 | 6.5 | V |
| | | $V_{CC}$ = 5 V; $\|I_{CC}\|$ < 20 mA | 3.0 | - | 6.5 | V |
| $I_{DD}$ | supply current | $V_{DD}$ = 3.3 V; $f_{XTAL}$ = 10 MHz | | | | |
| | | card inactive | - | - | 1.2 | mA |
| | | card active; $f_{CLK} = f_{XTAL}$; $C_L$ = 30 pF | - | - | 1.5 | mA |
| $I_{DDP}$ | DC-to-DC converter supply current | $V_{DDP}$ = 5 V; $f_{XTAL}$ = 10 MHz | | | | |
| | | inactive mode | - | - | 0.1 | mA |
| | | active mode; $f_{CLK} = f_{XTAL}$; $C_L$ = 30 pF; $\|I_{CC}\|$ = 0 | - | - | 10 | mA |
| **Card supply** | | | | | | |
| $V_{CC}$ | card suppy voltage (including ripple voltage) | 5 V card: | | | | |
| | | card active; $\|I_{CC}\|$ < 80 mA DC | 4.75 | 5.0 | 5.25 | V |
| | | card active; current pulses $I_p$ = 40 nAs | 4.65 | 5.0 | 5.25 | V |
| | | 3 V card: | | | | |
| | | card active; $\|I_{CC}\|$ < 65 mA DC | 2.85 | 3.0 | 3.15 | V |
| | | card active; current pulses $I_p$ = 40 nAs | 2.76 | 3.0 | 3.20 | V |
| $V_{CC(ripple)(p-p)}$ | ripple voltage on $V_{CC}$ (peak-to-peak value) | $f_{ripple}$ = 20 kHz to 200 MHz | - | - | 350 | mV |
| $\|I_{CC}\|$ | card supply current | $V_{CC}$ = 0 to 5 V | - | - | 80 | mA |
| | | $V_{CC}$ = 0 to 3 V | - | - | 65 | mA |

**Table 1. Quick reference data** *…continued*

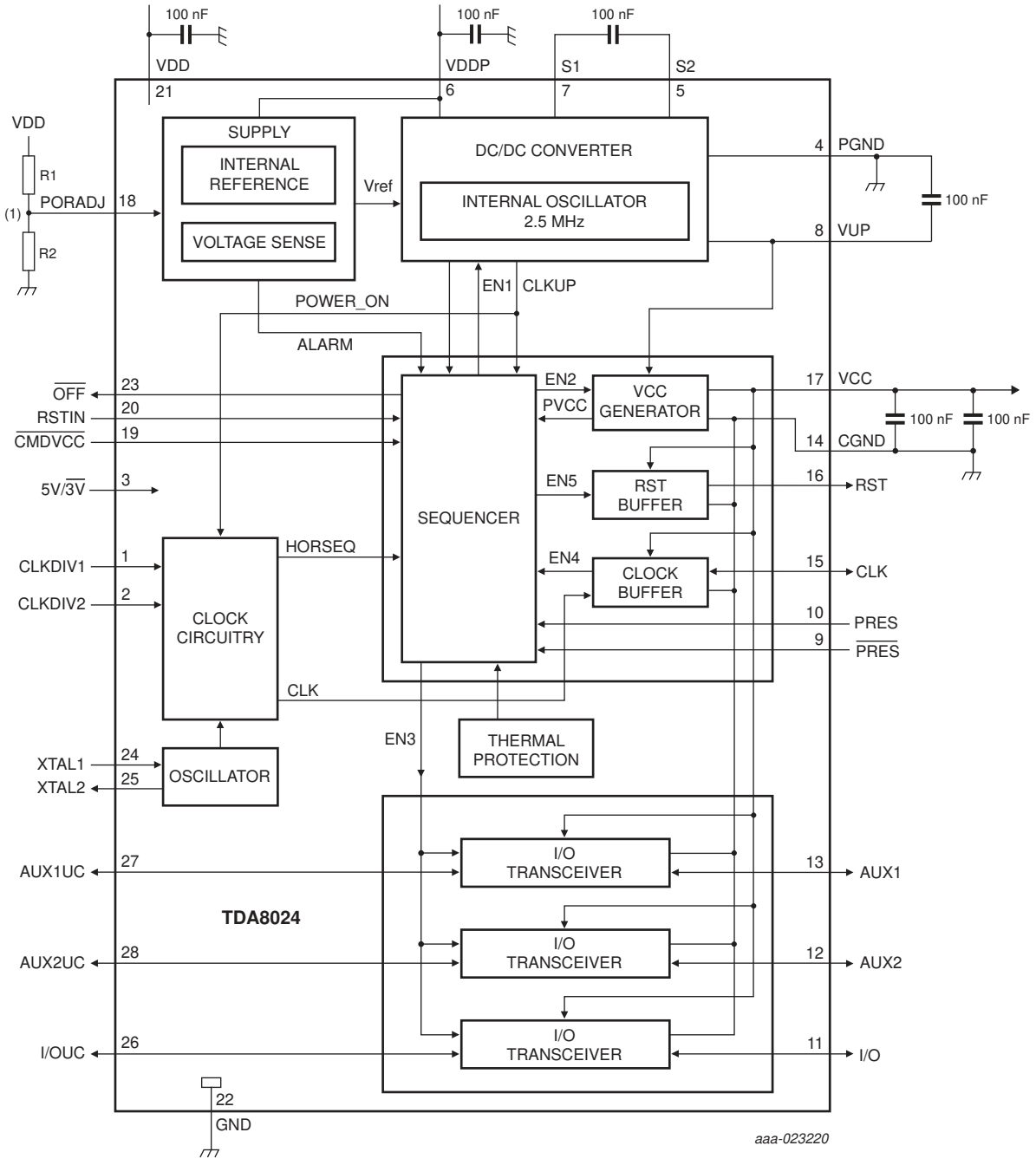
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **General** | | | | | | | |
| $t_{de}$ | deactivation time | | | 50 | 80 | 100 | µs |
| $P_{tot}$ | total power dissipation | continuous operation; $T_{amb}$ = −25 to +85 °C | | - | - | 0.56 | W |
| $T_{amb}$ | ambient temperature | | | −25 | - | +85 | °C |

# 5. Ordering information

**Table 2. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TDA8024T/C1 | SO28 | plastic small outline package; 28 leads; body width 7.5 mm | SOT136-1 |
| TDA8024AT/C1 | SO28 | plastic small outline package; 28 leads; body width 7.5 mm | SOT136-1 |
| TDA8024TT/C1 | TSSOP28 | plastic thin shrink small outline package; 28 leads; body width 4.4 mm, gold wires | SOT361-1 |
| TDA8024TT/C1/S1 | TSSOP28 | plastic thin shrink small outline package; 28 leads; body width 4.4 mm, copper wire | SOT361-1 |

# 6. Block diagram




(1) Optional external resistor bridge. If this bridge is not required pin 18 should be connected to ground; see Section 8.2.2. Pin 18 is not connected in the TDA8024AT.

**Fig 1. Block diagram**

# 7. Pinning information

## 7.1 Pinning

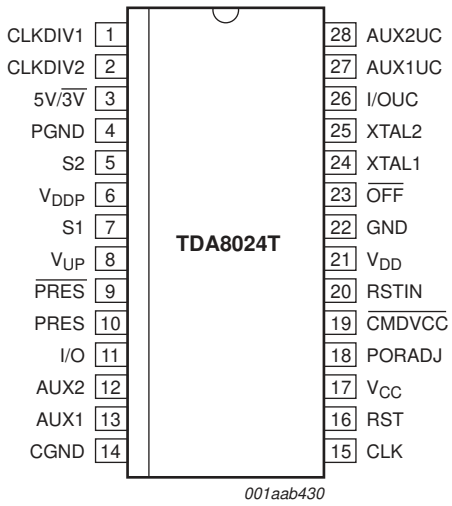



Fig 2. Pin configuration TDA8024T

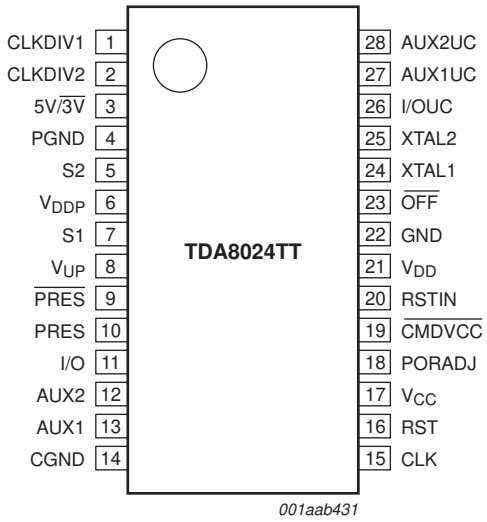



Fig 3. Pin configuration TDA8024TT

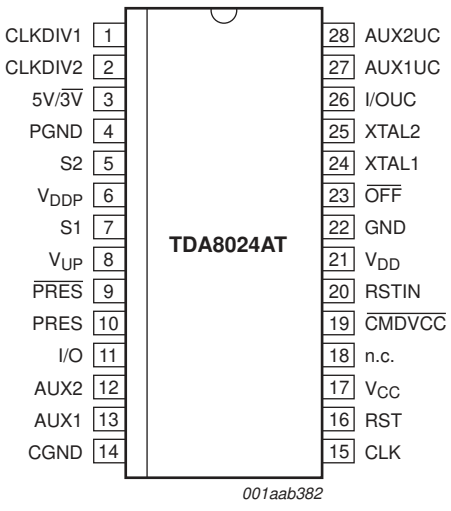



Fig 4. Pin configuration TDA8024AT

## 7.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Type | Description |
|---|---|---|---|
| CLKDIV1 | 1 | I | CLK frequency selection input 1 |
| CLKDIV2 | 2 | I | CLK frequency selection input 2 |
| 5V/$\overline{3V}$ | 3 | I | card supply voltage selection input; $V_{CC}$ = 5 V (HIGH) or $V_{CC}$ = 3 V (LOW) |
| PGND | 4 | S | DC-to-DC converter power supply ground |
| S2 | 5 | I/O | DC-to-DC converter capacitor; connected between pins S1 and S2; C = 100 nF with ESR < 100 mΩ |
| $V_{DDP}$ | 6 | S | DC-to-DC converter power supply voltage |
| S1 | 7 | I/O | DC-to-DC converter capacitor; connected between pins S1 and S2; C = 100 nF with ESR < 100 mΩ |
| $V_{UP}$ | 8 | I/O | DC-to-DC converter output decoupling capacitor connection; C = 100 nF with ESR < 100 mΩ must be connected between $V_{UP}$ and PGND |
| $\overline{PRES}$ | 9 | I | card presence contact input (active LOW); if PRES or $\overline{PRES}$ is active, the card is considered 'present' and a built-in debounce feature of 8 ms (typ.) is activated |
| PRES | 10 | I | card presence contact input (active HIGH); if PRES or $\overline{PRES}$ is active, the card is considered 'present' and a built-in debounce feature of 8 ms (typ.) is activated |
| I/O | 11 | I/O | data line to/from card reader contact C7; integrated 11 kΩ pull-up resistor to $V_{CC}$ |
| AUX2 | 12 | I/O | data line to/from card reader contact C8; integrated 11 kΩ pull-up resistor to $V_{CC}$ |
| AUX1 | 13 | I/O | data line to/from card reader contact C4; integrated 11 kΩ pull-up resistor to $V_{CC}$ |
| CGND | 14 | S | card signal ground |
| CLK | 15 | I/O | card clock to/from card reader contact C3 |
| RST | 16 | O | card reset output from card reader contact C2 |
| $V_{CC}$ | 17 | S | card supply voltage to card reader contact C1; decoupled to CGND via 2 × 100 nF or 100 + 220 nF capacitors with ESR < 100 mΩ[1] |
| PORADJ | 18 | I | Power-on reset threshold adjustment input for changing the reset threshold with an external resistor bridge; doubles the width of the POR pulse when used; this pin is not connected for the TDA8024AT |
| $\overline{CMDVCC}$ | 19 | I | input from the host to start activation sequence (active LOW) |
| RSTIN | 20 | I | card reset input from the host |
| $V_{DD}$ | 21 | S | supply voltage |
| GND | 22 | S | ground |
| $\overline{OFF}$ | 23 | O | NMOS interrupt output to the host (active LOW); 20 kΩ integrated pull-up resistor to $V_{DD}$ |
| XTAL1 | 24 | I | crystal connection or input for external clock |

**Table 3. Pin description** *...continued*

| Symbol | Pin | Type | Description |
|---|---|---|---|
| XTAL2 | 25 | O | crystal connection (leave open-circuit if external clock source is used) |
| I/OUC | 26 | I/O | host data I/O line; integrated 11 kΩ pull-up resistor to $V_{DD}$ |
| AUX1UC | 27 | I/O | auxiliary data line to/from the host; integrated 11 kΩ pull-up resistor to $V_{DD}$ |
| AUX2UC | 28 | I/O | |

[1] The noise margin on $V_{CC}$ will be higher with the 220 nF capacitor.

# 8. Functional description

Throughout this document it is assumed that the reader is familiar with ISO7816 terminology.

## 8.1 Power supply

The supply pins for the IC are $V_{DD}$ and GND. $V_{DD}$ should be in the range of 2.7 V to 6.5 V. All signals interfacing with the system controller are referred to $V_{DD}$, therefore $V_{DD}$ should also supply the system controller. All card reader contacts remain inactive during power-on or power-off.

The internal circuits are maintained in the reset state until $V_{DD}$ reaches $V_{th2} + V_{hys2}$ and for the duration of the internal Power-on reset pulse, $t_W$ (see Figure 5). When $V_{DD}$ falls below $V_{th2}$, an automatic deactivation of the contacts is performed.

A DC-to-DC converter is incorporated to generate the 5 V or 3 V card supply voltage ($V_{CC}$). The DC-to-DC converter should be supplied separately by $V_{DDP}$ and PGND. Due to the possibility of large transient currents, the two 100 nF capacitors of the DC-to-DC converter should be located as near as possible to the IC and have an ESR less than 100 mΩ.

The DC-to-DC converter functions as a voltage doubler or a voltage follower according to the respective values of $V_{CC}$ and $V_{DDP}$ (both have thresholds with a hysteresis of 100 mV).

The DC-to-DC converter function changes as follows.

- $V_{CC}$ = 5 V and $V_{DDP}$ > 5.8 V; voltage follower
- $V_{CC}$ = 5 V and $V_{DDP}$ < 5.7 V; voltage doubler
- $V_{CC}$ = 3 V and $V_{DDP}$ > 4.1 V; voltage follower
- $V_{CC}$ = 3 V and $V_{DDP}$ < 4.0 V; voltage doubler.

Supply voltages $V_{DD}$ and $V_{DDP}$ may be applied to the IC in any sequence.

After powering the device, $\overline{OFF}$ remains LOW until $\overline{CMDVCC}$ is set HIGH.

During power off, $\overline{OFF}$ falls LOW when $V_{DD}$ is below the falling threshold voltage.

## 8.2 Voltage supervisor

### 8.2.1 Without external divider on pin PORADJ (or with TDA8024AT)

The voltage supervisor surveys the $V_{DD}$ supply. A defined reset pulse of approximately 8 ms ($t_W$) is used internally to keep the IC inactive during power-on or power-off of the $V_{DD}$ supply (see Figure 5).

As long as $V_{DD}$ is less than $V_{th2} + V_{hys2}$, the IC remains inactive whatever the levels on the command lines. This state also lasts for the duration of $t_W$ after $V_{DD}$ has reached a level higher than $V_{th2} + V_{hys2}$.

When $V_{DD}$ falls below $V_{th2}$, a deactivation sequence of the contacts is performed.

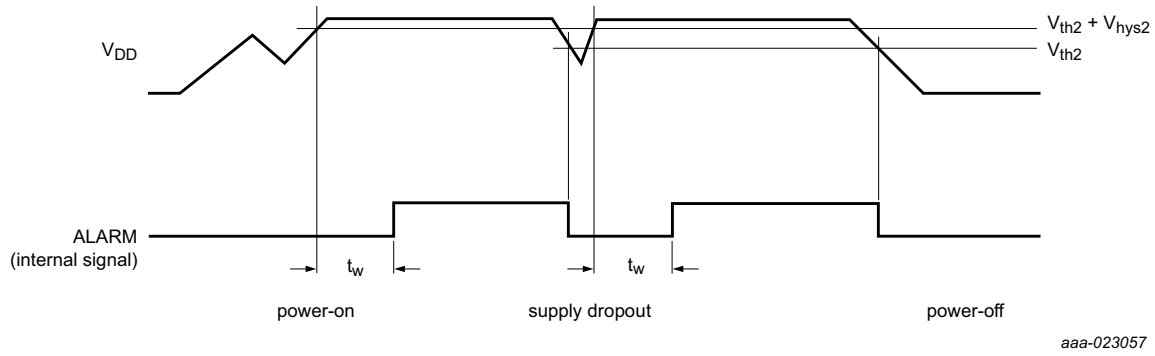



**Fig 5. Voltage supervisor**

### 8.2.2 With an external divider on pin PORADJ (not for the TDA8024AT)

If an external resistor bridge is connected to pin PORADJ (R1 and R2 in Figure 1), then the following occurs:

- The internal threshold voltage $V_{th2}$ is overridden by the external voltage and by the hysteresis, therefore:

$$V_{th2(ext)(rise)} = \left(1 + \frac{R1}{R2}\right) \times \left(V_{bridge} + \frac{V_{hys(ext)}}{2}\right)$$

$$V_{th2(ext)(fall)} = \left(1 + \frac{R1}{R2}\right) \times \left(V_{bridge} - \frac{V_{hys(ext)}}{2}\right)$$

  where $V_{bridge}$ = 1.25 V typ. and $V_{hys(ext)}$ = 60 mV typ.

- The reset pulse width $t_W$ is doubled to approximately 16 ms.

Input PORADJ is biased internally with a pull-down current source of 4 μA which is removed when the voltage on pin PORADJ exceeds 1 V. This ensures that after detection of the external bridge by the IC during power-on, the input current on pin PORADJ does not cause inaccuracy of the bridge voltage.

The minimum threshold voltage should be higher than 2 V.

The maximum threshold voltage may be up to $V_{DD}$.

### 8.2.3 Applications examples

The voltage supervisor is used as Power-on reset and as supply dropout detection during a card session.

Supply dropout detection is to ensure that a proper deactivation sequence is followed before the voltage is too low.

For the internal voltage supervisor to function, the system microcontroller should operate down to 2.35 V to ensure a proper deactivation sequence. If this is not possible, external resistor values can be chosen to overcome the problem.

#### 8.2.3.1 Microcontroller requiring a 3.3 V ± 20 % supply

For a microcontroller supplied by 3.3 V with a ±5% regulator and with resistors R1, R2 having a ±1% tolerance, the minimum supply voltage is 3.135 V.

$V_{PORADJ} = k \times V_{DD}$, where $k = \frac{S1}{S1 + S2}$ with S1 and S2 the actual values of nominal resistors R1 and R2.

This can be shown as:

$0.99 \times R1 < S1 < 1.01 \times R1$ and

$0.99 \times R2 < S2 < 1.01 \times R2$

Transposed, this becomes

$$1 + \left(0.98 \times \frac{R1}{R2}\right) = 1 + \left(\frac{0.99}{1.01}\right) \times \frac{R1}{R2} < \frac{1}{k}$$

$$\frac{1}{k} < 1 + \left(\frac{1.01}{0.99}\right) \times \frac{R1}{R2} = 1 + \left(1.02 \times \frac{R1}{R2}\right)$$

If $V1 = V_{th(ext)(rise)(max)}$ and $V2 = V_{th(ext)(fall)(min)}$ activation will always be possible if $V_{PORADJ} > V1$ and deactivation will always be done for $V_{PORADJ} < V2$.

Activation is always possible for $V_{DD} > \frac{V1}{k}$ and deactivation is always possible for $V_{DD} < \frac{V2}{k}$

That is V1 = 1.31 V and V2 = 1.19 V and $\frac{R1}{R2} < \left(\frac{3.135}{1.31} - 1\right) \times 0.98 = 1.365$

Suppose R1 + R2 = 100 kΩ, then $R2 = \frac{100\,k\Omega}{2.365} = 42.3\,k\Omega$ and R1 = 57.7 kΩ.

Deactivation will be effective at V2 × (1 + 1.02 × 1.365) = 2.847 V in any case.

If the microcontroller continues to function down to 2.80 V, the slew rate on $V_{DD}$ should be less than 2 V/ms to ensure that clock CLK is correctly delivered to the card until time $t_{12}$ (see Figure 9).

#### 8.2.3.2 Microcontroller requiring a 3.3 V ± 10% supply

For a microcontroller supplied by a 3.3 V with a ±1% regulator and with resistors R1, R2 having a ±0.1% tolerance, the minimum supply voltage is 3.267 V.

The same calculations as in Section 8.2.3.1 conclude:

$$\frac{R1}{R2} < \left(\frac{3.267}{1.310} - 1\right) \times 0.998 = 1.491$$

Therefor $R2 = \frac{100\ k\Omega}{2.49} = 40.14\ k\Omega$ and R1 = 59.86 kΩ.

Deactivation will be effective at V2 × (1 + 1.002 × 1.491) = 2.967 V in any case.

If the microcontroller continues to function down to 2.97 V, the slew rate on $V_{DD}$ should be less than 0.20 V/ms to ensure that clock CLK is correctly delivered to the card until time $t_{12}$ (see Figure 9).

## 8.3 Clock circuitry

The card clock signal (CLK) is derived from a clock signal input to pin XTAL1 or from a crystal operating at up to 26 MHz connected between pins XTAL1 and XTAL2.

The clock frequency can be $f_{XTAL}$, ½ × $f_{XTAL}$, ¼ × $f_{XTAL}$ or ⅛ × $f_{XTAL}$. Frequency selection is made via inputs CLKDIV1 and CLKDIV2 (see Table 4).

**Table 4. Clock frequency selection[1]**

| CLKDIV1 | CLKDIV2 | $f_{CLK}$ |
|---|---|---|
| 0 | 0 | $\frac{f_{XTAL}}{8}$ |
| 0 | 1 | $\frac{f_{XTAL}}{4}$ |
| 1 | 1 | $\frac{f_{XTAL}}{2}$ |
| 1 | 0 | $f_{XTAL}$ |

[1] The status of pins CLKDIV1 and CLKDIV2 must not be changed simultaneously; a delay of 10 ns minimum between changes is needed; the minimum duration of any state of CLK is eight periods of XTAL1.

The frequency change is synchronous, which means that during transition no pulse is shorter than 45% of the smallest period, and that the first and last clock pulses about the instant of change have the correct width.

When changing the frequency dynamically, the change is effective for only eight periods of XTAL1 after the command.

The duty factor of $f_{XTAL}$ depends on the signal present at pin XTAL1.

In order to reach a 45% to 55% duty factor on pin CLK, the input signal on pin XTAL1 should have a duty factor of 48% to 52% and transition times of less than 5% of the input signal period.

If a crystal is used, the duty factor on pin CLK may be 45% to 55% depending on the circuit layout and on the crystal characteristics and frequency.

In other cases, the duty factor on pin CLK is guaranteed between 45% and 55% of the clock period.

The crystal oscillator runs as soon as the IC is powered up. If the crystal oscillator is used, or if the clock pulse on pin XTAL1 is permanent, the clock pulse is applied to the card as shown in the activation sequences shown in Figure 7 and 8.

If the signal applied to XTAL1 is controlled by the system microcontroller, the clock pulse will be applied to the card when it is sent by the system microcontroller (after completion of the activation sequence).

## 8.4 I/O transceivers

The three data lines I/O, AUX1 and AUX2 are identical.

The Idle-state is realized by both I/O and I/OUC lines being pulled HIGH via a 11 kΩ resistor (I/O to $V_{CC}$ and I/OUC to $V_{DD}$).

Pin I/O is referenced to $V_{CC}$, and pin I/OUC to $V_{DD}$, thus allowing operation when $V_{CC}$ is not equal to $V_{DD}$.

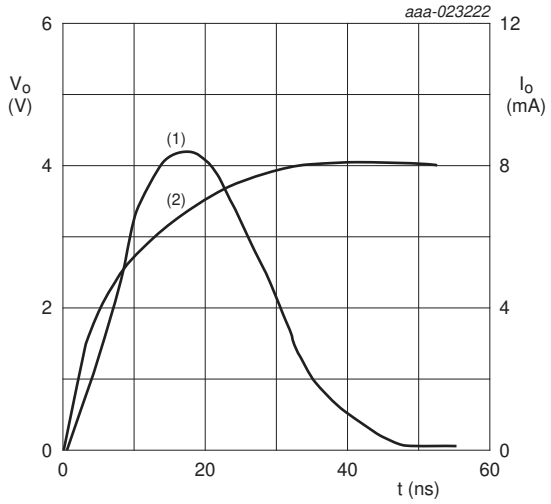
The first side of the transceiver to receive a falling edge becomes the master. An anti-latch circuit disables the detection of falling edges on the line of the other side, which then becomes a slave.

After a time delay $t_{d(edge)}$, an N-transistor on the slave side is turned on, thus transmitting the logic 0 present on the master side.

When the master side returns to logic 1, a P-transistor on the slave side is turned on during the time delay $t_{pu}$ and then both sides return to their idle states.

This active pull-up feature ensures fast LOW-to-HIGH transitions; as shown in Figure 6, it is able to deliver more than 1 mA at an output voltage of up to $0.9V_{CC}$ into an 80 pF load. At the end of the active pull-up pulse, the output voltage depends only on the internal pull-up resistor and the load current.

The current to and from the card I/O lines is limited internally to 15 mA and the maximum frequency on these lines is 1 MHz.




(1) Current

(2) Voltage

**Fig 6. I/O, AUX1 and AUX2 output voltage and current as functions of time during a LOW-to-HIGH transition.**

## 8.5 Inactive mode

After a Power-on reset, the circuit enters the inactive mode. A minimum number of circuits are active while waiting for the microcontroller to start a session:

- All card contacts are inactive (approximately 200 Ω to GND)
- Pins I/OUC, AUX1UC and AUX2UC are in the high-impedance state (11 kΩ pull-up resistor to $V_{DD}$)
- Voltage generators are stopped
- XTAL oscillator is running
- Voltage supervisor is active
- The internal oscillator is running at its low frequency

## 8.6 Activation sequence

After power-on and after the internal pulse width delay, the system microcontroller can check the presence of a card using the signals $\overline{OFF}$ and $\overline{CMDVCC}$ as shown in Table 5.

**Table 5. Card presence indication**

| $\overline{OFF}$ | $\overline{CMDVCC}$ | Indication |
|---|---|---|
| HIGH | HIGH | card present |
| LOW | HIGH | card not present |

If the card is in the reader (this is the case if $\overline{PRES}$ or PRES is active), the system microcontroller can start a card session by pulling $\overline{CMDVCC}$ LOW. The following sequence then occurs (see Figure 6):

1. $\overline{CMDVCC}$ is pulled LOW and the internal oscillator changes to its high frequency ($t_0$).

2. The voltage doubler is started (between $t_0$ and $t_1$).
3. $V_{CC}$ rises from 0 to 5 V (or 3 V) with a controlled slope ($t_2 = t_1 + 1.5 \times T$) where T is 64 times the period of the internal oscillator (approximately 25 μs).
4. I/O, AUX1 and AUX2 are enabled ($t_3 = t_1 + 4T$)

   (these were pulled LOW until this moment).
5. CLK is applied to the C3 contact of the card reader ($t_4$).
6. RST is enabled ($t_5 = t_1 + 7T$).

The clock may be applied to the card using the following sequence:

1. Set RSTIN HIGH.
2. Set $\overline{\text{CMDVCC}}$ LOW.
3. Reset RSTIN LOW between $t_3$ and $t_5$; CLK will start at this moment.
4. RST remains LOW until $t_5$, when RST is enabled to be the copy of RSTIN.
5. After $t_5$, RSTIN has no further affect on CLK; this allows a precise count of CLK pulses before toggling RST.

If the applied clock is not needed, then $\overline{\text{CMDVCC}}$ may be set LOW with RSTIN LOW. In this case, CLK will start at $t_3$ (minimum 200 ns after the transition on I/O), and after $t_5$, RSTIN may be set HIGH in order to obtain an Answer To Request (ATR) from the card.

Activation should not be performed with RSTIN held permanently HIGH.

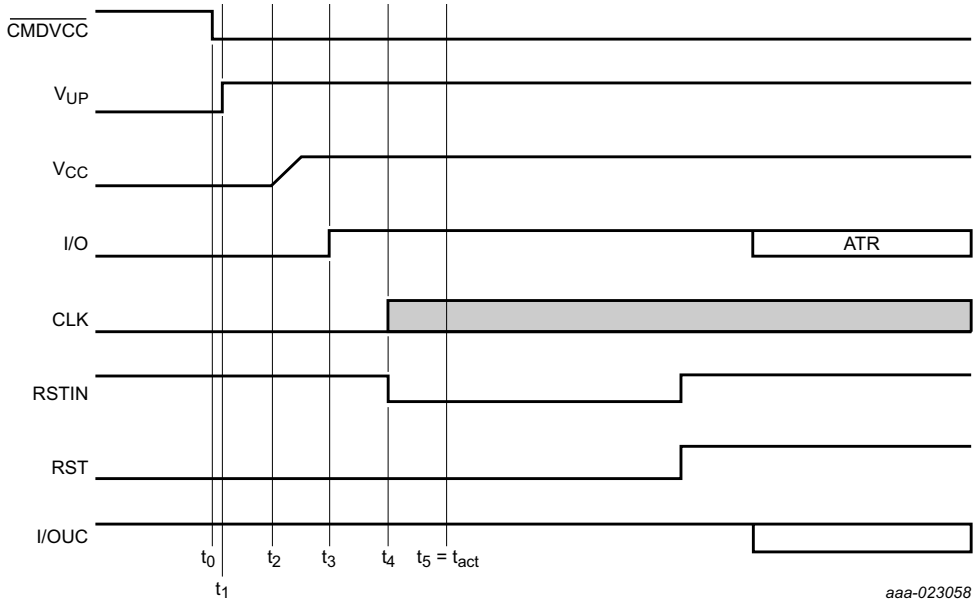



**Fig 7. Activation sequence using RSTIN and $\overline{\text{CMDVCC}}$.**

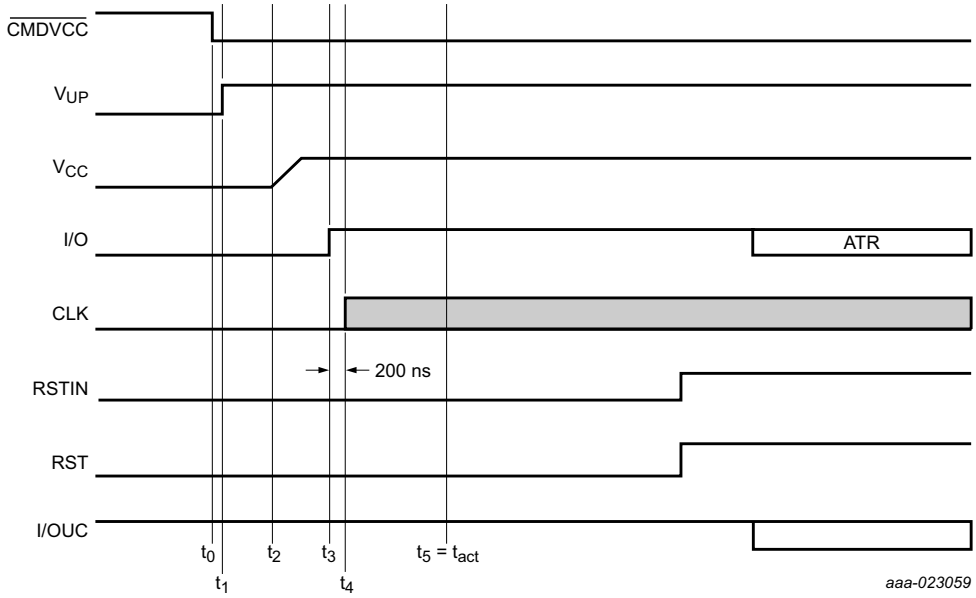



**Fig 8. Activation sequence at $t_3$.**

## 8.7 Active mode

When the activation sequence is completed, the TDA8024 will be in its active mode. Data is exchanged between the card and the microcontroller via the I/O lines. The TDA8024 is designed for cards without $V_{PP}$ (the voltage required to program or erase the internal non-volatile memory).

## 8.8 Deactive sequence

When a session is completed, the microcontroller sets the $\overline{\text{CMDVCC}}$ line HIGH. The circuit then executes an automatic deactivation sequence by counting the sequencer back and finishing in the inactive mode (see Figure 9):

1. RST goes LOW ($t_{10}$).
2. CLK is held LOW ($t_{12} = t_{10} + 0.5 \times T$) where T is 64 times the period of the internal oscillator (approximately 25 μs).
3. I/O, AUX1 and AUX2 are pulled LOW ($t_{13} = t_{10} + T$).
4. $V_{CC}$ starts to fall towards zero ($t_{14} = t_{10} + 1.5 \times T$).
5. The deactivation sequence is complete at $t_{de}$, when $V_{CC}$ reaches its inactive state.
6. $V_{UP}$ falls to zero ($t_{15} = t_{10} + 5T$) and all card contacts become low-impedance to GND; I/OUC, AUX1UC and AUX2UC remain at $V_{DD}$ (pulled-up via a 11 kΩ resistor).
7. The internal oscillator returns to its lower frequency.

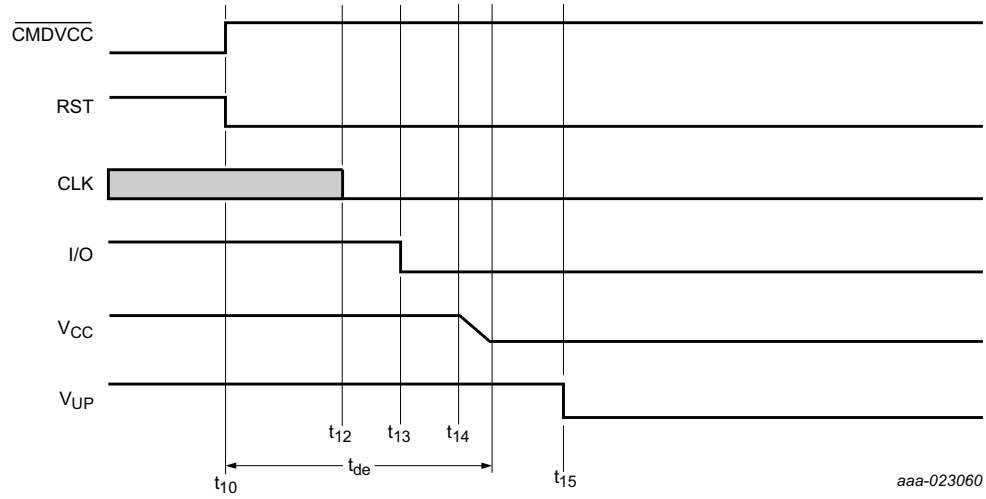



**Fig 9. Deactivation sequence.**

## 8.9 $V_{CC}$ generator

The $V_{CC}$ generator has a capacity to supply up to 80 mA continuously at 5 V and 65 mA at 3 V.

An internal overload detector operates at approximately 120 mA. Current samples to the detector are internally filtered, allowing spurious current pulses up to 200 mA with a duration in the order of µs to be drawn by the card without causing deactivation. The average current must stay below the specified maximum current value.

For reasons of $V_{CC}$ voltage accuracy, a 100 nF capacitor with an ESR < 100 mΩ should be tied to CGND near to pin $V_{CC}$, and a 100 nF or 220 nF capacitor (220 nF is the best choice) with the same ESR should be tied to CGND near card reader contact C1.

## 8.10 Fault detection

The following fault conditions are monitored:

- Short-circuit or high current on $V_{CC}$
- Removal of a card during a transaction
- $V_{DD}$ dropping
- DC-to-DC converter operating out of the specified values ($V_{DDP}$ too low or current from $V_{UP}$ too high)
- Overheating

There are two different cases (see Figure 10):

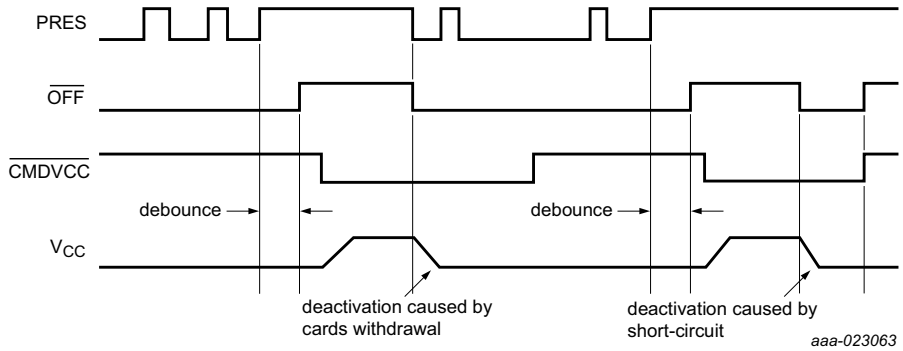
- $\overline{\text{CMDVCC}}$ **HIGH outside a card session.** Output $\overline{\text{OFF}}$ is LOW if a card is not in the card reader, and HIGH if a card is in the reader. A voltage drop on the $V_{DD}$ supply is detected by the supply supervisor, this generates an internal Power-on reset pulse but does not act upon $\overline{\text{OFF}}$. No short-circuit or overheating is detected because the card is not powered-up.

- $\overline{\text{CMDVCC}}$ **LOW within a card session.** Output $\overline{\text{OFF}}$ goes LOW when a fault condition is detected. As soon as this occurs, an emergency deactivation is performed automatically (see Figure 11). When the system controller resets $\overline{\text{CMDVCC}}$ to HIGH it may sense the $\overline{\text{OFF}}$ level again after completing the deactivation sequence. This distinguishes between a hardware problem or a card extraction ($\overline{\text{OFF}}$ goes HIGH again if a card is present).

Depending on the type of card-present switch within the connector (normally-closed or normally-open) and on the mechanical characteristics of the switch, bouncing may occur on the PRES signals at card insertion or withdrawal.

There is a debounce feature in the device with an 8 ms typical duration (see Figure 10). When a card is inserted, output $\overline{\text{OFF}}$ goes HIGH only at the end of the debounce time.

When the card is extracted, an automatic deactivation sequence of the card is performed on the first true/false transition on PRES or $\overline{\text{PRES}}$ and output $\overline{\text{OFF}}$ goes LOW.




See *"Application note AN10141"* for software decision algorithm on $\overline{\text{OFF}}$ signal.

**Fig 10. Behavior of $\overline{\text{OFF}}$, $\overline{\text{CMDVCC}}$, PRES and $V_{CC}$.**

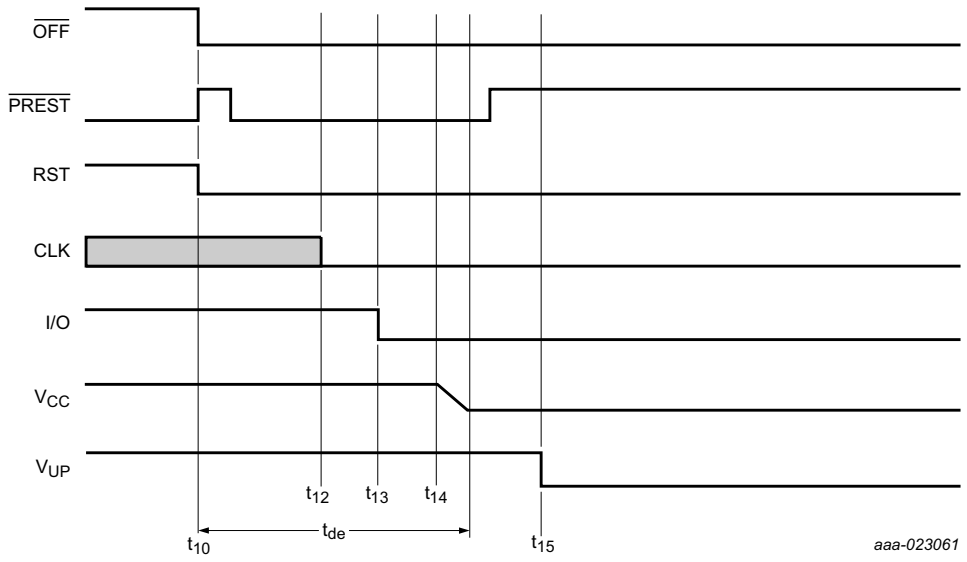



**Fig 11. Emergency deactivation sequence (card extraction)**

# 9. Limiting values

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | −0.3 | +6.5 | V |
| $V_{DDP}$ | DC-to-DC converter supply voltage | | −0.3 | +6.5 | V |
| $V_I$, $V_O$ | voltage on input and output pins | pins XTAL1, XTAL2, 5V/$\overline{3V}$, RSTIN, AUX1UC, $\overline{AUX2UC}$, I/$\overline{OUC}$, CLKDIV1, CLKDIV2, $\overline{CMDVCC}$, $\overline{OFF}$ and PORADJ | −0.3 | +6.5 | V |
| $V_{card}$ | voltage on card pins | pins PRES, $\overline{PRES}$, I/O, RST, AUX1, AUX2 and CLK | −0.3 | +6.5 | V |
| $V_n$ | voltage on other pins | pins $V_{UP}$, S1 and S2 | −0.3 | +6.5 | V |
| $T_{j(max)}$ | maximum junction temperature | | - | 150 | °C |
| $T_{stg}$ | storage temperature | | −55 | +150 | °C |
| $V_{ESD}$ | electrostatic discharge voltage | card contacts in typical application;[1][2] | | | |
| | | pins I/O, $\overline{RST}$, $V_{CC}$, AUX1, AUX2, CLK, PRES and $\overline{PRES}$ | −6 | +6 | kV |
| | | all pins;[1] | | | |
| | | Human Body Model (HBM) [2][3] | −2 | +2 | kV |
| | | Machine Model (MM) [4] | −200 | +200 | V |

[1] All card contacts are protected against any short-circuit with any other card contact.

[2] Every pin withstands the ESD test according to MIL-STD-883C class 3 for card contacts, class 2 for the remaining. Method 3015 (HBM; 1500 Ω and 100 pF) 3 pulses positive and 3 pulses negative on each pin referenced to ground.

[3] In accordance with EIA/JESD22-A114-B, June 2000.

[4] In accordance with EIA/JESD22-A115-A, October 1997.

# 10. Thermal characteristics

**Table 7. Thermal characteristics**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | | |
| | TDA8024T | | 70 | K/W |
| | TDA8024AT | | 70 | K/W |
| | TDA8024TT | | 100[1] | K/W |

[1] This figure was obtained using the following Printed-Circuit Board (PCB) technology: FR, 4 layers, 0.5 mm thickness, class 5, copper thickness 35 µm, Ni/Go plating, ground plane in internal layers.

# 11. Characteristics

**Table 8. Characteristics**

*$V_{DD}$ = 3.3 V; $V_{DDP}$ = 5 V; $T_{amb}$ = 25 °C; $f_{XTAL}$ = 10 MHz; all currents flowing into the IC are positive: see Table note 1; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Temperature** | | | | | | |
| $T_{amb}$ | ambient temperature | | –25 | - | +85 | °C |
| **Supplies** | | | | | | |
| $V_{DD}$ | supply voltage | | 2.7 | - | 6.5 | V |
| $V_{DDP}$ | DC-to-DC converter supply voltage | $V_{CC}$ = 5 V; $\|I_{CC}\|$ < 80 mA | 4.0 | 5.0 | 6.5 | V |
| | | $V_{CC}$ = 5 V; $\|I_{CC}\|$ < 20 mA | 3.0 | - | 6.5 | V |
| $I_{DD}$ | supply current | card inactive | - | - | 1.2 | mA |
| | | card active; $f_{CLK} = f_{XTAL}$; $C_L$ = 30 pF | - | - | 1.5 | mA |
| $I_{DDP}$ | DC-to-DC converter supply current | inactive mode | - | - | 0.1 | mA |
| | | active mode; $f_{CLK} = f_{XTAL}$; $C_L$ = 30 pF; $\|I_{CC}\|$ = 0 | - | - | 10 | mA |
| | | $V_{CC}$ = 5 V; $\|I_{CC}\|$ = 80 mA | - | - | 200 | mA |
| | | $V_{CC}$ = 3 V; $\|I_{CC}\|$ = 65 mA | - | - | 100 | mA |
| $V_{th2}$ | falling threshold voltage on $V_{DD}$ | no external resistors at pin PORADJ; $V_{DD}$ level falling | 2.35 | 2.45 | 2.55 | V |
| $V_{hys2}$ | hysteresis of threshold voltage $V_{th2}$ | no external resistors at pin PORADJ | 50 | 100 | 150 | mV |
| **Pin PORADJ**[2] | | | | | | |
| $V_{th(ext)(rise)}$ | external rising threshold voltage on $V_{DD}$ | external resistor bridge at pin PORADJ; $V_{DD}$ level rising | 1.240 | 1.28 | 1.310 | V |
| $V_{th(ext)(fall)}$ | external falling threshold voltage on $V_{DD}$ | external resistor bridge at pin PORADJ; $V_{DD}$ level falling | 1.190 | 1.22 | 1.26 | V |
| $V_{hys(ext)}$ | hysteresis of threshold voltage $Vt_{h(ext)}$ | external resistor bridge at pin PORADJ | 30 | 60 | 90 | mV |
| $\Delta V_{hys(ext)}$ | hysteresis of threshold voltage $V_{th(ext)}$ variation with temperature | external resistor bridge at pin PORADJ | - | - | 0.25 | mV/K |
| $t_w$ | width of internal Power-on reset pulse | no external resistors at pin PORADJ | 4 | 8 | 12 | ms |
| | | external resistor bridge at pin PORADJ | 8 | 16 | 24 | ms |
| $I_{L(PORADJ)}$ | leakage current on pin PORADJ | VPORADJ < 0.5 V | –0.1 | 4 | 10 | µA |
| | | VPORADJ > 1 V | –1 | - | +1 | µA |
| $P_{tot}$ | total power dissipation | continuous operation; $T_{amb}$ = –25 to +85 °C | - | - | 0.56 | W |
| **DC-to-DC converter** | | | | | | |
| $f_{CLK}$ | clock frequency | card active | 2.2 | - | 3.2 | MHz |
| $V_{th(vd-vf)}$ | threshold voltage for voltage doubler to change to voltage follower | 5 V card | 5.2 | 5.8 | 6.2 | V |
| | | 3 V card | 3.8 | 4.1 | 4.4 | V |

**Table 8. Characteristics** *...continued*

*$V_{DD}$ = 3.3 V; $V_{DDP}$ = 5 V; $T_{amb}$ = 25 °C; $f_{XTAL}$ = 10 MHz; all currents flowing into the IC are positive: see Table note 1; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{UP(av)}$ | output voltage on pin $V_{UP}$ (average value) | $V_{CC}$ = 5 V | 5.2 | 5.7 | 6.2 | V |
| | | $V_{CC}$ = 3 V; $V_{DDP}$ = 3.3 V | 3.5 | 3.9 | 4.3 | V |
| **Card supply voltage (pin $V_{CC}$)[3]** | | | | | | |
| $C_{VCC}$ | external capacitance on pin $V_{CC}$ | [4] | 80 | - | 400 | nF |
| $V_{CC}$ | card supply voltage (including ripple voltage) | 5 V card | | | | |
| | | card inactive; $\|I_{CC}\|$ = 0 mA | −0.1 | 0 | +0.1 | V |
| | | card inactive; $\|I_{CC}\|$ = 1 mA | −0.1 | 0 | +0.3 | V |
| | | card active; $\|I_{CC}\|$ < 80 mA | 4.75 | 5.0 | 5.25 | V |
| | | card active; single current pulse, $I_p$ = −100 mA; $t_p$ = 2 ms | 4.65 | 5.0 | 5.25 | V |
| | | card active; current pulses, $I_p$ = 40 nAs | 4.65 | 5.0 | 5.25 | V |
| | | card active; current pulses, $I_p$ = 40 nAs with $\|I_{CC}\|$ < 200 mA; $t_p$ < 400 ns | 4.65 | 5.0 | 5.25 | V |
| | | 3 V card | | | | |
| | | card inactive; $\|I_{CC}\|$ = 0 mA | −0.1 | 0 | +0.1 | V |
| | | card inactive; $\|I_{CC}\|$ = 1 mA | −0.1 | 0 | +0.3 | V |
| | | card active; $\|I_{CC}\|$ < 65 mA | 2.85 | 3.0 | 3.15 | V |
| | | card active; single current pulse, $I_p$ = −100 mA; $t_p$ = 2 ms | 2.76 | 3.0 | 3.20 | V |
| | | card active; current pulses, $I_p$ = 40 nAs | 2.76 | 3.0 | 3.20 | V |
| | | card active; current pulses, $I_p$ = 40 nAs with $\|I_{CC}\|$ < 200 mA; $t_p$ < 400 ns | 2.76 | 3.0 | 3.20 | V |
| $V_{CC(ripple)(p-p)}$ | ripple voltage on $V_{CC}$ (peak to peak value) | $f_{ripple}$ = 20 kHz to 200 MHz | - | - | 350 | mV |
| $\|I_{CC}\|$ | card supply current | $V_{CC}$ = 0 to 5 V | - | - | 80 | mA |
| | | $V_{CC}$ = 0 to 3 V | - | - | 65 | mA |
| | | $V_{CC}$ short-circuit to GND | 100 | 120 | 150 | mA |
| SR | slew rate | slew up or down | 0.08 | 0.15 | 0.22 | V/µs |
| **Crystal oscillator (pins XTAL1 and XTAL2)** | | | | | | |
| $C_{XTAL1}$, $C_{XTAL2}$ | external capacitance on pins XTAL1 and XTAL2 | depends on type of crystal or resonator used | - | - | 15 | pF |
| $f_{XTAL}$ | crystal frequency | | 2 | - | 26 | MHz |
| $f_{XTAL1}$ | frequency applied on pin XTAL1 | | 0 | - | 26 | MHz |
| $V_{IL}$ | LOW-level input voltage on pin XTAL1 | | −0.3 | - | +0.3$V_{DD}$ | V |

**Table 8. Characteristics** *...continued*

*$V_{DD}$ = 3.3 V; $V_{DDP}$ = 5 V; $T_{amb}$ = 25 °C; $f_{XTAL}$ = 10 MHz; all currents flowing into the IC are positive: see Table note 1; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | HIGH-level input voltage on pin XTAL1 | | $0.7V_{DD}$ | - | $V_{DD}$ + 0.3 | V |
| **Data lines (pins I/O, I/OUC, AUX1, AUX2, AUX1UC and AUX2UC)** | | | | | | |
| $t_{d(I/O-I/OUC)}$, $t_{d(I/OUC-I/O)}$ | I/O to I/OUC, I/OUC to I/O falling edge delay | | - | - | 200 | ns |
| $t_{pu}$ | active pull-up pulse width | | - | - | 100 | ns |
| $f_{I/O(max)}$ | maximum frequency on data lines | | - | - | 1 | MHz |
| $C_i$ | input capacitance on data lines | | - | - | 10 | pF |
| **Data lines to card reader (pins I/O, AUX1 and AUX2; with integrated 11 kΩ pull-up resistors to $V_{CC}$)** | | | | | | |
| $V_{o(inactive)}$ | output voltage | inactive mode | | | | |
| | | no load | 0 | - | 0.1 | V |
| | | $I_{o(inactive)}$ = 1 mA | - | - | 0.3 | V |
| $I_{o(inactive)}$ | output current | inactive mode; pin grounded | - | - | −1 | mA |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 1 mA | 0 | - | 0.3 | V |
| | | $I_{OL} \geq$ 15 mA | $V_{CC}$ − 0.4 | - | $V_{CC}$ | V |
| $V_{OH}$ | HIGH-level output voltage | no DC load | $0.9V_{CC}$ | - | $V_{CC}$ + 0.1 | V |
| | | 5 V and 3 V cards; $I_{OH}$ < −40 µA | $0.75V_{CC}$ | - | $V_{CC}$ + 0.1 | V |
| | | $\|I_{OH}\| \geq$ 10 mA | 0 | - | 0.4 | V |
| $V_{IL}$ | LOW-level input voltage | | 0.3 | - | 0.8 | V |
| $V_{IH}$ | HIGH-level input voltage | | 1.5 | - | $V_{CC}$ + 0.3 | V |
| $\|I_{IL}\|$ | LOW-level input current | $V_{IL}$ = 0 V | - | - | 600 | µA |
| $\|I_{LIH}\|$ | HIGH-level input leakage current | $V_{IH} = V_{CC}$ | - | - | 10 | µA |
| $t_{t(DI)}$ | data input transition time | $V_{IL(max)}$ to $V_{IH(min)}$ | - | - | 1.2 | µs |
| $t_{t(DO)}$ | data output transition time | $V_o$ = 0 to $V_{CC}$; $C_L \leq$ 80 pF; 10% to 90% | - | - | 0.1 | µs |
| $R_{pu}$ | integrated pull-up resistor | pull-up resistor to $V_{DD}$ | 9 | 11 | 13 | kΩ |
| $I_{pu}$ | current when pull-up active | $V_{OH} = 0.9V_{CC}$; C = 80 pF | −1 | - | - | mA |
| **Data lines to microcontroller (pins I/OUC, AUX1UC and AUX2UC; with integrated 11 kΩ pull-up resistors to $V_{DD}$)** | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 1 mA | 0 | - | 0.3 | V |
| $V_{OH}$ | HIGH-level output voltage | no DC load | $0.9V_{DD}$ | - | $V_{DD}$ + 0.1 | V |
| | | 5 V and 3 V cards; $I_{OH}$ < −40 µA | $0.75V_{DD}$ | - | $V_{DD}$ + 0.1 | V |
| $V_{IL}$ | LOW-level input voltage | | −0.3 | - | $+0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DD}$ | - | $V_{DD}$ + 0.3 | V |
| $\|I_{LIH}\|$ | HIGH-level input leakage current | $V_{IH} = V_{DD}$ | - | - | 10 | µA |
| $\|I_{IL}\|$ | LOW-level input current | $V_{IL}$ = 0 V | - | - | 600 | µA |
| $t_{t(DI)}$ | data input transition time | $V_{IL(max)}$ to $V_{IH(min)}$ | - | - | 1.2 | µs |

**Table 8. Characteristics** *...continued*

*$V_{DD}$ = 3.3 V; $V_{DDP}$ = 5 V; $T_{amb}$ = 25 °C; $f_{XTAL}$ = 10 MHz; all currents flowing into the IC are positive: see Table note 1; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{t(DO)}$ | data output transition time | $V_o$ = 0 to $V_{DD}$; $C_L$ < 30 pF; 10% to 90% | - | - | 0.1 | µs |
| $R_{pu}$ | integrated pull-up resistor | pull-up resistor to $V_{DD}$ | 9 | 11 | 13 | kΩ |
| $I_{pu}$ | current when pull-up active | $V_{OH}$ = 0.9$V_{DD}$; C = 30 pF | –1 | - | - | mA |
| **Internal oscillator** | | | | | | |
| $f_{OSC(int)}$ | frequency of internal oscillator | inactive mode | 55 | 140 | 200 | kHz |
| | | active mode | 2.2 | 2.7 | 3.2 | MHz |
| **Reset output to card reader (pin RST)** | | | | | | |
| $V_{o(inactive)}$ | output voltage | inactive mode | | | | |
| | | no load | 0 | - | 0.1 | V |
| | | $I_{o(inactive)}$ = 1 mA | 0 | - | 0.3 | V |
| $I_{o(inactive)}$ | output current | inactive mode; pin grounded | - | - | –1 | mA |
| $t_{d(RSTIN-RST)}$ | RSTIN to RST delay | RST enabled | - | - | 2 | µs |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 200 µA | 0 | - | 0.2 | V |
| | | $I_{OL}$ = 20 mA (current limit) | $V_{CC}$ – 0.4 | - | $V_{CC}$ | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = –200 µA | 0.9$V_{CC}$ | - | $V_{CC}$ | V |
| | | $I_{OH}$ = –20 mA (current limit) | 0 | - | 0.4 | V |
| $t_r$ | rise time | $C_L$ = 100 pF; $V_{CC}$ = 5 V or 3 V | - | - | 0.1 | µs |
| $t_f$ | fall time | $C_L$ = 100 pF; $V_{CC}$ = 5 V or 3 V | - | - | 0.1 | µs |
| **Clock output to card reader (pin CLK)** | | | | | | |
| $V_{o(inactive)}$ | output voltage | inactive mode | | | | |
| | | no load | 0 | - | 0.1 | V |
| | | $I_{o(inactive)}$ = 1 mA | 0 | - | 0.3 | V |
| $I_{o(inactive)}$ | output current | CLK inactive; pin grounded | 0 | - | –1 | mA |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 200 µA | 0 | - | 0.3 | V |
| | | $I_{OL}$ = 70 mA (current limit) | $V_{CC}$ – 0.4 | - | $V_{CC}$ | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = –200 µA | 0.9$V_{CC}$ | - | $V_{CC}$ | V |
| | | $I_{OH}$ = –70 mA (current limit) | 0 | - | 0.4 | V |
| $t_r$ | rise time | $C_L$ = 30 pF [5] | - | - | 16 | ns |
| $t_f$ | fall time | $C_L$ = 30 pF [5] | - | - | 16 | ns |
| δ | duty factor (except for $f_{XTAL}$) | $C_L$ = 30 pF [5] | 45 | - | 55 | % |
| SR | slew rate | slew up or down; $C_L$ = 30 pF | 0.2 | - | - | V/ns |
| **Control inputs (pins CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$, RSTIN and 5V/$\overline{\text{3V}}$)[6]** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | –0.3 | - | +0.3$V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | 0.7$V_{DD}$ | - | $V_{DD}$ + 0.3 | V |
| $\lvert I_{LIL} \rvert$ | LOW-level input leakage current | 0 < $V_{IL}$ < $V_{DD}$ | - | - | 1 | µA |
| $\lvert I_{LIH} \rvert$ | HIGH-level input leakage current | 0 < $V_{IH}$ < $V_{DD}$ | - | - | 1 | µA |

**Table 8. Characteristics** *...continued*

*$V_{DD}$ = 3.3 V; $V_{DDP}$ = 5 V; $T_{amb}$ = 25 °C; $f_{XTAL}$ = 10 MHz; all currents flowing into the IC are positive: see Table note 1; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Card presence inputs (pins PRES and $\overline{PRES}$)[7]** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | −0.3 | - | $+0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DD}$ | - | $V_{DD}$ + 0.3 | V |
| $\lvert I_{LIL}\rvert$ | LOW-level input leakage current | $0 < V_{IL} < V_{DD}$ | - | - | 5 | µA |
| $\lvert I_{LIH}\rvert$ | HIGH-level input leakage current | $0 < V_{IH} < V_{DD}$ | - | - | 5 | µA |
| **Interrupt output (pin $\overline{OFF}$; NMOS drain with integrated 20 kΩ pull-up resistor to $V_{DD}$)** | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 2 mA | 0 | - | 0.3 | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = −15 µA | $0.75V_{DD}$ | - | - | V |
| $R_{pu}$ | integrated pull-up resistor | 20 kΩ pull-up resistor to $V_{DD}$ | 16 | 20 | 24 | kΩ |
| **Protection and limitation** | | | | | | |
| $\lvert I_{CC(sd)}\rvert$ | shutdown and limitation current pin $V_{CC}$ | | - | 130 | 150 | mA |
| $I_{I/O(lim)}$ | limitation current pins I/O, AUX1 and AUX2 | | −15 | - | +15 | mA |
| $I_{CLK(lim)}$ | limitation current pin CLK | | −70 | - | +70 | mA |
| $I_{RST(lim)}$ | limitation current pin RST | | −20 | - | +20 | mA |
| $T_{sd}$ | shut-down temperature | | - | 150 | - | °C |
| **Timing** | | | | | | |
| $t_{act}$ | activation time | see Figure 7 | 50 | - | 220 | µs |
| $t_{de}$ | deactivation time | see Figure 8 | 50 | 80 | 100 | µs |
| $t_3$ | start of the window for sending CLK to the card | see Figure 7 | 50 | - | 130 | µs |
| $t_5$ | end of the window for sending CLK to the card | see Figure 7 | 140 | - | 220 | µs |
| $t_{debounce}$ | debounce time pins PRES and $\overline{PRES}$ | see Figure 10 | 5 | 8 | 11 | ms |

[1] All parameters remain within limits but are tested only statistically for the temperature range. When a parameter is specified as a function of $V_{DD}$ or $V_{CC}$ it means their actual value at the moment of measurement.

[2] If no external bridge is used then, to avoid any disturbance, it is recommended to connect pin 18 to ground. Pin 18 is not connected in the TDA8024AT.

[3] To meet these specifications, pin $V_{CC}$ should be decoupled to CGND using two ceramic multilayer capacitors of low ESR both with values of 100 nF, or one 100 nF and one 220 nF (see Figure 13).

[4] Permitted capacitor values are 100 nF, or 100 nF + 100 nF, or 220 nF, or 220 nF + 100 nF, or 330 nF.

[5] Transition time and duty factor definitions are shown in Figure 12; $\delta = \frac{t_1}{t_1 + t_2}$

[6] Pin $\overline{CMDVCC}$ is active LOW; pin RSTIN is active HIGH; for CLKDIV1 and CLKDIV2 functions see Table 1.

[7] Pin $\overline{PRES}$ is active LOW; pin PRES is active HIGH; PRES has an integrated 1.25 µA current source to GND (PRES to $V_{DD}$); the card is considered present if at least one of the inputs $\overline{PRES}$ or PRES is active.

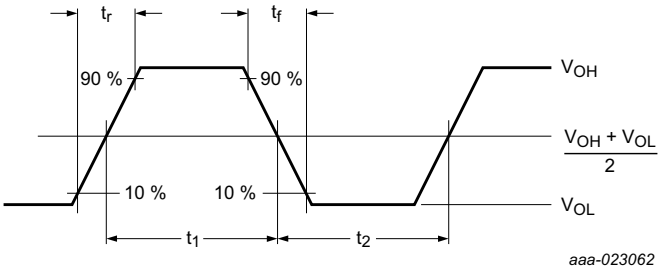



**Fig 12. Definition of output and input transition times**

## 12. Application information

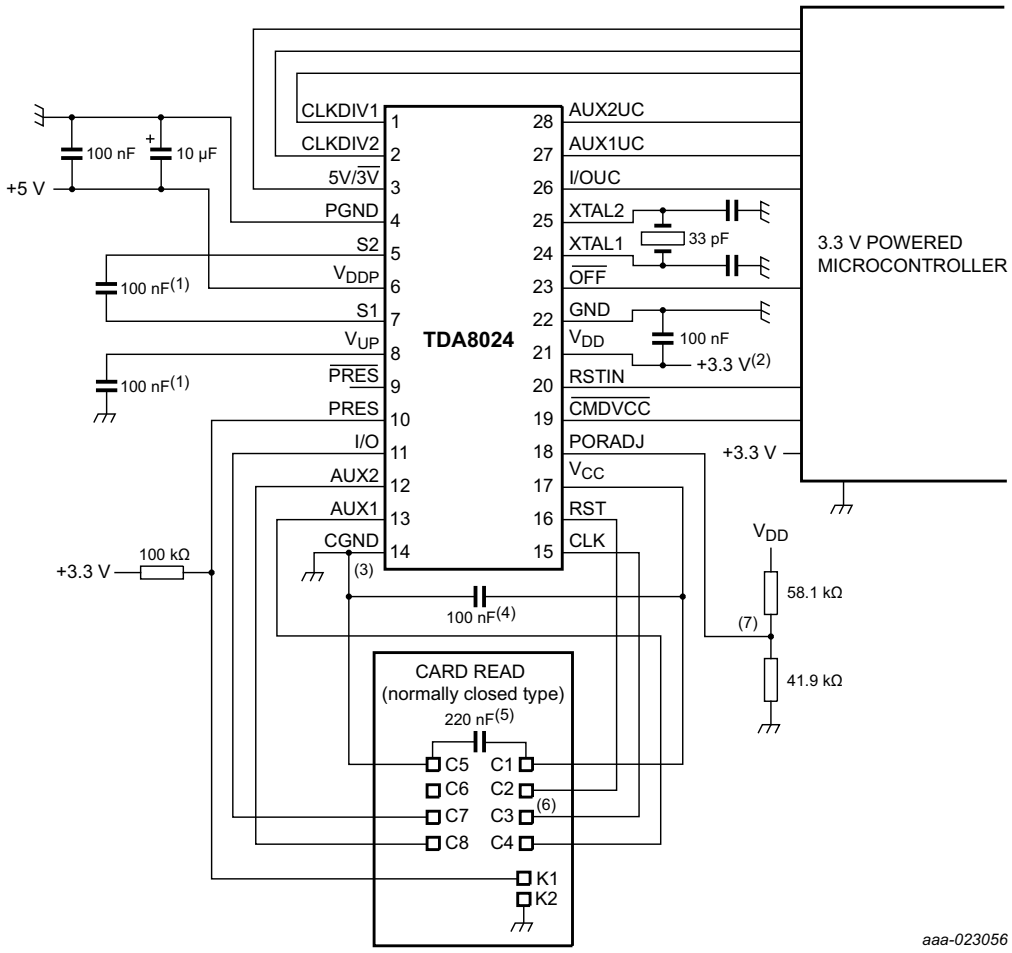
Performance can be affected by the layout of the application. For example, an additional cross-capacitance of 1 pF between card reader contacts C2 and C3 or C2 and C7 can cause contact C2 to be polluted with high frequency noise from C3 (or C7). In this case, include a 100 pF capacitor between contacts C2 and CGND.

Application recommendations:

- Ensure there is ample ground area around the TDA8024 and the connector; place the TDA8024 very near to the connector; decouple the $V_{DD}$ and $V_{DDP}$ lines (these lines are best positioned under the connector)
- The TDA8024 and the microcontroller must use the same $V_{DD}$ supply. Pins CLKDIV1, CLKDIV2, RSTIN, PRES, $\overline{\text{PRES}}$, AUX1UC, I/OUC, AUX2UC, 5V/3V, $\overline{\text{CMDVCC}}$, and $\overline{\text{OFF}}$ are referred to $V_{DD}$; if pin XTAL1 is to be driven by an external clock, also refer this pin to $V_{DD}$
- Track C3 should be placed as far as possible from the other tracks
- The track connecting CGND to C5 should be straight (the two capacitors on C1 should be connected to this ground track)
- Avoid ground loops between CGND, PGND and GND
- Decouple $V_{DDP}$ and $V_{DD}$ separately; if the two supplies are the same in the application, then they should be connected in star on the main track.

With all these layout precautions, noise should be kept to an acceptable level and jitter on C3 should be less than 100 ps.

Reference layouts are provided in *"Application note 10141"*, available on request.




(1) These capacitors must be of the low ESR-type and be placed near the IC (within 100 mm).

(2) TDA8024 and the microcontroller must use the same $V_{DD}$ supply.

(3) Make short, straight connections between CGND, C5 and the ground connection to the capacitor.

(4) Mount one low ESR-type 100 nF capacitor close to pin $V_{CC}$.

(5) Mount one low ESR-type 100 or 220 nF capacitor close to C1 contact (less than 100 mm from it).

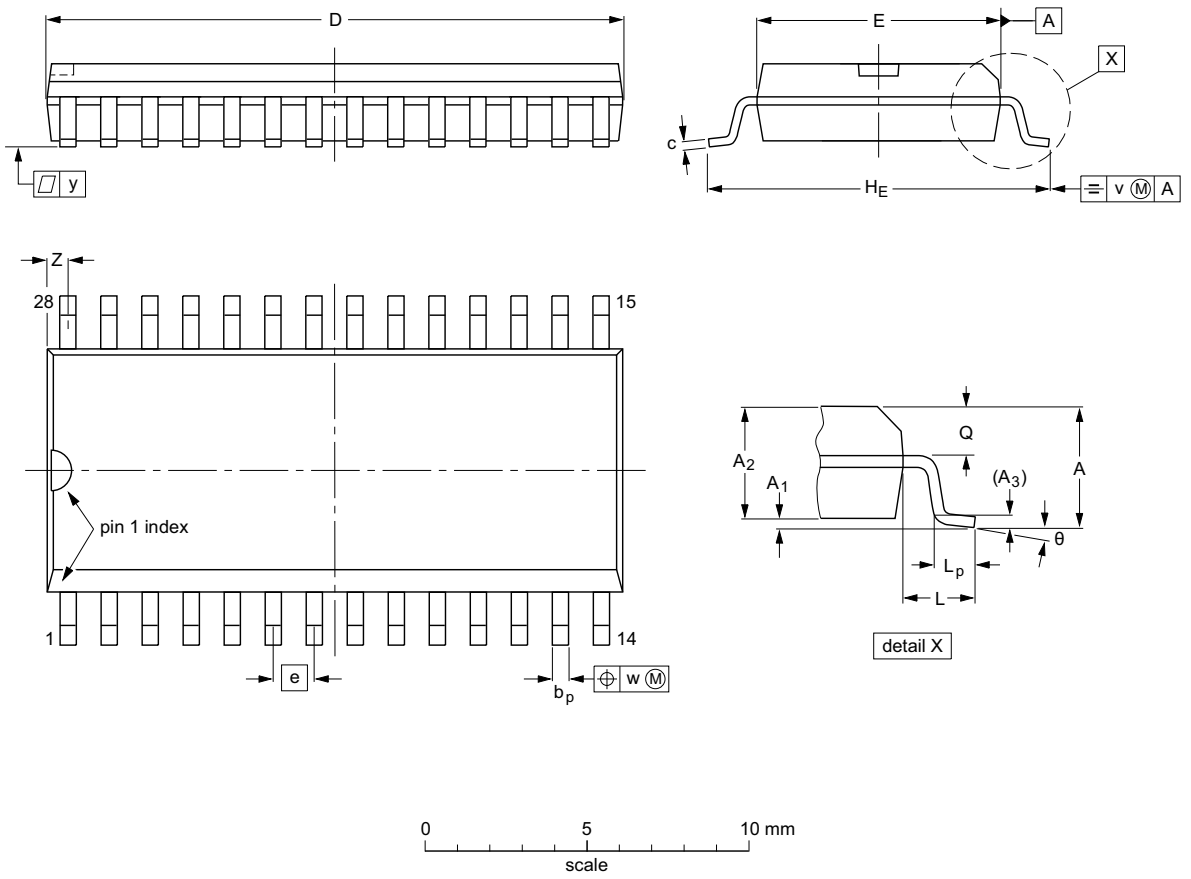
(6) The connection to C3 should be routed as far from C2, C7, C4 and C8 and, if possible, surrounded by grounded tracks.

(7) Optional resistor bridge for changing the threshold of $V_{DD}$. If this bridge is not required pin 18 should be connected to ground; see Section 8.2.2. Pin 18 is not connected in the TDA8024AT.

**Fig 13. Application diagram**

# 13. Package outline

**SO28: plastic small outline package; 28 leads; body width 7.5 mm** **SOT136-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.3<br>0.1 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 18.1<br>17.7 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | 8°<br>0° |
| inches | 0.1 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.71<br>0.69 | 0.30<br>0.29 | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

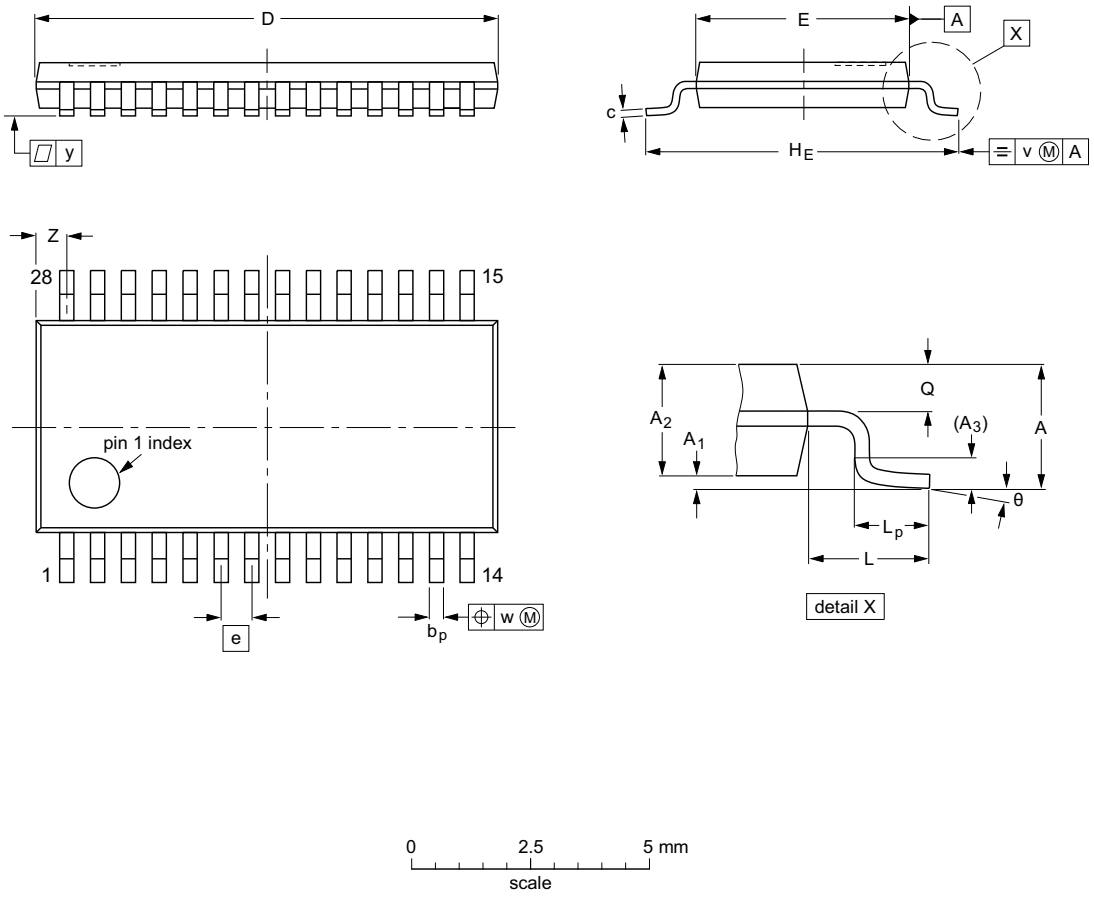
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT136-1 | 075E06 | MS-013 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 14. Package outline SOT136-1 (SO28)**

**TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm** **SOT361-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 9.8<br>9.6 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.8<br>0.5 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT361-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 15. Package outline SOT361-1 (TSSOP28)**

# 14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 16) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

**Table 9. SnPb eutectic process (from J-STD-020D)**

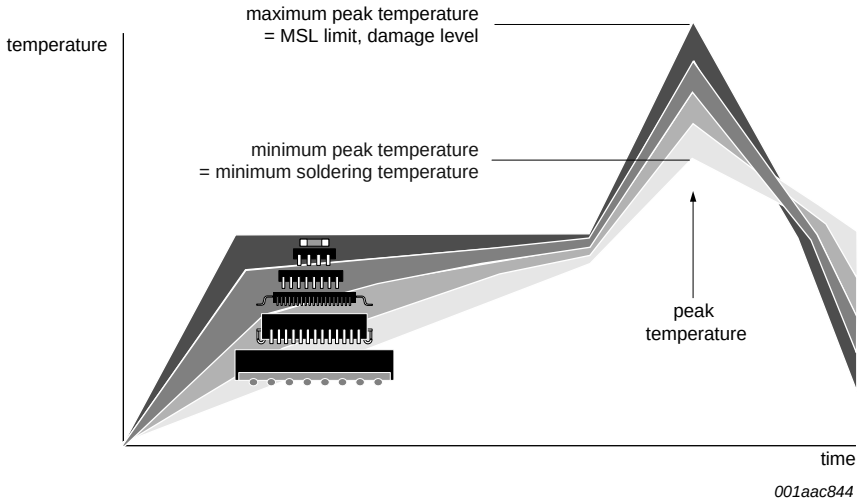
| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 10. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 16.




MSL: Moisture Sensitivity Level

**Fig 16. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

# 15. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| TDA8024 v.4.0 | 20160603 | Product data sheet | - | TDA8024_3 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Section 5 “Ordering information”: updated | | | |
| TDA8024_3 | 20040712 | Product specification | - | TDA8024_2 |
| TDA8024_2 | 20030819 | Product specification | - | - |

# 16. Legal information

## 16.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 16.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet —** A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification —** The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 16.3 Disclaimers

**Limited warranty and liability —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values —** Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale —** NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control —** This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Quick reference data —** The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Non-automotive qualified products —** Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations —** A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

### 16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 17. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

## 18. Contents





For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 3 June 2016**
**Document identifier: TDA8024**