# EV1924A-R-00A

## 100V, 4A, Half-Bridge Gate Driver Evaluation Board

## DESCRIPTION

The EV1924A-R-00A is an evaluation board for the MP1924A, a high-frequency, half-bridge gate driver. Its high-side and low-side driver channels are independently controlled, and are matched with a time delay of less than 5ns.

The board is configured as a buck converter. The INH and INL signals are independent of each other. Complementary PWMs with proper dead time should be implemented for INH and INL.

## FEATURES

- 115V Bootstrap Voltage Range
- On-Chip Bootstrap Diode
- Quiescent Current Below 150µA
- Typical Propagation Delay of 20ns
- Gate Driver Matching of Less than 5ns
- UVLO for Both High-Side and Low-Side Gate Drivers
- TTL-Compatible Input
- Available in QFN-10 (4mmx4mm) and SOIC-8 Packages

## ELECTRICAL SPECIFICATIONS

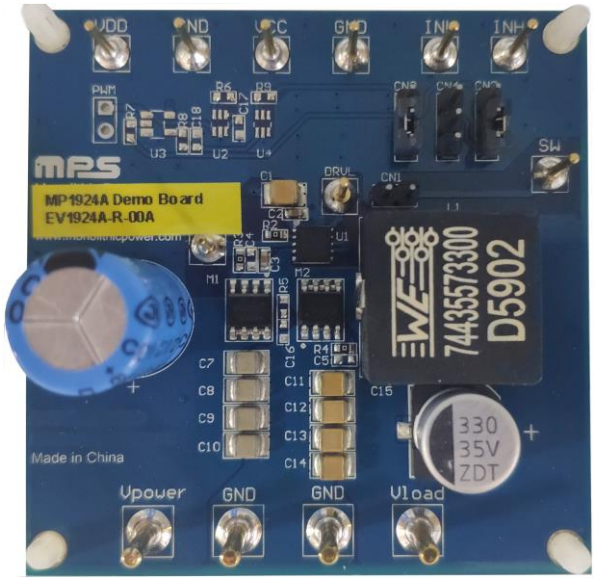
| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Driver power supply voltage | $V_{DD}$ | 8 to 15 | V |
| Input power supply voltage | $V_{IN}$ | 0 to 100 | V |

## APPLICATIONS

- Motor Drivers
- Telecom Half-Bridge Power Supplies
- Avionics DC/DC Converters



## EV1924A-R-00A EVALUATION BOARD




**(LxWxH) 6.35cmx6.35cmx1cm**

| Board Number | MPS IC Number |
|---|---|
| EV1924A-R-00A | MP1924AHR |

## QUICK START GUIDE

1. Preset the driver power supply voltage $V_{DD}$ between 8V and 15V.
2. Preset the input power supply voltage $V_{POWER}$ between 0V and 100V.
3. Attach a complementary PWM with a proper dead time to CN4.
4. Attach the driver power supply to:
   a. Positive (+): VDD
   b. Negative (-): GND
5. Attach the input power supply to:
   a. Positive (+): $V_{POWER}$
   b. Negative (-): GND
6. Attach the load to:
   a. Positive (+): $V_{LOAD}$
   b. Negative (-): GND
7. Turn the driver power supply on.

   Check the INH, INL, DRVH, and DRVL signals. Ensure that a sufficient dead time for DRVH and DRVL has been established before continuing to step 8.
8. Turn the input power supply on.
9. Turn the load on, then check output voltage and current.
10. To turn the system off, follow the steps below:
    a. Turn the load off.
    b. Turn $V_{POWER}$ off.
    c. Turn $V_{DD}$ off.

# EVALUATION BOARD SCHEMATIC

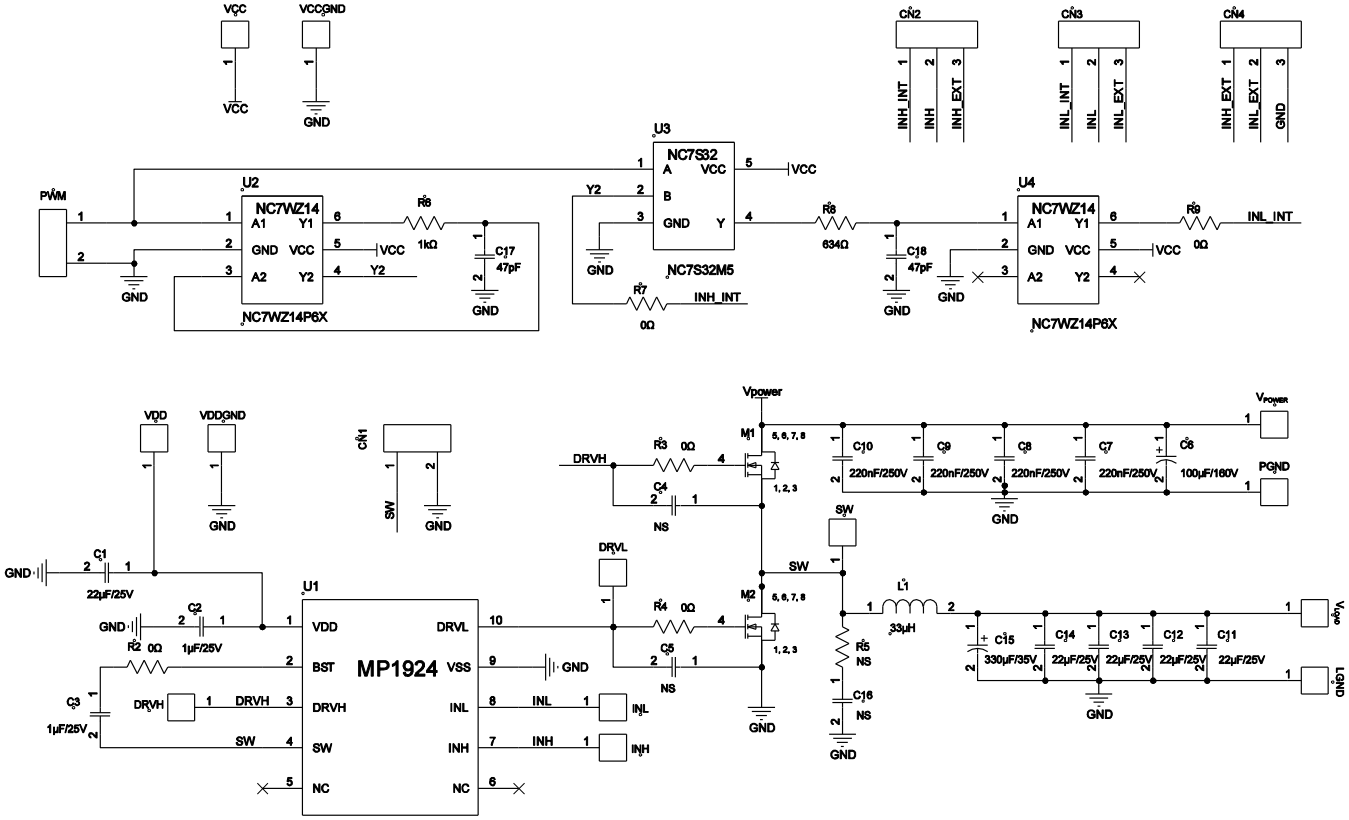



**Figure 1: Evaluation Board Schematic**

## EV1924A-R-00A BILL OF MATERIALS

| Qty | Ref | Value | Description | Package | Manufacturer | Manufacturer P/N |
|---|---|---|---|---|---|---|
| 5 | C1, C11, C12, C13, C14 | 22µF/ 25V | Ceramic capacitor, 25V, X5R | 1210 | Murata | GRM32ER71E226KE15L |
| 2 | C2, C3 | 1µF/ 25V | Ceramic capacitor, 25V, X5R | 0603 | TDK | C1608X5R1E105K |
| 3 | C4, C5, C16 | NS | | | | |
| 1 | C6 | 100µF/ 160V | Electrolytic capacitor, 160V | DIP | Jianghai | CD110-160V100 |
| 4 | C7, C8, C9, C10 | 220nF/ 250V | Ceramic capacitor, 250V, X7R | 1210 | Murata | GRM32DR72E224KW01L |
| 1 | C15 | 330µF/ 35V | Electrolytic capacitor, 35V | SMD | Jianghai | VZ1-35V330 |
| 1 | L1 | 33µH | Inductor, 33µH, 8.5A | SMD | Wurth | 74435573300 |
| 1 | R5 | NS | | | | |
| 3 | R2, R3, R4 | 0Ω | Film resistor, 5% | 0603 | Yageo | RC0603JR-070RL |
| 2 | M1, M2 | AM4490N | N-channel MOSFET | PowerPAK SO-8 | Analog Power | AM4490N |
| 1 | U1 | MP1924A | Integrated gate driver | QFN-10 (4mmx4mm) | MPS | MP1924AHR |
| 4 | $V_{POWER}$, $V_{LOAD}$, GNDx2 | | 2mm needle | | | |
| 9 | VDD, GND, VCC, GND, INL, INH, DRVH, DRVL, SW | | 1mm needle | | | |

## PCB LAYOUT

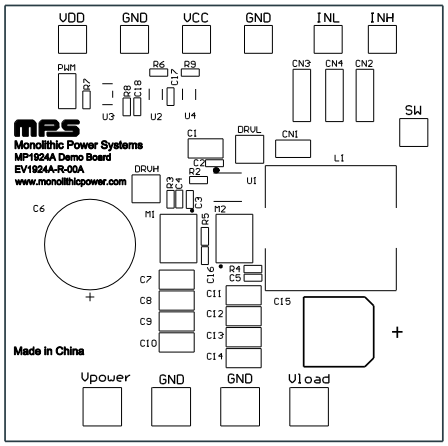



Figure 2: Top Silkscreen Layer

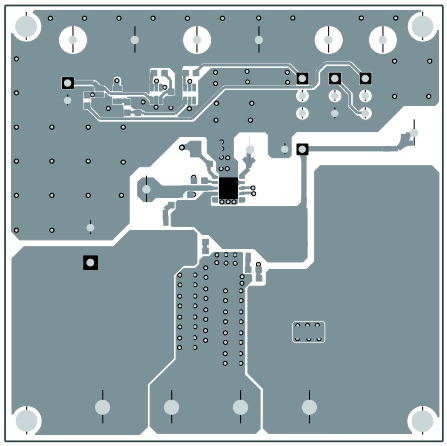


Figure 3: Top Layer

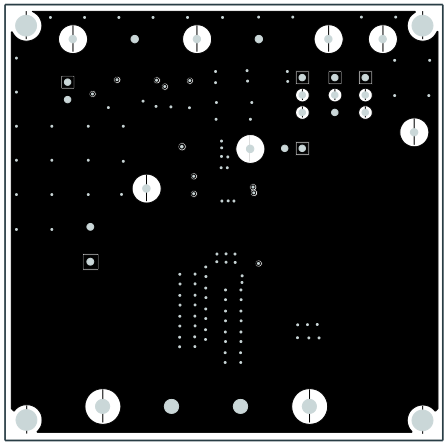


Figure 4: Mid-Layer 1

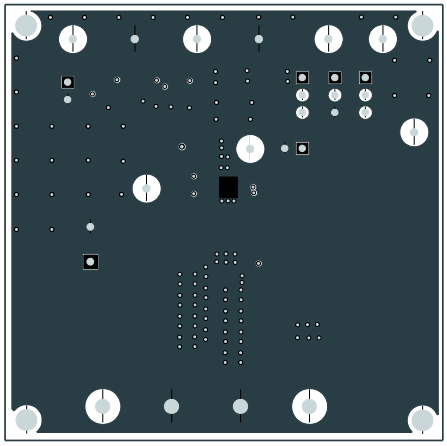


Figure 5: Mid-Layer 2

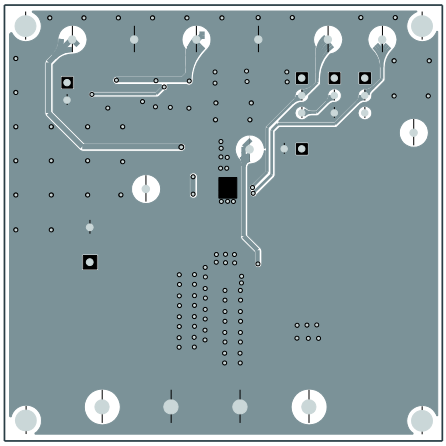


Figure 6: Bottom Layer

## Revision History

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 7/22/2020 | Initial Release | - |