A Product Line of Diodes Incorporated

PI6C49S1504T

High Performance Selectable 1:4 Differential Fanout Buffer

Features

- 4 differential outputs with 2 banks
- User-configurable output signaling standard for each bank: LVDS or LVPECL or HCSL
- LVCMOS reference output up to 200MHz
- Up to 1.5GHz output frequency for differential outputs
- Ultra-low additive phase jitter: < 0.03ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Selectable reference inputs support either single-ended or differential or Xtal
- Low skew between outputs within banks (<40ps)
- Low delay from input to output (Tpd typ. < 1.5ns)
- Separate input output supply voltage for level shifting
- 2.5V / 3.3V power supply
- Industrial temperature support
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 32-pin, TQFN (ZH)

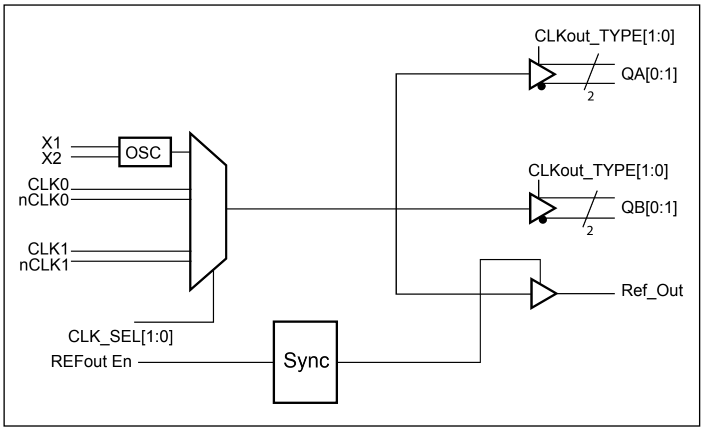
Description

The PI6C49S1504T is a high-performance fanout buffer device which supports up to 1.5GHz frequency. This device is ideal for systems that need to distribute low-jitter clock signals to multiple destinations.

Applications

- Networking Systems, including Switches and Routers
- High-Frequency Backplane-based Computing and Telecom Platforms

Block Diagram

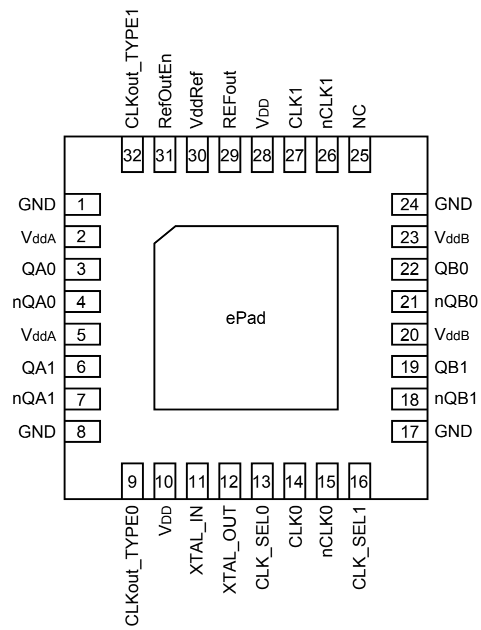


Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

® Diodes Incorporated

Pin Configuration



Pin Description

Pin #	Pin Name	Type	Description
1, 8, 17, 24	GND	Power	Negative power supply
25	NC	-	Not Connect
2, 5	V_{ddA}	Power	Power supply for Bank A Output buffers. V_{ddA} operates from 3.3V or 2.5V
13	CLK_SEL0	Input	Clock input source selection pin
16	CLK_SEL1	Input	Clock input source selection pin
14, 15	CLK0 nCLK0	Input	Differential clock input
27, 26	CLK1 nCLK1	Input	Differential clock input
11	XTAL_In	Input	Input for crystal, XO, or single ended clock
12	XTAL_Out	Output	Output for crystal. Leave Xtal_Out floating if Xtal_In is driven by a single ended clock
10, 28	V_{DD}	Power	Power supply for core
18, 19	nQB1 QB1	Output	Differential output clock
21, 22	nQB0 QB0	Output	Differential output clock

© Diodes Incorporated

Pin Description Cont.

Pin #	Pin Name	Type	Description
29	Ref_Out	Output	Reference output clock
7, 6	nQA1 QA1	Output	Differential output clock
4, 3	nQA0 QA0	Output	Differential output clock
9	CLKout_TYPE0	Input	Bank A and Bank B output buffer type selection pins
32	CLKout_TYPE1	Input	Bank A and Bank B output buffer type selection pins
ePad	ePad	GND	Connect to the PCB ground
20, 23	V_{ddB}	Power	Power supply for Bank B Output buffers. V_{ddB} operates from 3.3 V or 2.5V
30	VddRef	Power	Power supply for reference clock output
31	RefOutEn	Input	REFout enable input

© Diodes Incorporated

Function Table

Table 1: Input Selection

CLK_SEL1	CLK_SEL0	Selected Input
0	0	CLK0, nCLK0
0	1	CLK1, nCLK1
1	X	XTAL_In

Table 2: Differential Output Buffer Type Selection

CLKout_TYPE1	CLKout_TYPE0	CLKoutX Buffer Type (Bank A and B)
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	Disabled (Hi-Z)

Table 3: Reference Output Enable

REFout_EN	REFout STATE
0	Disabled (Hi-Z)
1	Enabled

Table 4: CLKx Input vs. Output States

State of Selected Input Clock	State of Enabled Outputs
CLKx and nCLKx Inputs Floating	Logic Low
CLKx and nCLKx Inputs Shorted Together	Not Supported. Output is Undefined
CLKx Logic Low	Logic Low
CLKx Logic High	Logic High

© Diodes Incorporated

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature..-55 to +150°C
Supply Voltage to Ground Potential (V_{DD}, V_{DDO})... -0.5 to +4.6V
Inputs (Referenced to GND) .... -0.5 to V_{DD}+0.5V
Clock Output (Referenced to GND)................. -0.5 to V_{DD}+0.5V
Latch up 200mA
ESD Protection (Input) ....2000V min (HBM)
Junction Temperature .... 150 °C max

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage		2.375		3.465	V
V_{DDO}	Output Supply Voltage	$V_{DDO} \le V_{DD}$	2.375		3.465	V
I_{DD}	Core Power Supply Current			90	120	mA
I_{DDO}	Output Power Supply Current	All LVPECL outputs unloaded		150	190	mA
		All LVDS outputs loaded		110	130	mA
		All HCSL outputs loaded		95		mA
T_A	Ambient Operating Temperature(1)		-40		85	°C
T_B	PCB Operating Temperature(1)		-40		105	°C

Note:
1. Either T_A or T_B used as operating condition

DC Electrical Specifications - Differential Inputs

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_{IH}	Input High current	Input = V_{DD}			150	uA
I_{IL}	Input Low current	Input = GND	-150			uA
C_{IN}	Input capacitance			3		PF
V_{IH}	Input high voltage				V_{DD}+0.3	V
V_{IL}	Input low voltage		-0.3			V
V_{ID}	Input Differential Amplitude PK-PK		0.15		1.3	V
V_{CM}	Common model input voltage		0.25		V_{DD}-1.2	V
ISO_{MUX}	MUX isolation			-89		dBc

DC Electrical Specifications - LVCMOS Inputs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High current	Input = V_{DD}			150	uA
I_{IL}	Input Low current	Input = GND	-150			uA
V_{IH}	Input high voltage	V_{DD}=3.3V	2.0		V_{DD}+0.3	V
V_{IL}	Input low voltage	V_{DD}=3.3V	-0.3		0.8	V
V_{IH}	Input high voltage	V_{DD}=2.5V	1.7		V_{DD}+0.3	V
V_{IL}	Input low voltage	V_{DD}=2.5V	-0.3		0.7	V

DC Electrical Specifications- LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage		V_{DDO}-1.4		V_{DDO}-0.9	V
V_{OL}	Output Low voltage		V_{DDO}-2.2		V_{DDO}-1.7	V

DC Electrical Specifications- LVDS Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage		1.4	1.5	1.6	V
V_{OL}	Output Low voltage		1	1.1	1.25	V
Vocm	Output commode voltage		1.2	1.3	1.45	V
DVocm	Change in Vocm between completely output states				50	mV
Ro	Output impedance		85		140	W

DC Electrical Specifications – HCSL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage	2.5V	660	725	850	mV
		3.3V	700	850	900	mV
V_{OL}	Output Low voltage		-150		150	mV

DC Electrical Specifications – LVCMOS Output

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage	V_{DDO}=3.3V +/-5%, I_{OH} = -8mA	2.3			V
		V_{DDO}=2.5V +/- 5%, I_{OH} = -8mA	1.5			V
V_{OL}	Output Low voltage	V_{DDO}=3.3V +/-5%, I_{OL} = 8mA			0.5	V
		V_{DDO}=2.5V +/- 5%, I_{OL} = 8mA			0.4	V
V_{OH}	Output High voltage	V_{DDO}=3.3V +/-5%, I_{OH} = -24mA	2.1			V
		V_{DDO}=2.5V +/- 5%, I_{OH} = -16mA	1.5			V
V_{OL}	Output Low voltage	V_{DDO}=3.3V +/-5%, I_{OL} = 24mA			1	V
		V_{DDO}=2.5V +/- 5%, I_{OL} = 16mA			0.8	V

AC Electrical Specifications – Differential Outputs

Parameter	Description	Conditions		Min.	Typ.	Max.	Units
F_{OUT}	Clock output frequency	LVPECL, LVDS				1500	MHz
		HCSL				250	
T_r	Output rise time	From 20% to 80%	LVPECL	100	150	300	ps
			LVDS	100	150	300	
			HCSL	300		700	
T_f	Output fall time	From 80% to 20%	LVPECL	100	150	300	ps
			LVDS	100	150	300	
			HCSL	300		700	
T_{ODC}	Output duty cycle	Frequency<650MHz, $V_{ID} \geq 400mV$	LVPECL, HCSL (<250MHz)	48		52	%
			LVDS	47		53	
		Frequency<1GHz, $V_{ID} \geq 400mV$	LVPECL	45		55	
			LVDS	45		55	
		Frequency<1.5GHz, $V_{ID} \geq 400mV$	LVDS	40		60	
		Frequency<1.5GHz, $V_{ID} \geq 400mV$	LVPECL	40		60	
V_{PP}	Output swing Single-ended	LVPECL outputs @ <1GHz		500		1100	mV
		LVPECL outputs @ >1GHz		400		1000	
		LVDS outputs @ <1GHz		250		600	
		LVDS outputs @ >1GHz		250		550	
T_j	Buffer additive jitter RMS	156.25MHz, 12kHz to 20MHz			0.02		ps
		156.25MHz, 10kHz to 1MHz			0.01		ps

AC Electrical Specifications – Differential Outputs Cont.

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{CROSS}	Absolute crossing voltage	HCSL		460		mV
DV_{CROSS}	Total variation of crossing voltage	HCSL			140	mV
T_{SK}	Output Skew	4 outputs devices, outputs in same bank, with same load, at DUT.		15	40	ps
T_{PD}	Propagation Delay	LVPECL, LVDS @ 3.3V, 100MHz		570		ps
		HCSL @ 3.3V, 100MHz		900		ps
T_{OD}	Valid to HiZ				200	ns
T_{OE}	HiZ to valid				200	ns
$T_{P2P\ Skew}$	Part to Part Skew(1)			80	120	ps

AC Electrical Specifications – CMOS

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Ref_Out frequency	XTAL input	10		50	MHz
		Reference input			200	MHz
T_j	Buffer additive jitter RMS	XTAL input		0.3		ps
		Reference input		0.03		ps
t_r/t_f	Rise time, Fall time	C_L = 5pF		0.8		ns
T_{ODC}	Output duty cycle	C_L = 5pF 3.3V, max test freq. 250MHz 2.5V, max test freq. 150MHz	45		55	%
t_{PD}	Propagation delay	3.3V, 25MHz		4500		ps
t_S	Setup time		300			ps
t_{SOD}	Clock edge to output disable	Ref_Out	2		4	cycles
t_{SOE}	Clock edge to output enable	Ref_Out	2		4	cycles
R_{IUT}	Output Impedance	V_{DDO} = 3.3V ± 5%		30		Ω
		V_{DDO} = 2.5V ± 5%		45		Ω

Notes:

1. This parameter is guaranteed by design

© Diodes Incorporated

Crystal Characteristics

Parameter	Min.	Typ.	Max.	Units
Mode of Oscillation	Fundamental			
Frequency Range	10		50	MHz
Equivalent Series Resistance (ESR)			70	Ω
Shunt Capacitance			7	pF
Load Capacitance	10		18	pF
Drive Level			500	µW

Recommended Crystals

Diodes Recommends:

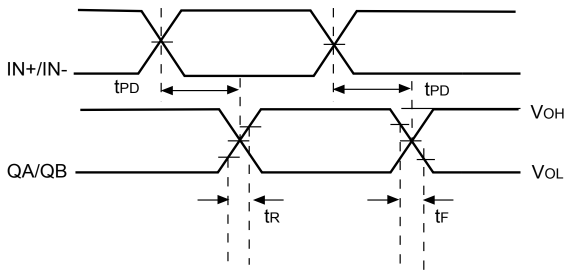
a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm
http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf

b) FY2500091, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm
http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm
http://www.pericom.com/pdf/datasheets/se/FL.pdf

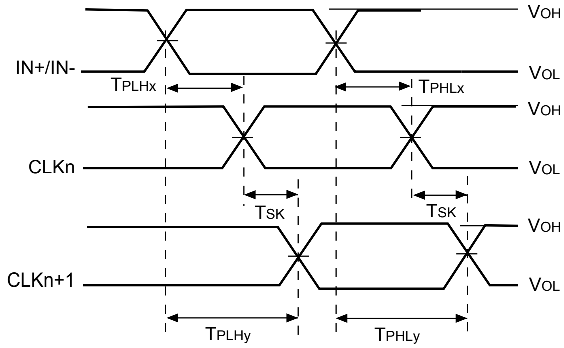
© Diodes Incorporated

Propagation Delay (T_{PD})



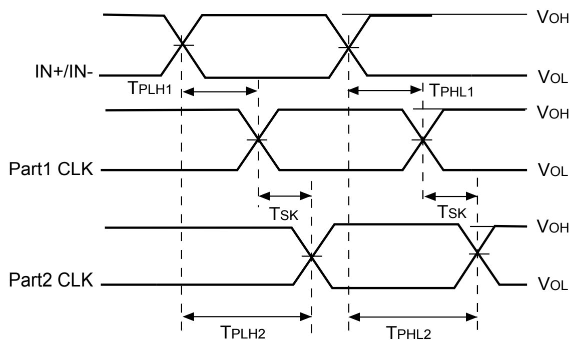
$T_{SK} = T_{PLH2} - T_{PLH1}$ or $T_{SK} = T_{PHL2} - T_{PHL1}$

Output Skew (TSK)



$T_{SK} = T_{PLHy} - T_{PLHx}$ or $T_{SK} = T_{PHLy} - T_{PHLx}$

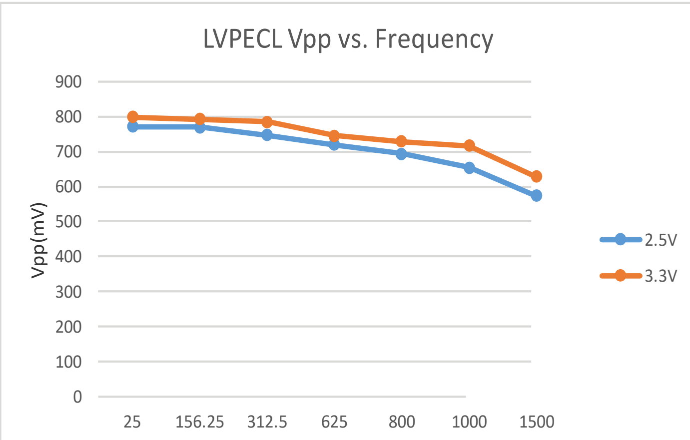
Part to Part Skew

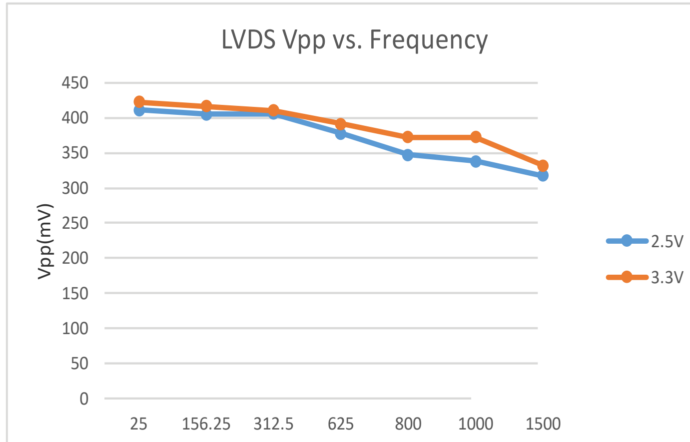


$T_{SK} = T_{PLH2} - T_{PLH1}$ or $T_{SK} = T_{PHL2} - T_{PHL1}$

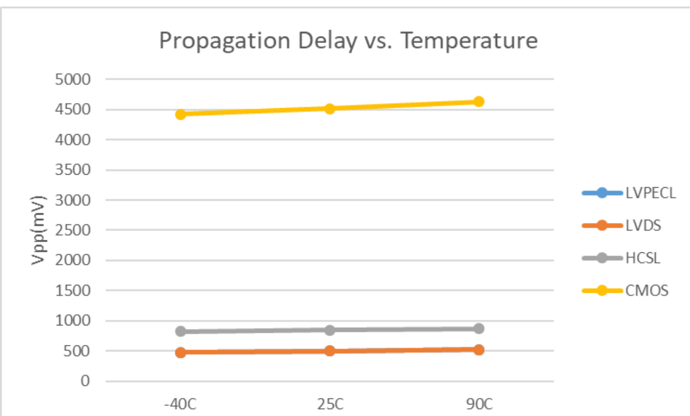
® Diodes Incorporated

LVPECL/ LVDS Output Swing vs. Frequency



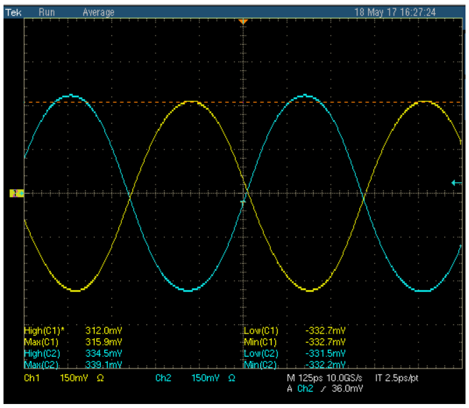


Propagation Delay vs Temperature

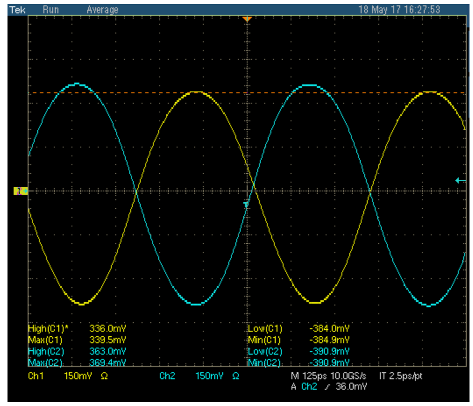


© Diodes Incorporated

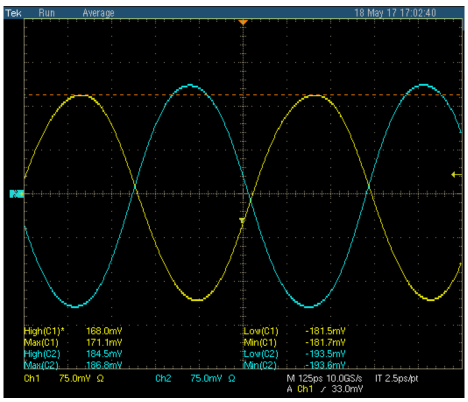
1.5GHz LVPECL/ LVDS Waveform



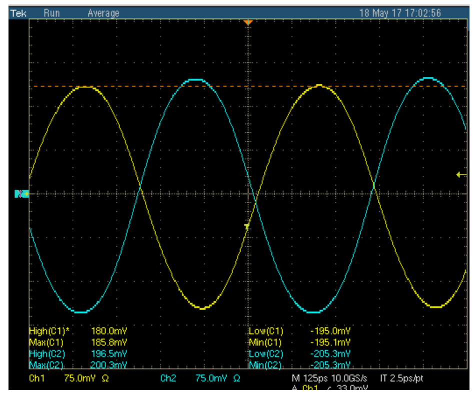
2.5V LVPECL Waveform



3.3V LVPECL Waveform



2.5V LVDS Waveform



3.3V LVDS Waveform

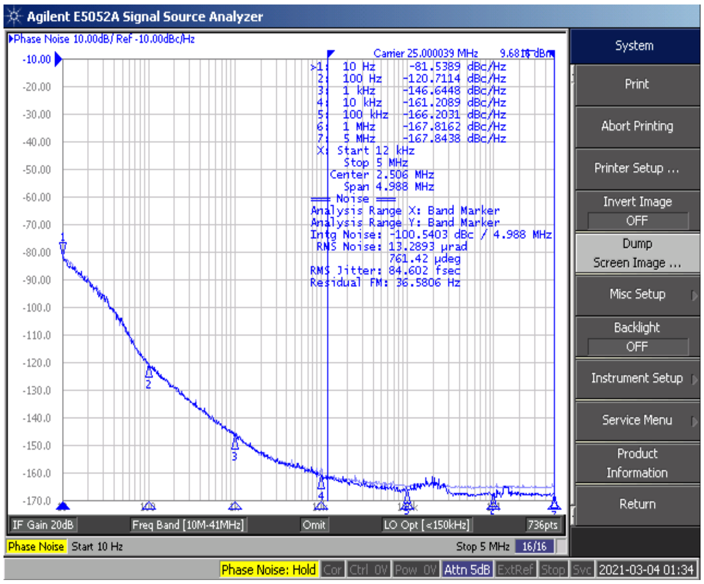
© Diodes Incorporated

Phase Noise and Additive Jitter

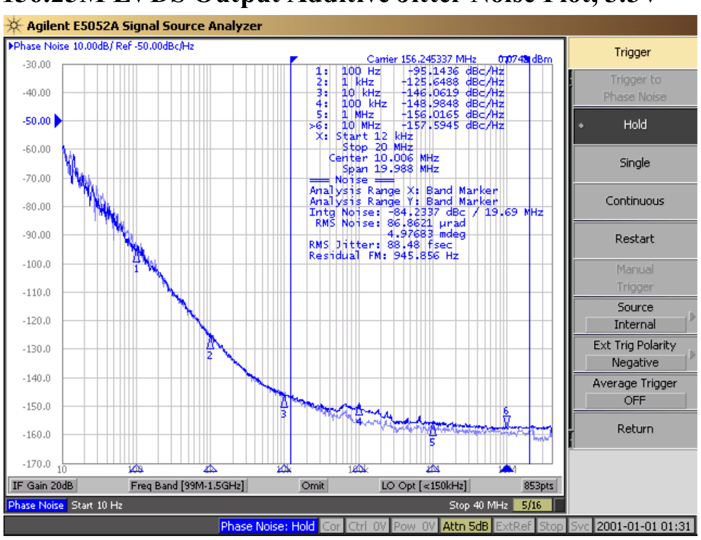
Output phase noise (Dark Blue) vs Input Phase noise (light blue)

Additive jitter is calculated at 25MHz ~71fS RMS (12kHz to 5MHz). Additive jitter = $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$

Ref_out 25MHz Phase Noise Plot, VDD=VDDO=3.3V, 25°C , Driven by 25MHz CMOS XO

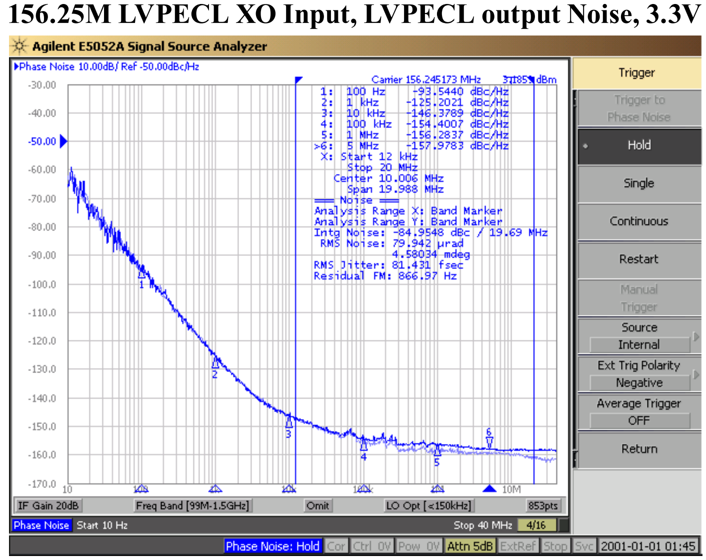


156.25M LVDS Output Additive Jitter Noise Plot, 3.3V



3.3V LVDS Output Jitter 88fs vs. Input 72fs

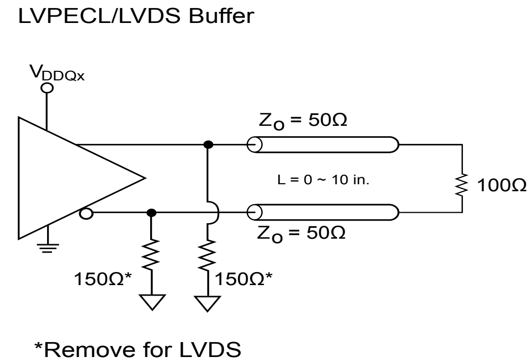
156.25M LVPECL XO Input, LVPECL output Noise, 3.3V



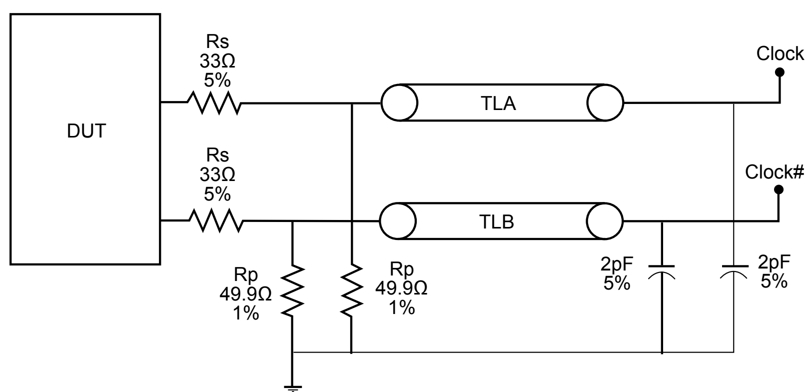
3.3V 156.25M LVPECL Input LVPECL output Jitter 81fs vs. input jitter 75fs

© Diodes Incorporated

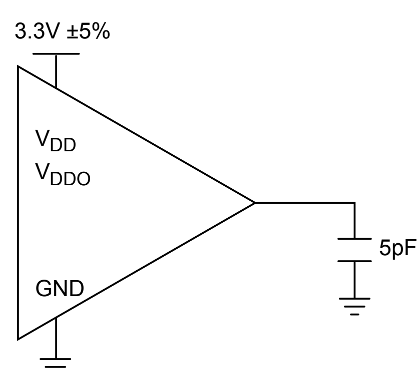
Configuration Test Load Board Termination for LVPECL/ LVDS Outputs



Configuration Test Load Board Termination for HCSL Outputs



Configuration Test Load Board Termination for LVCMOS Outputs



® Diodes Incorporated

Application Information

Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

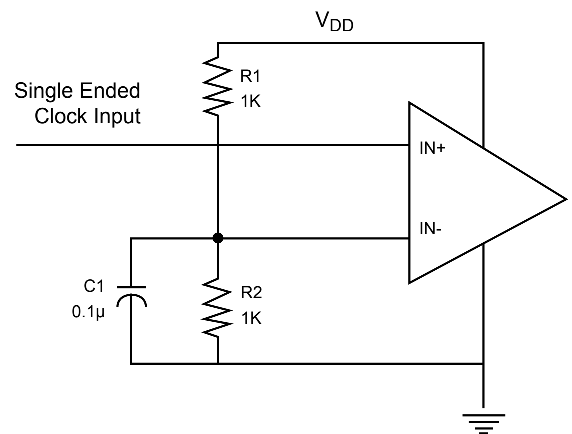
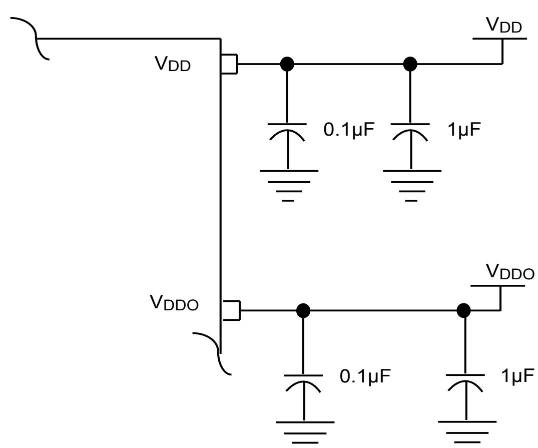


Figure 1. Single-ended Input to Differential Input Device

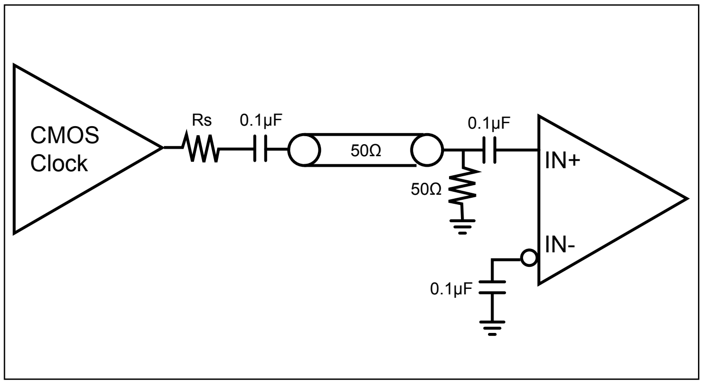
Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. All power pins should be individually connected to the power supply plane through vias, and 0.1µF an 1µF bypass capacitors should be used for each pin.

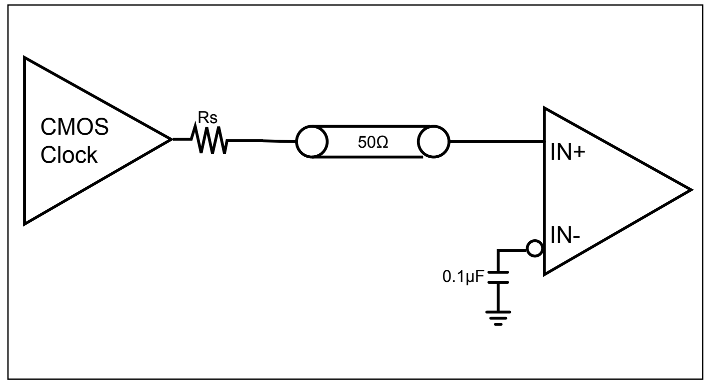


® Diodes Incorporated

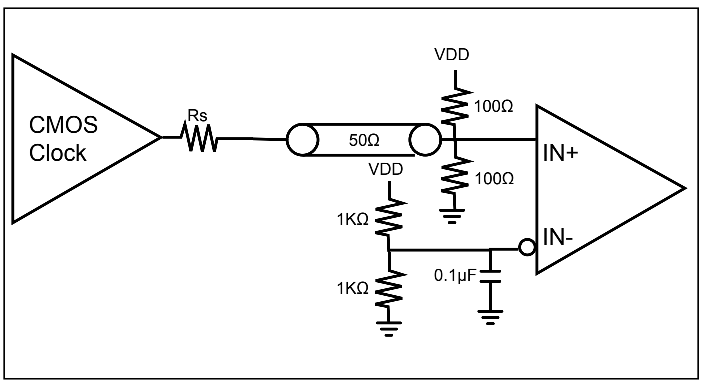
Single Ended Input, AC Couple



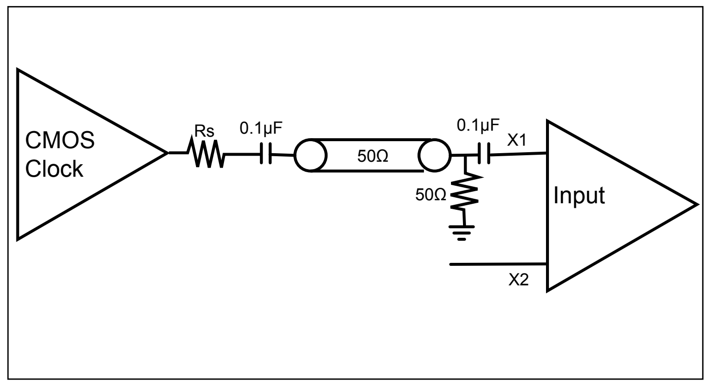
Single Ended Input, DC Couple



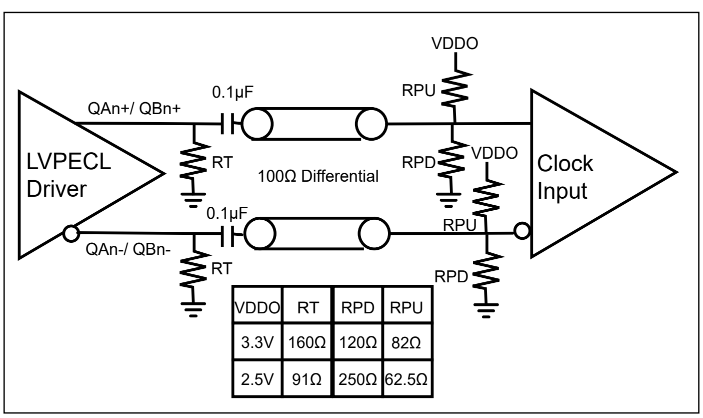
Single Ended Input, DC Couple



Driving X1 with a Single Ended Input

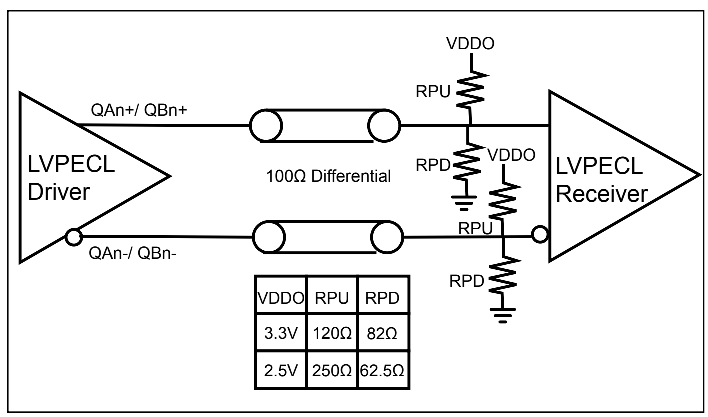


LVPECL, AC Couple, Thevenin Equivalent



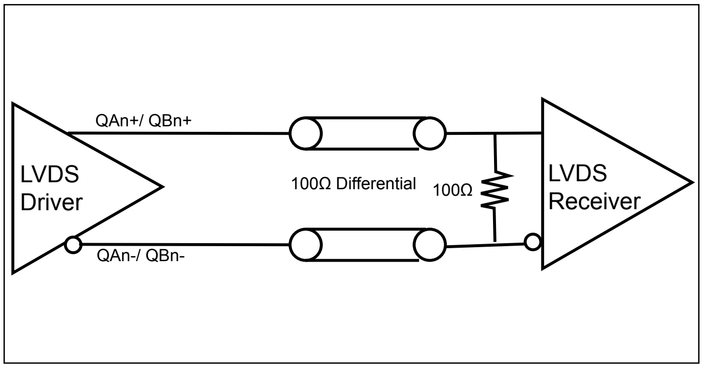
VDDO	RT	RPD	RPU
3.3V	160Ω	120Ω	82Ω
2.5V	91Ω	250Ω	62.5Ω

LVPECL, DC Couple, Thevenin Equivalent

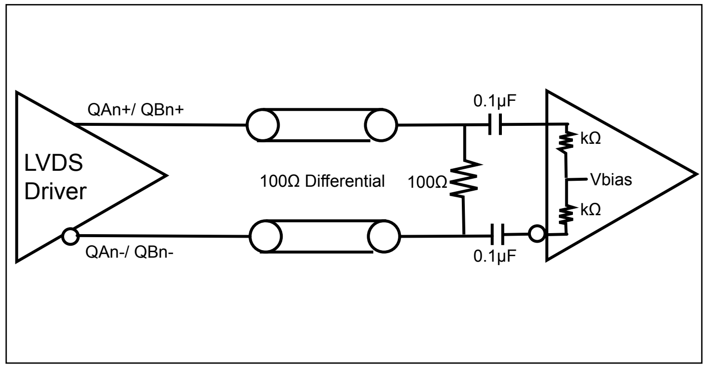


VDDO	RPU	RPD
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

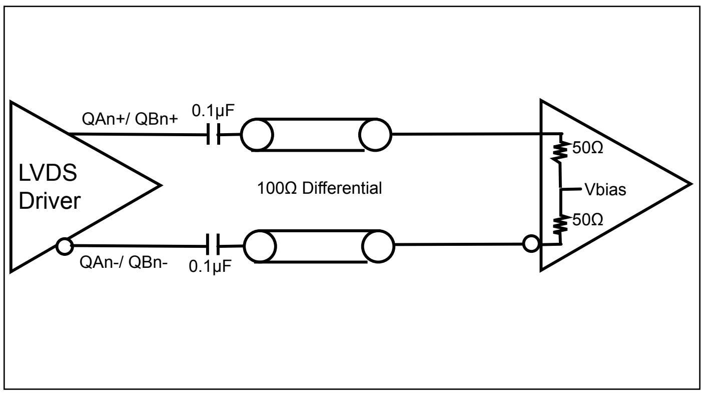
LVDS DC Couple



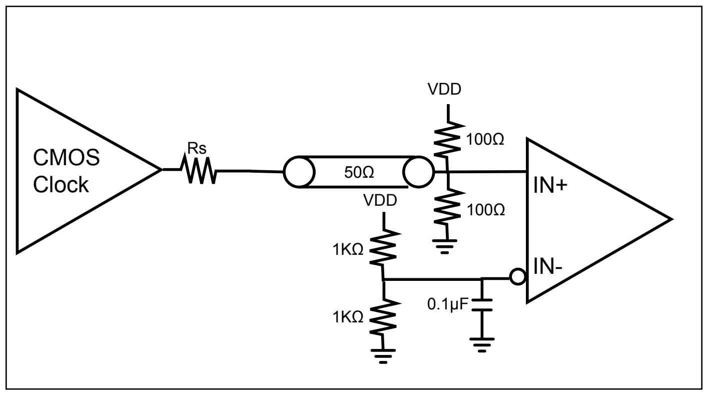
LVDS AC Couple at Load



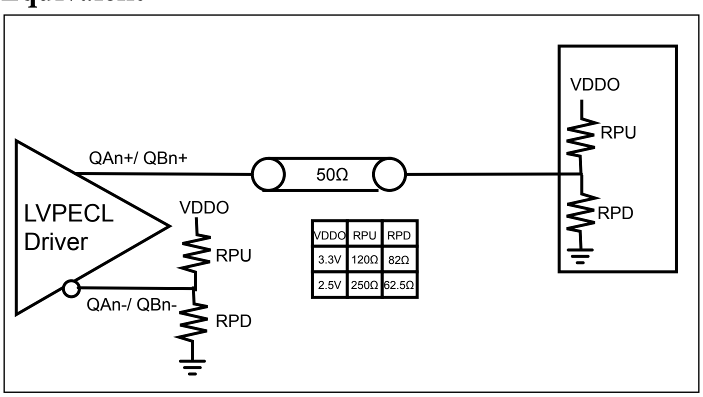
LVDS AC Couple with Internal Termination



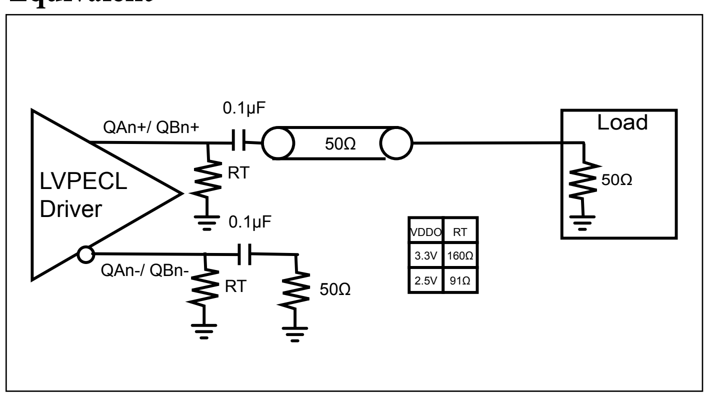
Single Ended LVPECL, DC Couple



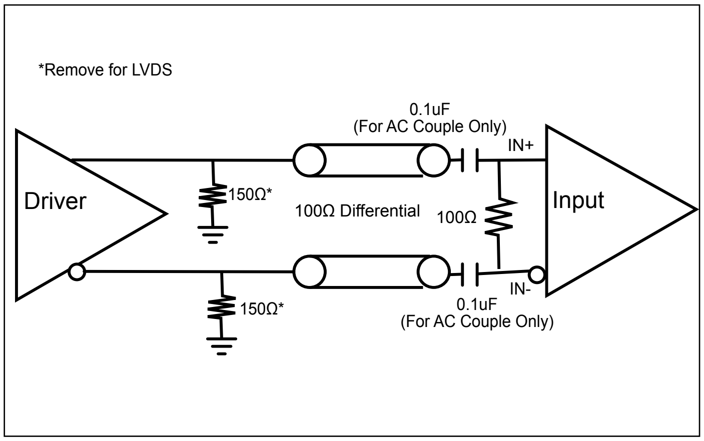
Single Ended LVPECL, DC Couple, Thevenin Equivalent



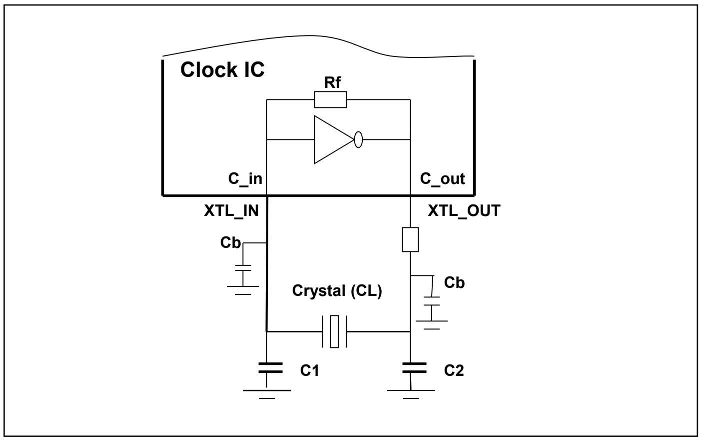
Single Ended LVPECL, AC Couple, Thevenin Equivalent



LVPECL/ LVDS AC and DC input



Clock IC Crystal Input Guide



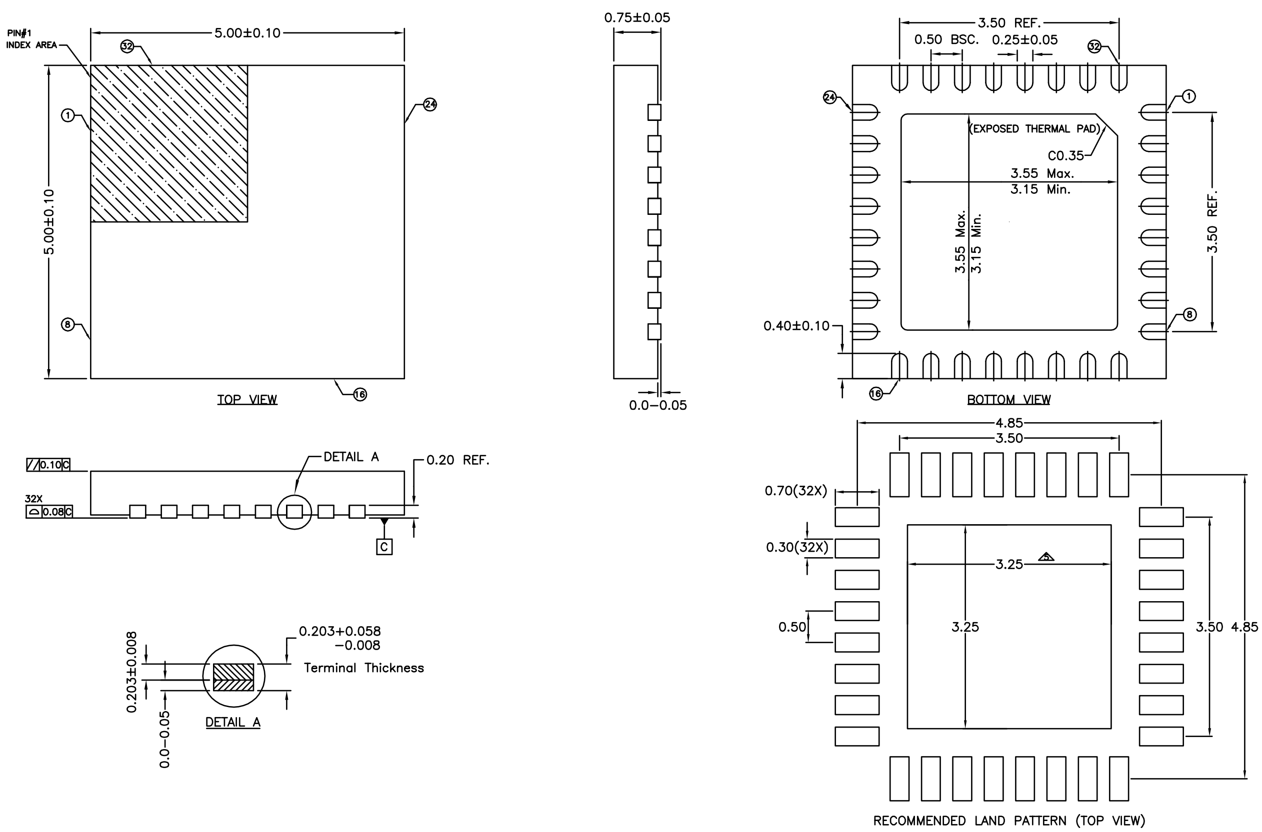
Part Marking

Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

® Diodes Incorporated

Packaging Mechanical

32-TQFN (ZH)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220.
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

DIODES INCORPORATED — PERICOM ENABLING SERIAL CONNECTIVITY

DATE: 12/06/16

DESCRIPTION: 32-Contact, Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZH (ZH32)

DOCUMENT CONTROL #: PD-2070 REVISION: C

17-0570

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description	Operating Temperature
PI6C49S1504TZHIEX	ZH	32-contact, Thin Quad Flat No-Lead (TQFN)	-40 °C to 85 °C

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel

IMPORTANT NOTICE

1. DIODES INCORPORATED AND ITS SUBSIDIARIES ("DIODES") MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes products. Diodes products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of the Diodes products for their intended applications, (c) ensuring their applications, which incorporate Diodes products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.

3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes' websites, harmless against all damages and liabilities.

4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes' website) under this document.

5. Diodes products are provided subject to Diodes' Standard Terms and Conditions of Sale (https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

6. Diodes products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.

7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.

8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.

Copyright © 2021 Diodes Incorporated

www.diodes.com