Octal Sample-and-Hold with Multiplexed Input

SMP08

FEATURES

- **Internal Hold Capacitors**
- **Low Droop Rate**
- **TTL/CMOS Compatible Logic Inputs**
- **Single or Dual Supply Operation**
- **Break-Before-Make Channel Addressing**
- **Compatible With CD4051 Pinout**
- **Low Cost**

APPLICATIONS

- **Multiple Path Timing Deskew for A.T.E.**
- **Memory Programmers**
- **Mass Flow/Process Control Systems**
- **Multichannel Data Acquisition Systems**
- **Robotics and Control Systems**
- **Medical and Analytical Instrumentation**
- **Event Analysis**
- **Stage Lighting Control**

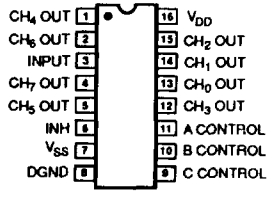
ORDERING INFORMATION †

PACKAGE: 16-PIN DIP/SO		OPERATING TEMPERATURE RANGE
CERDIP 16-PIN	PLASTIC 16-PIN	
TBA*	–	MIL
SMP08FQ	SMP08FP	XIND
–	SMP08FS	XIND

* Consult factory for 883 data sheet.

† Burn-in is available on industrial temperature range parts in CerDIP and plastic DIP packages.

PIN CONNECTIONS



16-PIN CERDIP (Q-Suffix)

16-PIN EPOXY DIP (P-Suffix)

16-PIN SO (S-Suffix)

GENERAL DESCRIPTION

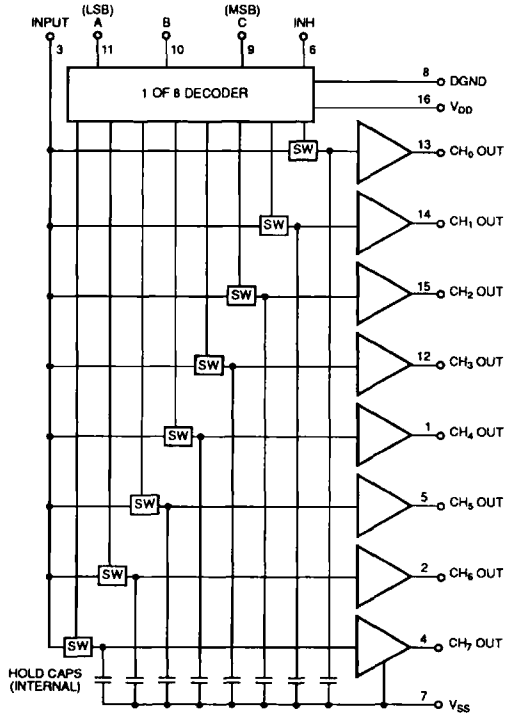
The SMP-08 is a monolithic octal sample-and-hold; it has eight internal buffer amplifiers, input multiplexer, and internal hold capacitors. It is manufactured in an advanced oxide isolated CMOS technology to obtain high accuracy, low droop rate, and fast acquisition time. The SMP-08 has a typical linearity error of only 0.01% and can accurately acquire a 10-bit input signal to ±1/2 LSB in less than seven microseconds. The SMP-08's output swing includes the negative supply in both single and dual supply operation.

The SMP-08 was specifically designed for systems that use a calibration cycle to adjust a multiple of system parameters. The low cost and high level of integration makes the SMP-08 ideal for calibration requirements that have previously required an ASIC, or high cost multiple D/A converters.

The SMP-08 is also ideally suited for a wide variety of sample-and-hold applications including amplifier offset or VCA gain adjustments. One or more SMP-08s can be used with single or multiple DACs to provide multiple set points within a system.

The SMP-08 offers significant cost and size reduction over discrete designs. It is available in a 16-pin hermetic or plastic DIP, or surface mount SOIC package.

FUNCTIONAL DIAGRAM



Manufactured under the following U.S. patent: 4,739,281

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{DD} to DGND ..... –0.3V, 17V
V_{DD} to V_{SS} ..... –0.3V, 17V
V_{LOGIC} to DGND ..... –0.3V, V_{DD}
V_{IN} to DGND ..... V_{SS}, V_{DD}
V_{OUT} to DGND ..... V_{SS}, V_{DD}
Analog Output Current ..... ±20mA
(Not short-circuit protected)
Operating Temperature Range
FP, FS ..... –40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SO (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

CAUTION:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper anti-static handling procedures.
3. Remove power before inserting or removing units from their sockets.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{SS} = –5V, DGND = 0V, R_L = No Load, T_A = –40°C to +85°C for SMP-08F, unless otherwise noted.

			SMP-08F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Linearity Error		–3V ≤ V_{IN} ≤ +3V	—	0.01	—	%
Buffer Offset Voltage	V_{OS}	T_A = +25°C –40°C ≤ T_A ≤ +85°C	— —	2.5 3.5	10 20	mV
Hold Step	V_{HS}	V_{IN} = 0V	—	1	4	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	T_A = +25°C, V_{IN} = 0V	—	2	20	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 0V (Note 1)	1.2	—	—	mA
Output Sink Current	I_{SINK}	V_{IN} = 0V (Note 1)	0.5	—	—	mA
Output Voltage Range		R_L = 20kΩ	–3.0	—	+3.0	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4	—	—	V
Logic Input Low voltage	V_{INL}		—	—	0.8	V
Logic Input Current	I_{IN}	V_{IN} = 2.4V	—	0.5	1	µA
DYNAMIC PERFORMANCE (Note 2)						
Acquisition Time	t_{AQ}	T_A = +25°C, –3V to +3V to 0.1%	—	7	—	µs
Hold Mode Settling Time	t_H	To ± 1mV of Final Value	—	1	—	µs
Channel Select Time	t_{CH}		—	90	—	ns
Channel Deselect Time	t_{DCS}		—	45	—	ns
Inhibit Recovery Time	t_{IR}		—	90	—	ns
Slew Rate	SR		—	3	—	V/µs
Capacitive Load Stability		<30% Overshoot	—	500	—	pF
Analog Crosstalk		–3V to +3V Step	—	–72	—	dB

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{SS} = –5V, DGND = 0V, R_L = No Load, T_A = –40°C to +85°C for SMP-08F, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	SMP-08F MIN	SMP-08F TYP	SMP-08F MAX	UNITS
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±6V	60	75	—	dB
Supply Current	I_{DD}	T_A = +25°C –40°C ≤ T_A ≤ +85°C	— —	5.5 7.5	7.5 9.5	mA

NOTES:
1. Outputs are capable of sinking and sourcing over 20mA but offset is guaranteed at specified load levels.
2. All input control signals are specified with $t_r = t_f$ = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.

ELECTRICAL CHARACTERISTICS at V_{DD} = +12V, V_{SS} = 0V, DGND = 0V, R_L = No Load, T_A = –40°C to +85°C for SMP-08F, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SMP-08F MIN	SMP-08F TYP	SMP-08F MAX	UNITS
Linearity Error		60mV ≤ V_{IN} ≤ 10V	—	0.01	—	%
Buffer Offset Voltage	V_{OS}	T_A = +25°C –40°C ≤ T_A ≤ +85°C	— —	2.5 3.5	10 20	mV
Hold Step	V_{HS}	V_{IN} = 6V	—	1	4	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	T_A = +25°C, V_{IN} = 6V	—	2	20	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 6V (Note 1)	1.2	—	—	mA
Output Sink Current	I_{SINK}	V_{IN} = 6V (Note 1)	0.5	—	—	mA
Output Voltage Range		R_L = 20kΩ R_L = 10kΩ	0.06 0.06	— —	10.0 9.5	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4	—	—	V
Logic Input Low voltage	V_{INL}		—	—	0.8	V
Logic Input Current	I_{IN}	V_{IN} = 2.4V	—	0.5	1	µA
DYNAMIC PERFORMANCE (Note 2)						
Acquisition Time	t_{AQ}	T_A = +25°C, 0 to 10V to 0.1%	—	9	—	µs
Hold Mode Settling Time	t_H	To ± 1mV of Final Value	—	1	—	µs
Channel Select Time	t_{CH}		—	90	—	ns
Channel Deselect Time	t_{DCS}		—	45	—	ns
Inhibit Recovery Time	t_{IR}		—	90	—	ns
Slew Rate	SR	R_L = 20kΩ (Note 3)	3	4	—	V/µs
Capacitive Load Stability		<30% Overshoot	—	500	—	pF
Analog Crosstalk		0 to 10V Step	—	–72	—	dB
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	10.8V ≤ V_{DD} ≤ 13.2V	60	75	—	dB
Supply Current	I_{DD}	T_A = +25°C –40°C ≤ T_A ≤ +85°C	— —	6.0 8.0	8.0 10.0	mA

NOTES:
1. Outputs are capable of sinking and sourcing over 20mA but offset is guaranteed at specified load levels.
2. All input control signals are specified with $t_r = t_f$ = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
3. Slew rate is measured in the sample mode with a 0 to 10V step from 20% to 80%.