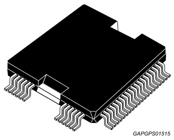
L9779WD

Multifunction IC for engine management system

Datasheet - production data



HiQUAD-64

Features

- 5 V logic regulator
- 3.3 V logic regulator
- 5 V tracking sensor supply
- Smart reset function
- Power latch with Secure Engine Off (SEO) functionality, to safely complete driver switch off procedure
- Flying wheel interface function (VRS) with adaptive time and amplitude control
- Protected low-side relay driver
  - OUT13 to 18, MRD
- Protected low-side (injector drivers)
  - OUT1 to 4
- Protected low-side (high current)
  - OUT5, 6, 7
- Protected low-side (low current)
  - OUT19, 20
- IGBT pre-drivers (IGN1 to 4)
- External MOS pre-drivers (OUT8 to 9)
- Configurable power stages CPS
  - Stepper motor driver/ high-side - low-side (OUT21 to 28)
- Thermal warning and shutdown
- Serial interface
  - Micro Second Channel interface (MSC)
  - ISO9141 interface (K-Line)
- High speed CAN transceiver
- Dedicated pin VDDIO to select the voltage level of digital output used for serial communication
- VDA 2.0 compliance with 3 level Watchdog
- Package: HiQUAD-64

Description

The L9779WD is an integrated circuit designed for automotive environment and implemented in BCD6S technology.

It is conceived to provide all basic functions for standard engine management control units.

It is assembled in the HiQUAD-64 power package.

Table 1. Device summary

Order code	Package	Packing
L9779WD	HiQUAD-64	Tray
L9779WD-TR	HiQUAD-64	Tape and Reel

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1 Detailed features description

- Package
  - HiQUAD-64
- 5 V logic regulator
  - 5 V precision voltage regulator (± 2%) with external NMOS
  - Max current regulated: 400 mA
  - Charge pump capacitor at pin CP is used to drive the gate of the external NMOS transistor
- 3.3 V logic regulator
  - 3.3 V precision voltage regulator (± 2%) with over-current protection
  - Max current regulated: 100 mA
- 5 V tracking sensor supply
  - 2 x 5 V tracking sensor supply with protection and diagnosis on MSC
  - Short-circuit to Vbat/GND fully protected
  - Max current regulated: 2 x 100 mA
- VDD_IO supply
  - All the digital output is supplied by external VDD_IO through VDD_IO pin
- Smart reset
  - Main Reset monitoring VB_UV Logic voltage management and safety control
- Watch dog
  - Main reset management 5 V voltage monitoring safety output disable
  - MicroSecond Channel activity watch dog
  - MSC controllable query and answer watch dog compliant with VDA2.0 level 3 (enabled by default)
- Power latch
  - L9779WD is switched on by KEY_ON signal and switched off by logic OR of KEY_ON signal and MicroSecond Channel bit
- Secure engine off mode (default) switches off the drivers in the following order:
  - OUT1 through to OUT4 in 225 ms (typical)
  - OUT13 and OUT14 in 600 ms (typical)
- Flying wheel interface function (VRS)
  - The VRS is the interface between the microprocessor and the magnetic pick-up or variable reluctance sensor that collects the information coming from the flying wheel
  - Adaptive filtering on amplitude and timing adapts better the device response to VRS input switching
- Protected low-side driver
  - LSa (OUT1 to 5)

    4 Ch. serial IN via MicroSecond Channel, R_{dson} = 0.72 Ohm @150 °C, V_{cl} = 58 V ±5, I_{max} = 2.2 A;

    1 Ch. serial IN via MicroSecond Channel, R_{dson} = 0.72 Ohm @150 °C, V_{cl} = 58 V ±5, I_{max} = 3 A;

– LSb (OUT6, 7)

  2 Ch. serial IN via MicroSecond Channel, R_{dson} = 0.47 Ohm @150°C, V_{cl} = 45 V ±5, I_{max} = 5 A

– LSc (OUT19, 20)

  2 Ch serial IN via MicroSecond Channel, I_{max} = 50 mA

Full diagnosis on MicroSecond Channel (2 bit for each channel) and voltage slew rate control.

When an over current fault occurs, the driver switch off with faster slew rate in order to reduce the power dissipation.

- Protected low side relay driver (OUT13 to 18, MRD)
  - LSD

    6 Ch. serial IN via MicroSecond Channel, R_{dson} = 1.5 Ohm @150 °C, V_{cl} = 48 V, I_{max} = 600 mA (2 of them with low battery voltage function);

    1 main relay driver R_{dson} = 2.4 Ohm @150 °C, V_{cl} = 48 V, I_{max} = 600 mA

  With full diagnosis on MicroSecond Channel (2 bit for each channel) and voltage slew-rate control.

  When an over current fault occurs, the driver switch off with faster slew rate in order to reduce the power dissipation.

- Ignition pre-drivers (IGN1 to 4)
  - 4 x ignition pre-drivers with full diagnostic.
- External MOS pre-drivers (OUT8 to 9)
  - 2 x MOS pre-drivers with sense of the external drain voltage to perform the diagnostic:

    Open load in OFF state

    Shorted load in ON state with programmable threshold voltage and programmable filter time via MSC

- Configurable power stages CPS: stepper motor driver/ high-side - low-side (OUT21 to 28)

  1 x Stepper motor driver designed for a double winding coil motor, used for engine idle speed control.

  The bridge driver is made by 4 independent high-side drivers and 4 independent low-side drivers:

  - 4 high-side driver, R_{dson} =1.5 Ohm, I_{max} = 600 mA
  - 4 low-side driver, R_{dson} = 1.5 Ohm, I_{max} = 600mA

  The 4 high-side drivers and the 4 low-side drivers can be controlled independently

  The low-side drivers could be connected in parallel (in pairs): OUT22 with OUT24 and OUT27 with OUT28.

  Low-side and high-side drivers implement voltage SR control to minimize emission.

  Two high-side drivers have the low battery voltage function.

- Thermal shutdown
  - 1 x Thermal shutdown (T_j > 175 °C = Tsd) if T_j > Tsd: VTRK1, 2 are turned off.
  - 1 x Thermal shutdown (T_j > 175 °C = Tsd) if Tj > Tsd: OUT1 to 10, OUT13 to 20, OUT21 to 28, IGN1 to 4 are turned off.
  - 1 x Thermal shutdown (T_j > 175 °C = Tsd) if T_j > Tsd: MRD is turned off (if battery present).

– 1 x Thermal Shutdown (T_j > 175 °C = Tsd) if T_j > Tsd: V3V3 is turned off.

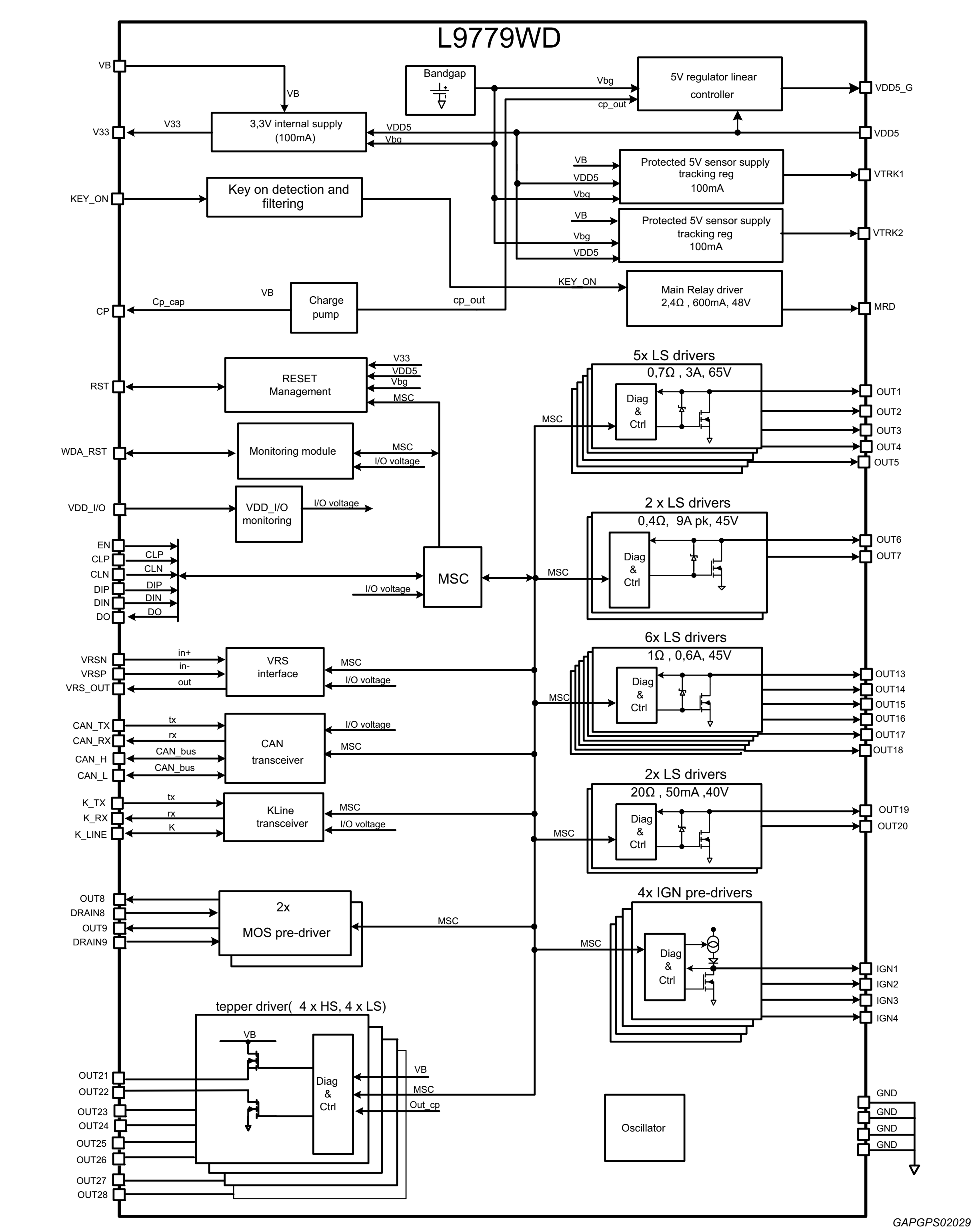
There are 5 temperature sensors for OT2 (OUT1..10, OUT13…20, OUT21…28, IGN1…4 are turned off) in different Layout position, they are logically “AND” in case of thermal shutdown.

- ISO9141 interface
  – ISO9141 serial interface (K-Line)
- CAN transceiver

  The CAN bus transceiver allows the connection of the microcontroller, with CAN controller unit, to a high speed CAN bus with transmission rates up to 1Mbit/s for exchange of data with other ECUs.

2 Block diagram

Figure 1. Block diagram



3 Pins description

Figure 2. Pins connection diagram (top view)

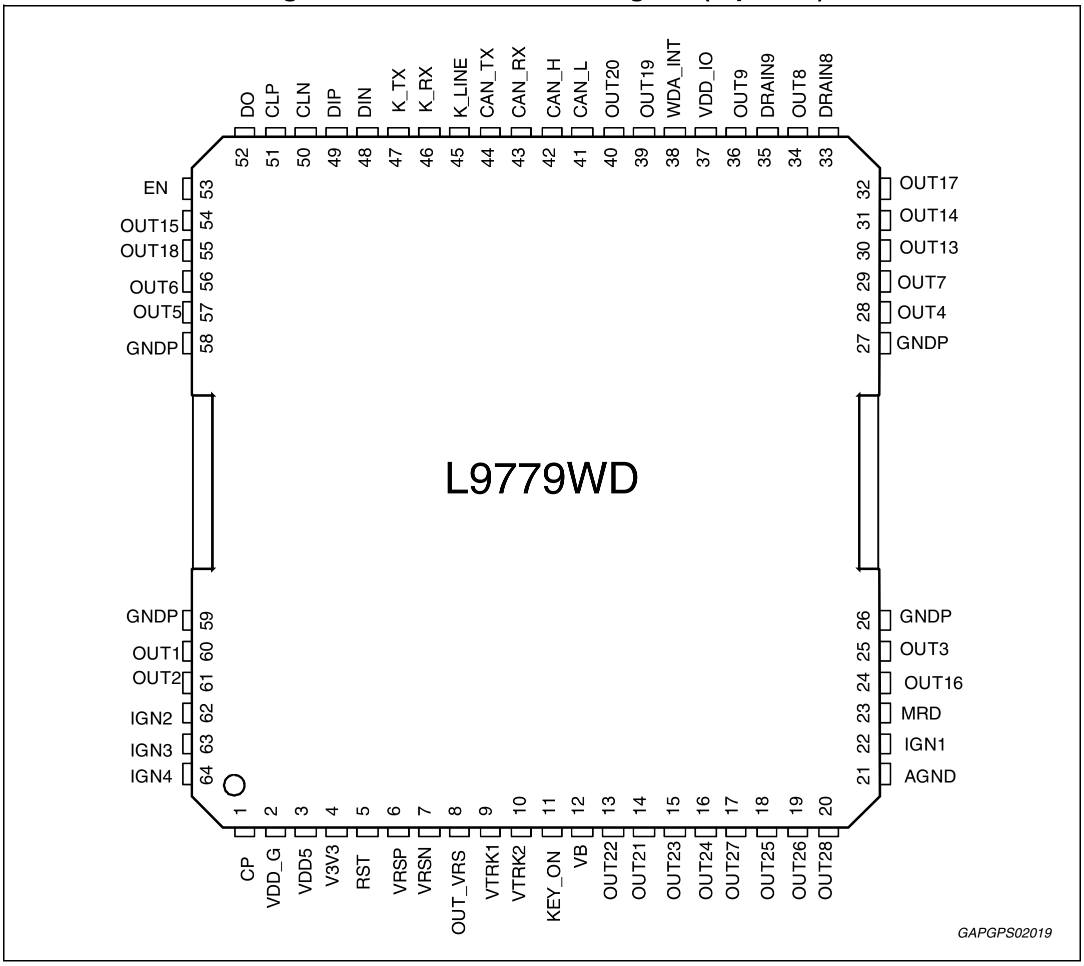


Table 2. Pins description

Pin#	Name	Function	Type	Polarization/note
Supply block				
12	VB	Battery supply	Power supply polarization	-
3	VDD5	5 V output voltage regulator	Power logic output supply	-
2	VDD_G	5 V regulator ext MOS gate	Analog output	-
11	KEY_ON	Key signal	Analog Input	Internal pull down resistor
4	V3V3	3.3 V output voltage regulator	Power logic output supply	-
1	CP	Charge pump	Analog Input	-
9	VTRK1	Sensor1 tracking supply 5V	Sensor supply output	-

Table 2. Pins description (continued)

Pin#	Name	Function	Type	Polarization/note
10	VTRK2	Sensor1 tracking supply 5V	Sensor supply output	-
5	RST	Reset input/output for µP	Output: push-pull DGT input	Open drain
37	VDD_IO	External supply	Power input	-
38	WDA_INT	WDA Interrupt Signal	Output: open drain DGT input	-
VRS				
7	VRSN	Negative VRS input	Analog input	1.65 V internal polarization
6	VRSP	Positive VRS input	Analog input	1.65 V internal polarization
8	OUT_VRS	Digital VRS output	DGT output	Push-pull
CAN				
44	CAN_TX	Can transceiver input (from TX µP)	DGT input	-
43	CAN_RX	Can transceiver output (to RX µP)	DGT output	-
42	CAN_H	Bi-dir protected CAN_H wire	Analog input/output	-
41	CAN_L	Bi-dir protected CAN_L wire	Analog input/output	-
ISO9141				
47	K_TX	ISO9141 logical input	DGT input	Internal pull-up resistor
45	K_LINE	Bi-dir protected K-line wire	Analog input/output	Open drain
46	K_RX	ISO9141logical output	DGT output	Push-pull
Low side drivers				
60	OUT1	Output low-side 1 for R, L load (Injector)	Power output	Open drain
61	OUT2	Output low-side 2 for R, L load (Injector)	Power output	Open drain
25	OUT3	Output low-side 3 for R, L load (Injector)	Power output	Open drain
28	OUT4	Output low-side 4 for R, L load (Injector)	Power output	Open drain
26	PGND	Power GND	PGND	-
27	PGND	Power GND	PGND	-
57	OUT5	Output low-side 5 for R, L load (high current)	Power output	Open drain
56	OUT6	Output low-side 6 for R, L load (heater)	Power output	Open drain
29	OUT7	Output low-side 7 for R, L load (heater)	Power output	Open drain

Table 2. Pins description (continued)

Pin#	Name	Function	Type	Polarization/note
30	OUT13	Output low-side 13 for relay (low. bat.)	Power output	Open drain
31	OUT14	Output low-side 14 for relay (low. bat.)	Power output	Open drain
54	OUT15	output low-side 15 for relay	Power output	Open drain
24	OUT16	Output low-side 16 for relay	Power output	Open drain
32	OUT17	Output low-side 17 for relay	Power output	Open drain
55	OUT18	Output low-side 18 for relay	Power output	Open drain
58	PGND	Power GND	PGND	-
59	PGND	Power GND	PGND	-
Ignition pre-driver				
22	IGN1	Output ignition driver 1	Power output	-
62	IGN2	Output ignition driver 2	Power output	-
63	IGN3	Output ignition driver 3	Power output	-
64	IGN4	Output ignition driver 4	Power output	-
21	GND_STEP	Analog GND	AGND	-
Main relay driver				
23	MRD	Main relay driver	Power output	Open drain
Low current drivers (50 mA)				
39	OUT19	Output low-side 19	Power Output	Open drain
40	OUT20	Output low-side 20	Power Output	Open drain
Ext MOS pre-driver				
33	DRAIN8	Ext. drain voltage sense for OUT8	Input	-
34	OUT8	Gate driver for ext MOS OUT8	Power output	-
35	DRAIN9	Ext. Drain voltage sense for OUT9	Input	-
36	OUT9	Gate driver for ext MOS OUT9	Power output	-
MSC interface				
51	CLP	Clock positive for differential interface	DGT Input	-
50	CLN	Clock negative for differential interface	DGT Input	-
49	DIP	Downstream data positive for differential interface	DGT Input	-
48	DIN	Downstream data negative for differential interface	DGT Input	-
53	EN	Enable pin	DGT Input	-

Table 2. Pins description (continued)

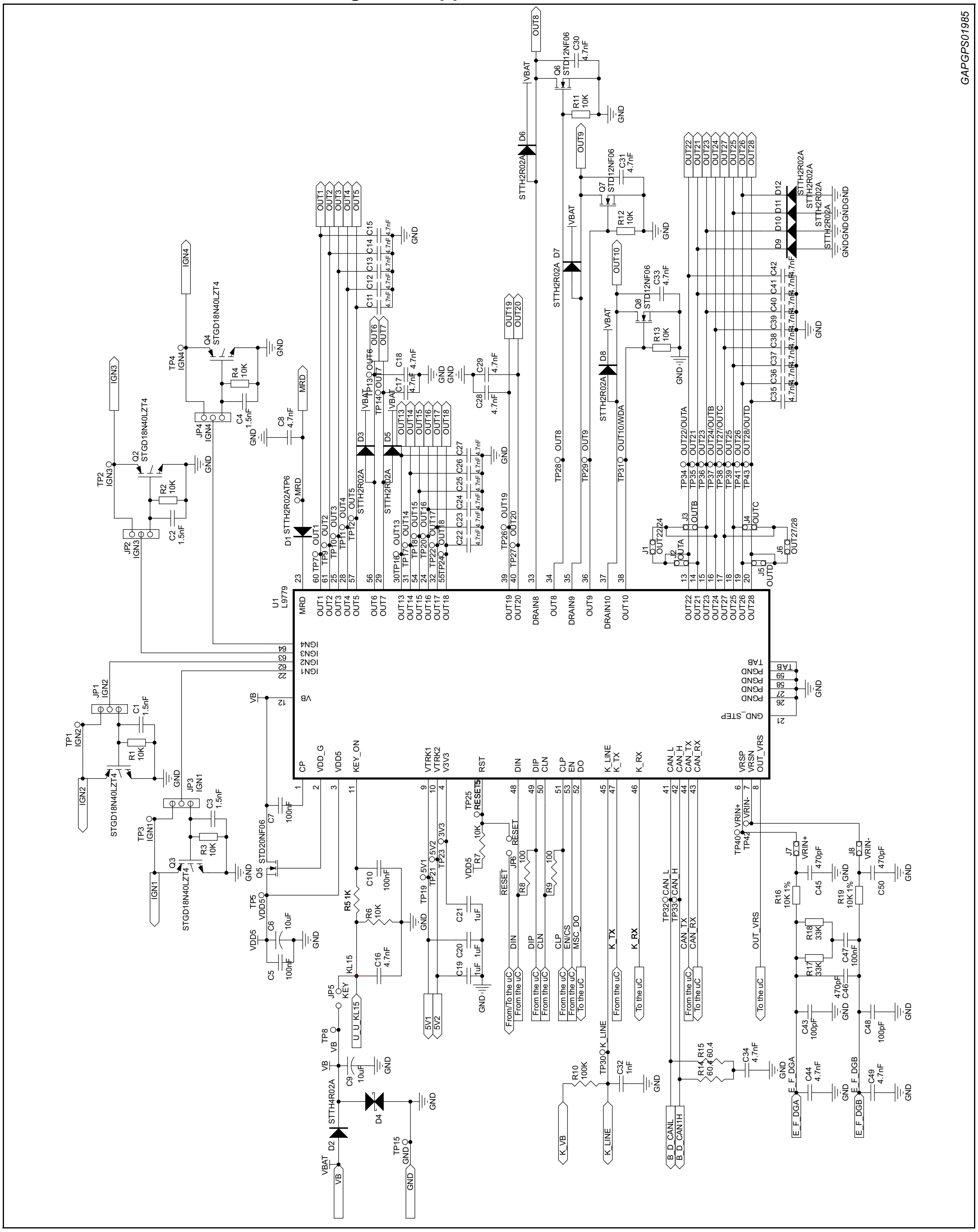
Pin#	Name	Function	Type	Polarization/note
52	DO	Upstream data push-pull output	DGT Output	-
Configurable power stage: Stepper motor driver / low-side, high-side drivers				
14	OUT21	Output high-side 21 / stepper (low. bat.)	Power output	Open drain
13	OUT22	Output low-side 22/ stepper	Power output	Open drain
15	OUT23	Output high-side 23 / stepper	Power output	Open drain
16	OUT24	Output low-side 24 / stepper	Power output	Open drain
18	OUT25	Output high-side 25 / stepper (low. bat.)	Power output	Open drain
19	OUT26	Output high-side 26 / stepper	Power output	Open drain
17	OUT27	Output low-side 27/ stepper	Power output	Open drain
20	OUT28	Output low-side 28 / stepper	Power output	Open drain

Note: OUT11 and OUT12 are not valid.

All the powers GND are connected to the package slug, so it is mandatory to connect the slug to GND.

4 Application schematic

Figure 3. Application schematic



5 Absolute maximum ratings

Warning: Maximum ratings are absolute ratings: exceeding any of these values may cause permanent damage to the integrated circuit

Table 3. Absolute maximum ratings

Pin	Parameter	Condition	Value	Unit
VB	DC supply battery power voltage (Vb)	Also without external components	-0.3 to +40	V
V3V3	DC logic supply voltage	-	-0.3 to VDD5, when V3V3 = VDD5 = max+19V	V
VTRK1,2	DC sensors supply voltage	-	-2 to +40	V
VDD_G	-	-	-0.3 to VDD5, when VDDG = VDD5 = max+19	V
VDD5	Voltage pin	-	-0.3 to 19	V
CP	-	-	-0.3 to 40 Max ABS = +40 V when VB = 40 V	V
KEY_ON	-	Protected with external component (R = 1 kΩ plus a diode, refer to *Figure 4*) for negative pulse (isopulse 1)	-1.2 to +40	V
RST	-	-	-0.3 to +19	V
VRSP	-	Max current to be limited with external resistors (see *Section 6.16.3: Application circuits on page 106*)	-20 to +20	mA
VRSM	-	Max current to be limited with external resistors (see *Section 6.16.3: Application circuits on page 106*)	-20 to +20	mA
MRD	-	-	-0.3 to +40	V
OUT1-5	Low-side output	-	-1 to +53	V
OUT6-7	Low-side output	-	-1 to +40	V
OUT8-9	-	-	-0.3 to 40	V
VDD_IO	DC logic output supply voltage	-	-0.3 to 19	V
DRAIN8-9	-	-	-1 to 60	V
WDA_INT	-	-	-0.3 to 19	V

Table 3. Absolute maximum ratings (continued)

Pin	Parameter	Condition	Value	Unit
OUT13-18	Low-side output	-	-1 to +40	V
OUT19-20	Low-side output	-	-1 to +40	
IGNx	-	-	-1 to 19	V
OUT21, 23, 25, 26	High-side output	With external diode vs ground for negative voltage	-1.0 to VB (–2.0 dynamically for a short time)	V
OUT22, 24, 27 28	Low-side output	-	-1 to 41	V
DIP,DIN	-	-	-0.3 to +19	V
DO, CAN_RX,K_RX, OUT_VRS	-	-	-0.3 to VDD_IO, when DO = VDD_IO = max+19V	V
EN	-	-	-0.3 to +19	V
CLP,CLN	-	-	-0.3 to +19	V
CAN_TX	-	-	-0.3 to +19	V
CAN_H, CAN_L	-	-	-18 to 40 (1)	V
K_TX	-	-	-0.3 to +19	V
K_LINE	-	-	-18 to 40	V

1. In case of negative voltage is applied on CAN_H or CAN_L the voltage slew rate must be <10 V/µs.

5.1 ESD protection

Table 4. ESD protection

Item	Condition	Min	Max	Unit
All pins	Electro static discharge voltage “Charged-device-model – CDM” all pin(1)	-500	+500	V
All pins	Electro static discharge voltage “Charged-device-model – CDM” corner pin (1,20,21,32,33,52,53,64)	-750	+750	V
All pins	ESD voltage HBM respect to GND	-1.5	+1.5	KV
Pins to connector(2)	ESD voltage HBM respect to GND	-4	+4	KV

1. All pins are OK at ±500 V except VTRK1, VTRK2, VB, CP, HIGHSIDE21-23-25-26. [1, 9, 10, 12, 14, 15, 18 e 19]. Pins 1, 9, 10, 12, 14, 15, 18 e 19 passed ±350 V
2. Pins to connector are: LSa, LSb, LSc, LSd, DRAIN1-3, IGNx,VTRK1-2, CAN_H, CAN_L, K_LINE, OUT22, 24, 27, 28. (60, 61, 24, 25, 28, 29, 30, 31, 32, 39, 40, 54, 55, 56, 57, 22, 62, 63, 64, 9, 10, 42, 41, 45, 13, 16, 17, 20, 33, 35).

Test circuit according to HBM (EIA/JESD22-A114-B) and CDM (EIA/JESD22-C101-C).

5.2 Latch-up test

According to JEDEC 78 class 2 level A.

5.3 Temperature ranges and thermal data

Table 5. Temperature ranges and thermal data

Symbol	Parameter	Min	Max	Unit
T_{amb}	Operating temperature	-40	125	°C
T_j	Continuative operative junction temperature	-40	150	°C
T_{stg}	Storage temperature	-40	150	°C
$R_{thj-case}$	Thermal resistance junction-to-case	-	1	°C/W
$R_{thj-amb}$	Thermal resistance junction-to-ambient(1)	-	16	°C/W
T_s	Lead temperature during soldering (for a time = 10 s max)	-	260	°C

1. With 2S2P+vias PCB.

5.4 Operating range

Table 6. Operating range

Pins symbol	Battery voltage range	Junction temperature condition	Note
VB	4.15 V < Vb < 6 V	-40 < Tj < 40	Low battery
	6 V < Vb = 18 V	-40 < Tj < 150	Normal battery
	18 V < Vb = 28 V	-40 < Tj < 40	High battery
	28 < Vb = 40 V, t_{rise} = 10ms, T_{pulse}= 400 ms.	-40 < Tj < 40	Load dump

5.4.1 Low battery

All the functions are guaranteed with degraded parameters. The voltage regulators follow VB in RDSon mode with drop-out depending on load current.
V3V3 regulator works as expected assuming VDD5 > 4 V.

5.4.2 Normal battery

All the functions and the parameters are guaranteed by testing coverage.

5.4.3 High battery

All the functions are guaranteed with degraded parameters.

5.4.4 Load dump

The device is switched-off if load dump exceeds battery overvoltage threshold for a time longer than filter time.

6 Functional description

6.1 Ignition switch, main relay, battery pin

The system has an ignition switch pin KEY_ON and a pin VB for battery behind the main relay connected at pin MRD.

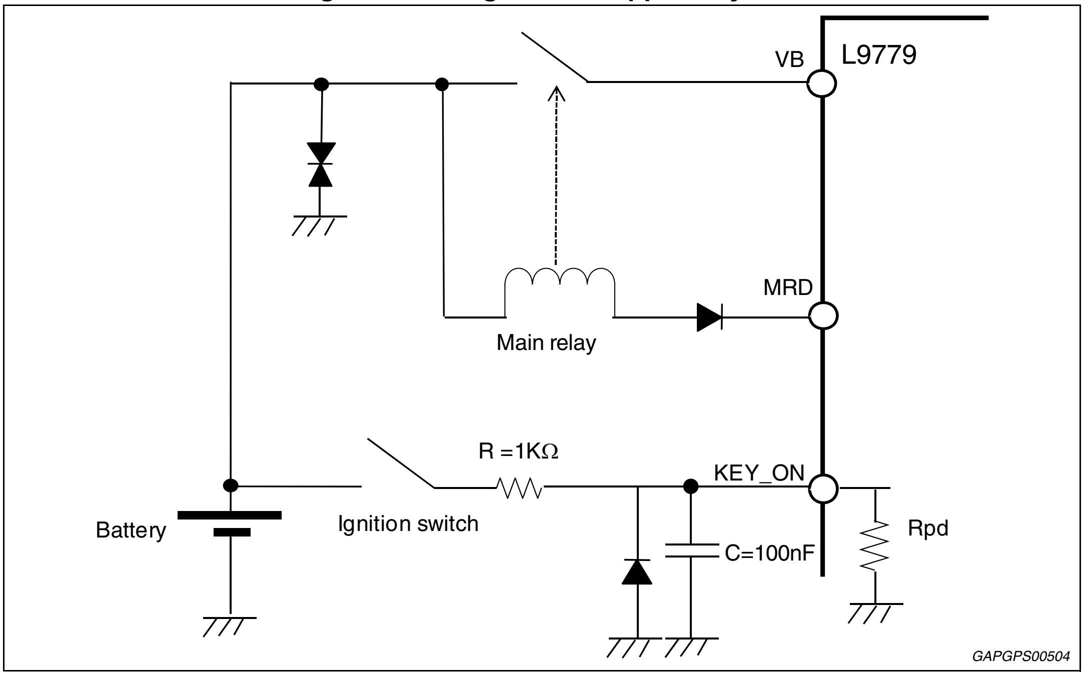
L9779WD can also support the configuration where it is permanently supplied by VB; in this case the MRD output can be used to connect the loads to VB.

At pin KEY_ON there is an external diode for reverse battery protection. An internal Pull-down resistor is provided on the KEY_ON pin. The external components to be connected to KEY pin are shown in the below schematic.

Internal functions and regulators are supplied by VB; only some basic functions required for startup are supplied from KEY_ON as described below. Reverse protection for pin VB is done by the main relay. Transient negative voltage at VB may be limited by an external diode if necessary. There is no integrated reverse protection at pin VB.

The pin connected to the battery line can bear the ISO 7637/1 noise pulses without any damage. The VB voltage must be externally limited to +40 V and -0.3 V (with external components as in *Figure 4*). It is suggested the use of a transil.

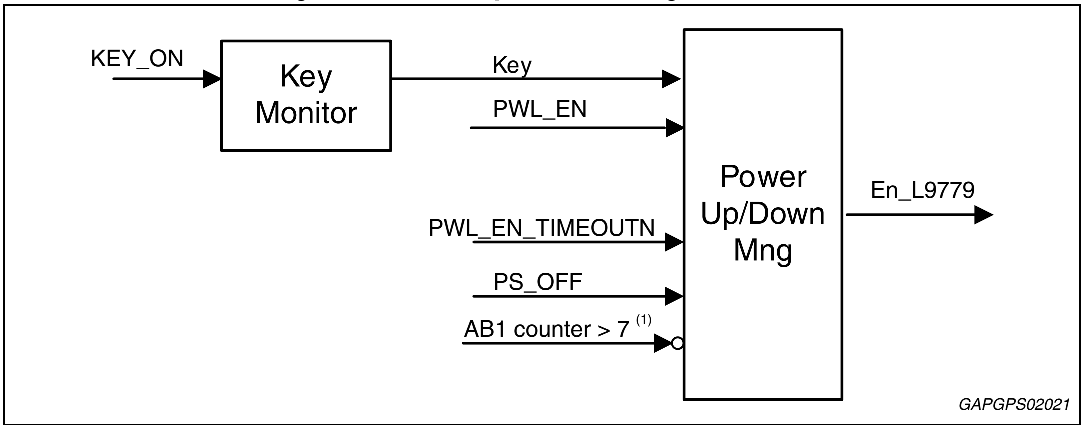
Figure 4. Configuration supplied by VB



1. The external components connected to KEY_ON pin are mandatory in order to protect the device from ISO 7637 pulses.

6.2 Power-up/down management unit

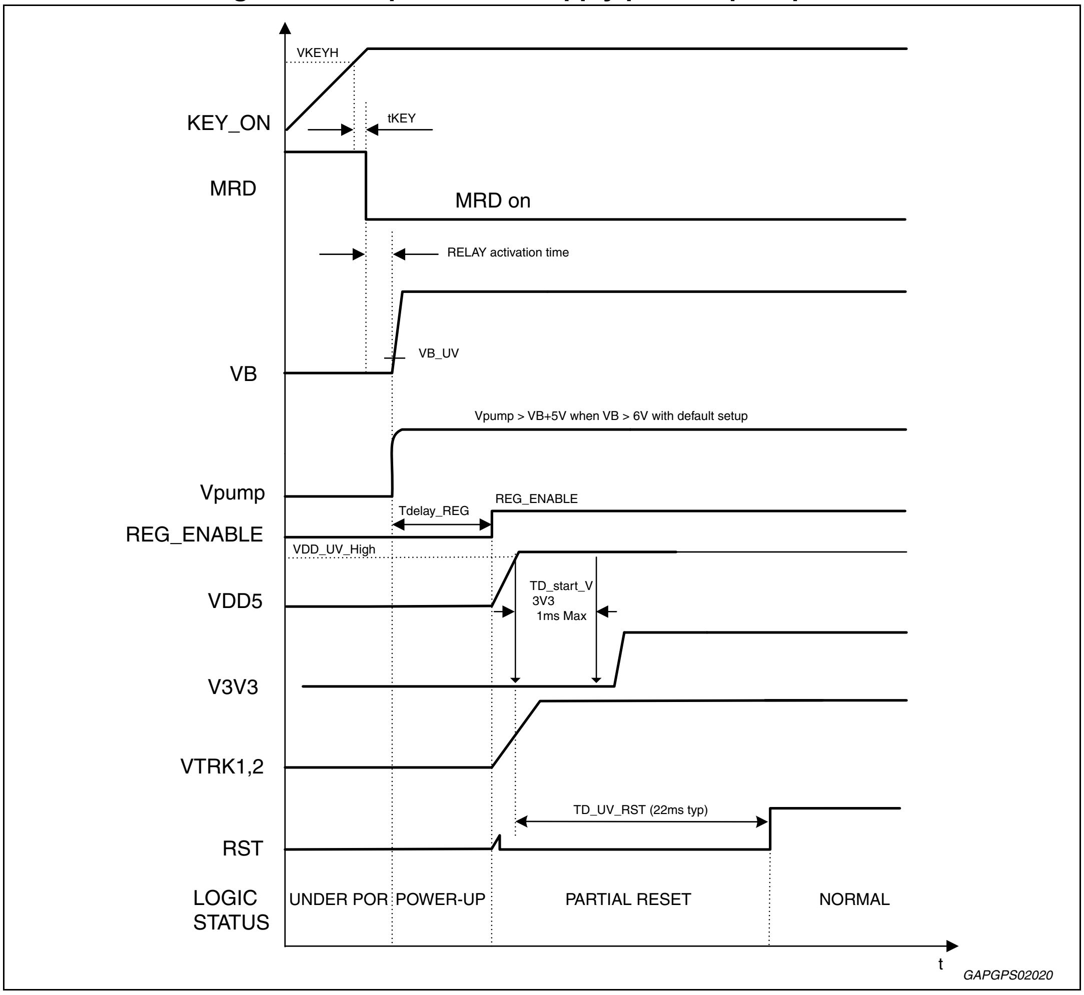
Figure 5. Power-up/down management unit



1. AB1 counter function defined at WDA *Section 6.17.1*.

6.2.1 Power-up sequence

Figure 6. Non-permanent supply power-up sequence



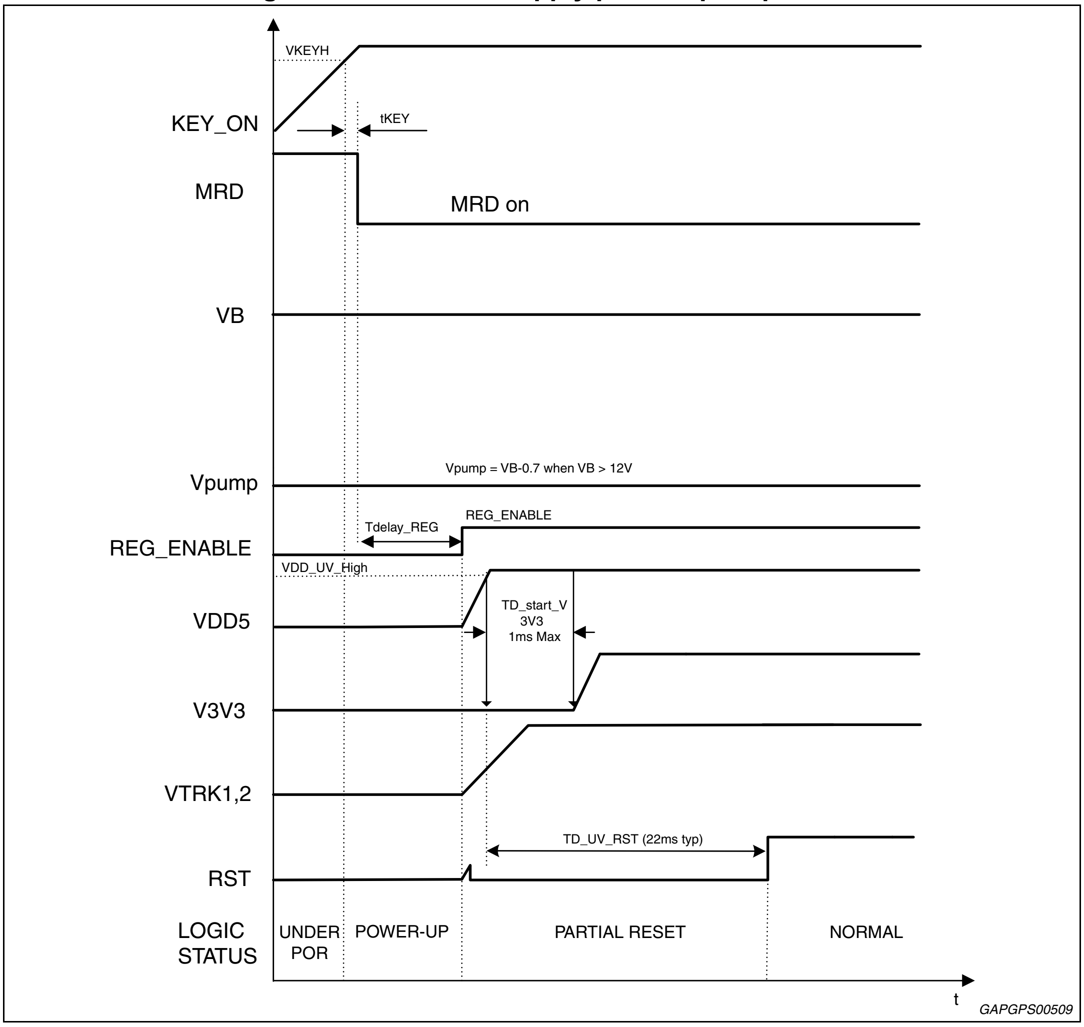
When the KEY_ON reaches a sufficient high voltage VKEYH, after a minimum deglitch filter time T_KEY the system is switched on. First of all the main relay driver is switched on, so the main relay connects VB pin to battery.

Control current into pin KEY_ON is sufficient for basic functions such as filtering time, control the main relay output stage, internal oscillator and internal bias currents.

When the voltage at VB exceeds the under voltage-detection threshold for VB (VB_UV_H) the internal biasing circuits are activated.

VDD5 regulator is activated Tdelay_REG seconds later. After VDD5 exceeds the VDD_UV threshold and with typ. 1.0 ms delay, the V3V3 is activated also. The sensor supplies VTRK1, 2 are turned on together with VDD5.

Figure 7. Permanent supply power-up sequence



In case VB is always connected, when the KEY_ON voltage exceeds VKEYH the internal biasing circuits are activated.

VDD5 regulator is activated Tdelay_REG seconds after the tKEY filter time has expired.

VDD5 regulator is activated Tdelay_REG seconds later. After VDD5 exceeds the VDD_UV threshold and with typ. 1.0 ms delay, the V3V3 is activated also. The sensor supplies VTRK1, 2 are turned on together with VDD5.

6.2.2 Power-down sequence

The system is switched off according to the status of KEY_ON, VB and power latch mode bit PWL_EN_N set by the µC, according to:

En_L9779 = [(!PWL_EN_N AND PWL_EN_TIMEOUTN) OR KEY_ON] AND VB_UVN.

The KEY_ON is the status of KEY_ON pin after deglitch filter time.

En_L9779 represents the enable signals used by different blocks.

The system will be switched off after a minimum deglitch filter time if the voltage at pin KEY_ON is below VKEYL and if power latch mode is not active i.e. PWL_EN_N =1.

Otherwise, if the power latch mode is active PWL_EN_N=0, nothing happens until the power latch mode has finished by the µC writing PWL_EN_N=1.

However L9779WD will wait for a maximum time-out time PWL_TIMEOUT for PWL_EN_N de-assertion after which the system will be forced to switch off. PWL_TIMEOUT can be enabled and configured by 3 bit PWL_TIMEOUT_CONF.

For TNL description see Smart reset circuit description.

The status of KEY_ON can be read through the bit KEY_ON_STATUS. After tKEY filter time the status of KEY_ON can be read through the bit KEY_ON_FLT also.

All the supply outputs shall be switched-off simultaneously. If the supplied devices have particular sequencing requirements, external diodes or clamping devices will be used.

During power down, whether the regulators are switched off at the same time as the main relay output or not is decided via the <PSOFF> bit.

- <PSOFF>='0' (default): simultaneous switching-off the regulators with the main-relay driver MRD
- <PSOFF>='1': regulators remain active when the main relay driver MRD will be switched off

With this function it is possible to detect a stuck main relay. If conditions to switch off are satisfied when <PSOFF>='1', the MRD is switched off while the voltage regulators continue to operate as long as no under voltage is detected at VB. The RST pin is not asserted till VDD_UV. The µC measures the time passed since shutdown. If a certain time is exceeded, then a stuck main relay is detected and this fault is stored in the µC (not in the L9779WD). After this the µC turns off the voltage regulators by setting the bit <PSOFF> to '0' (reset state). With a stuck main relay the voltage at pin VB remains present at battery level with a current consumption of I_{Leak}.

Secure Engine Off function is that the engine can be directly switched off by the key-switch via a hardware path and without the help or interference of software or µC.

Whenever the KEY_ON signal goes low the output stages mentioned in the following pages are disabled.

In no power latch/no SEO mode the key-switch has direct shut-off access to the injector stages (OUT1-4 in L9779) and to the starter relay drivers (OUT13 and OUT14).

An additional feature for the starter delay drivers is that the starters are only shut-off after the time delay THOLD if the SEO condition is still active. To satisfy the Secure Engine Switch off THOLD time, we need to activate the drivers OUT1-4 at least for 225 ms and the OUT 13/14 at least for 600 ms when the Key is ON, the Watch DOG Algorithm [Watchdog influence *Section 6.17.2*] is served and the PWL is enabled after the power on.

The KEY_ON, WDA and “OUT 13/ 14 Switch ON” events for 13 and 14 channels or the KEY_ON, WDA [Watchdog influence *Section 6.17.2*] and "OUT_1-4 Switch ON" events for 1 to 4 channels are “anded” by the internal SEO filter in order to guarantee the THOLD switch off time after the KEY OFF. Example: If the Key is not maintained in ON state for at least 225 ms for driver 1 to 4 and 600 ms for drivers 13/14, the SEO hold time will not be granted and the drivers are switched off immediately at next Key turn OFF. The same behaviour will happen if the WDA [Watchdog influence *Section 6.17.2*] is not served (EC ≥ 4) for 225 ms and 600ms when Key is in ON state after the POWER ON.

The ignition stages are not affected by the SEO signal. This is different from the WDA signal which additionally switches off the ignition stages.

To avoid misunderstandings one must be aware that the SEO function has nothing to do with the WDA function and is not a part of the WDA module. The SEO function is related to the key switch, not to the WDA function. The SEO function adds an additional safety procedure for switching off.

Other functions than the injector stages and the starter relay drivers are not affected or influenced by the SEO signal.

With the falling edge of KEY_ON a timer is started which disables the mentioned power stages after 200 ms to 250 ms (typ. 225 ms). The timer is clocked by an internal oscillator. The timer does not depend on any µC clock or function. The µC still has control on switching on/off drivers during SEO time. This function is configured by CONFIG_REG6 register. After a SEO event, KEY should be stay ON for at least 600ms so to allow a further SEO event delay.

Figure 8. Power-down sequence without power latch mode

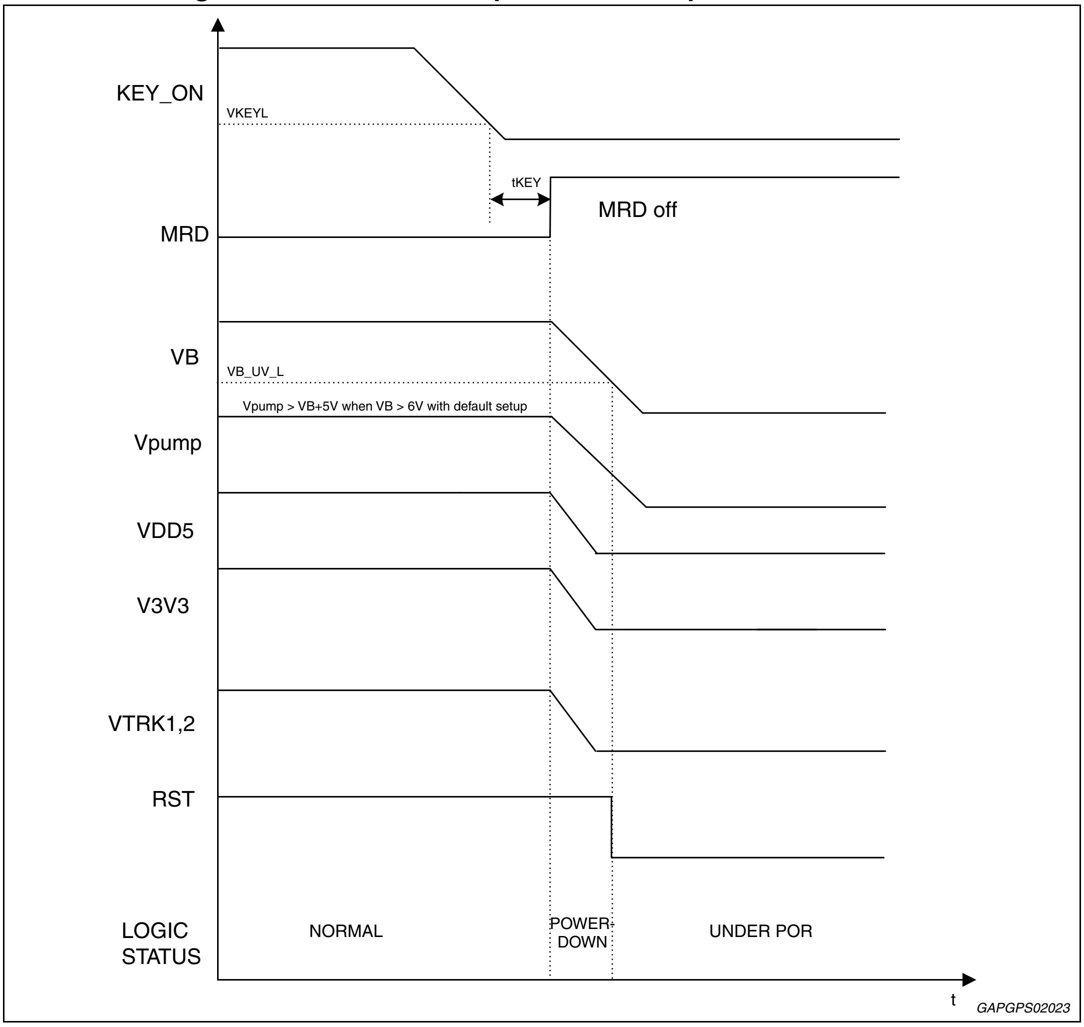


Figure 9. Power-down sequence without power latch mode and PSOFF = 1

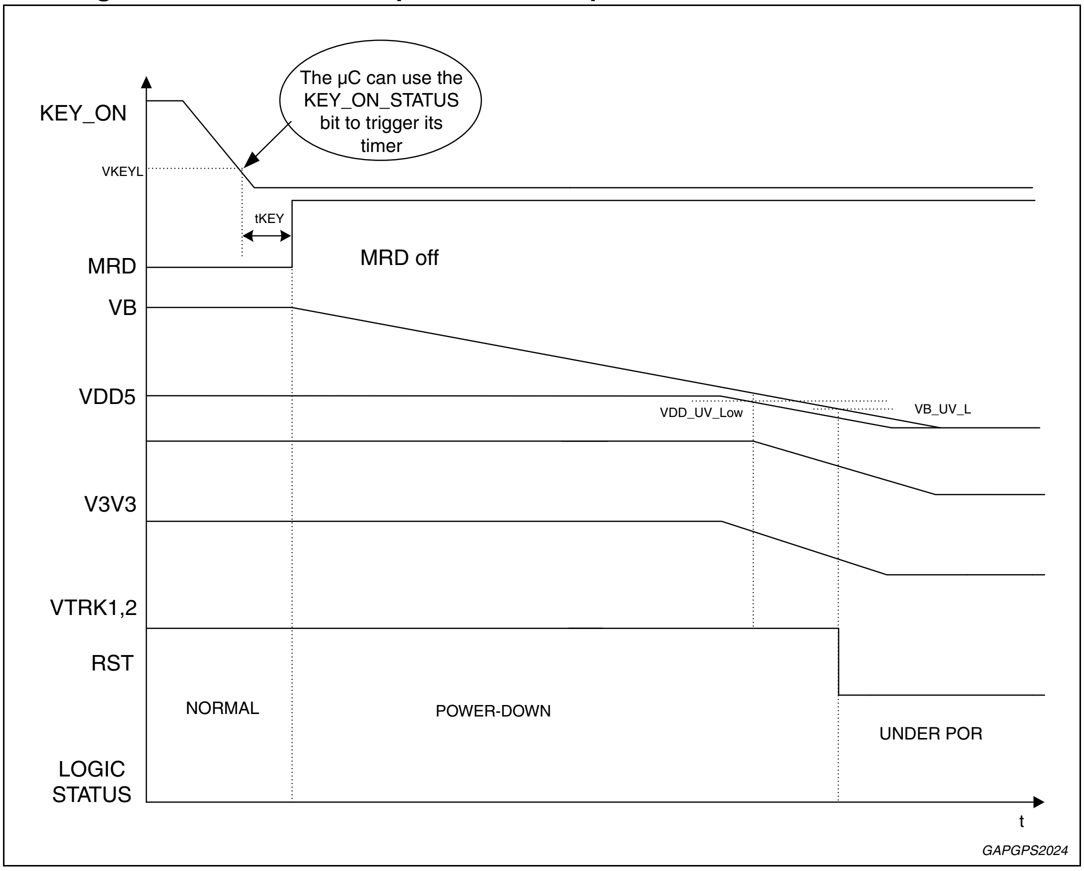


Figure 10. Power-down sequence with power latch mode

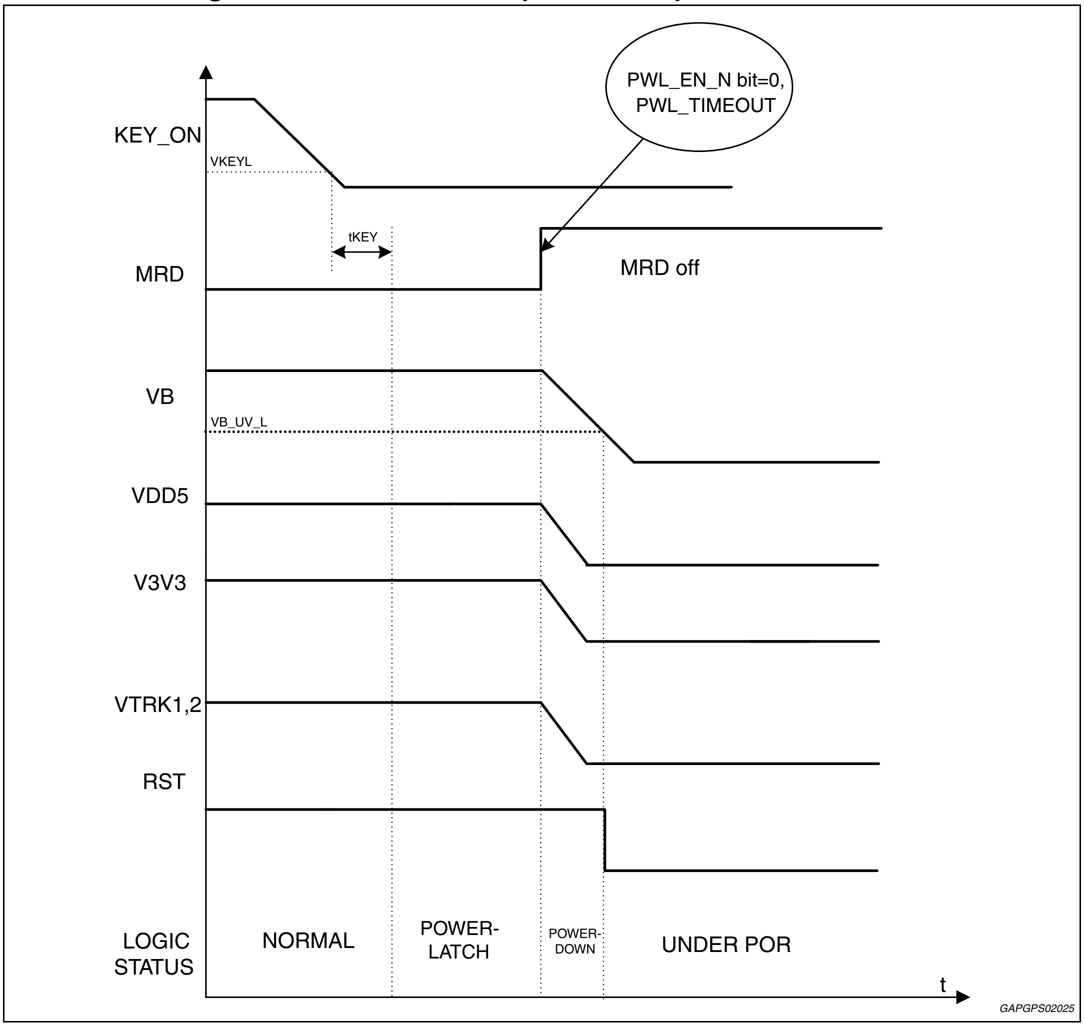


Figure 11. Power-down sequence with power latch mode and KEY_ON toggle

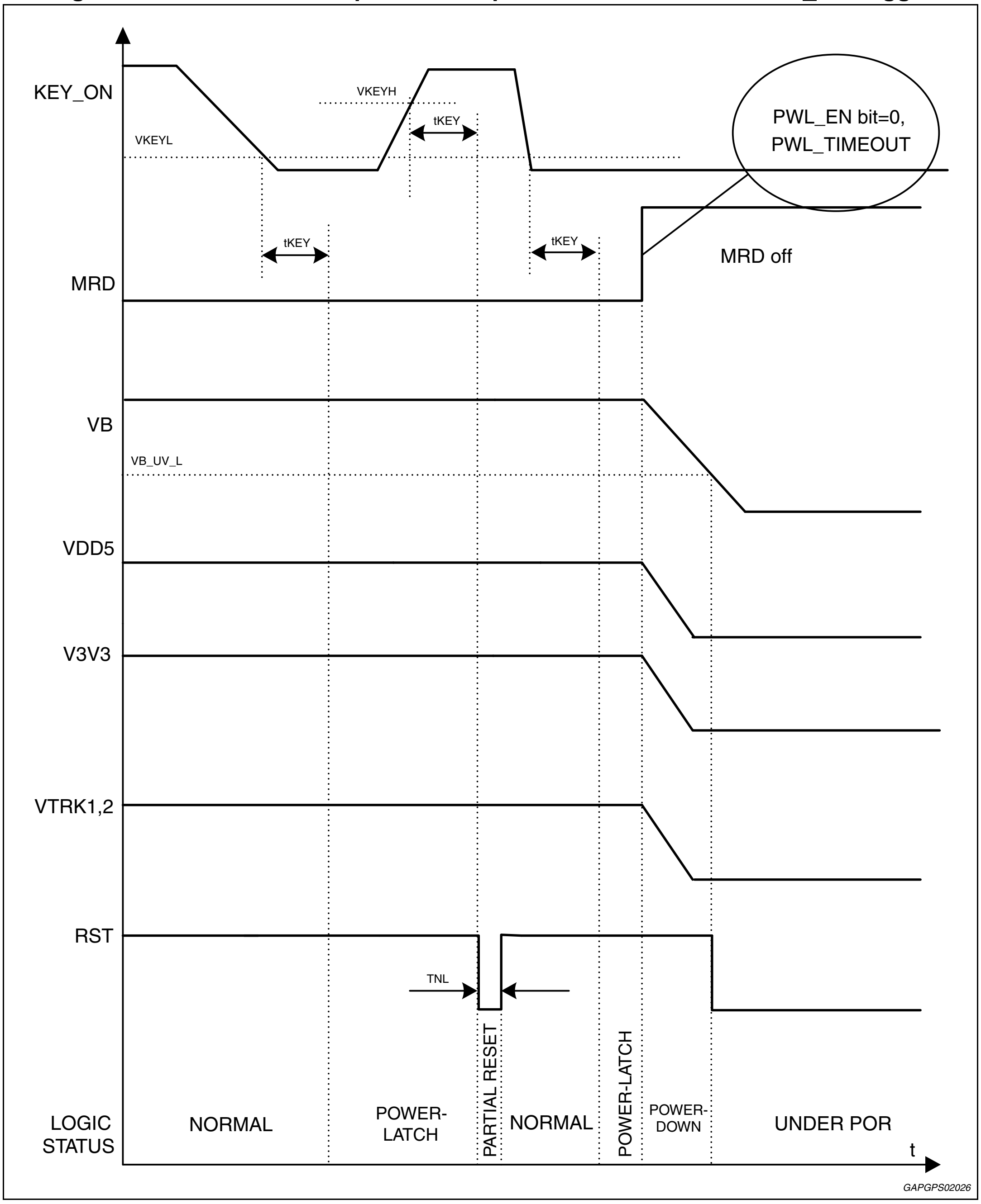
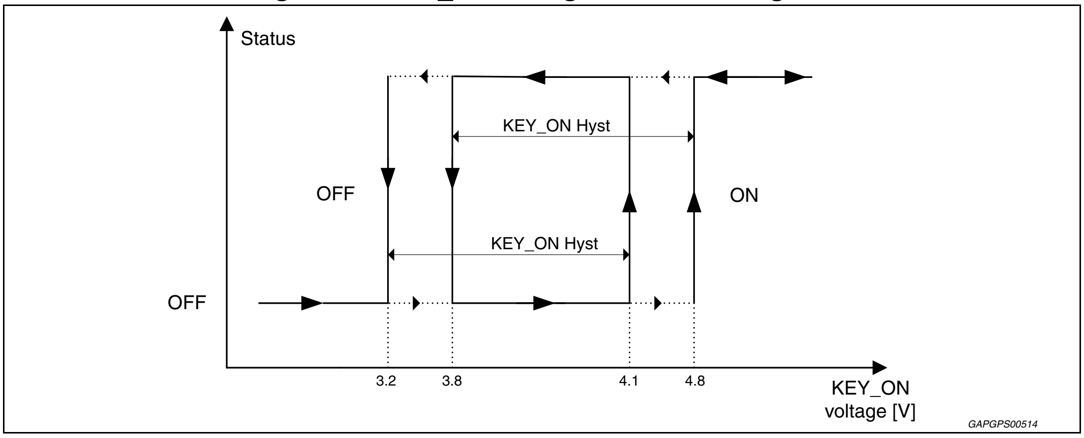


Table 7. KEY_ON pin electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
KEY_ON	VKEYL	Input threshold low voltage	VB = 0 to 19 V	3.2	3.5	3.8	V
	VKEYH	Input threshold high voltage		4.15	4.5	4.8	V
	$VKEY_{HYS}$	Input voltage hysteresis		0.5	1	1.5	V
	I_KEY	Input current	VB = 0 to 19 V KEY_ON = 5 V	-	-	550	µA
	t_{KEY}	Filter time for switching on/off	VB = 0 to 19 V	7.5	16	24	ms
	Rpd	Internal pull down resistor - NOT tested - Guarantee by design	KEY_ON = 5 V	150	-	400	kΩ

Figure 12. KEY_ON voltage vs. status diagram



6.3 VDD_IO function

6.3.1 Description of VDD_IO function and IC pin

The scope of the VDD_IO function and the new related VDD_IO pin is that the voltage level of the L9779WD output ports can be adapted to the voltage levels of the ports of different microcontrollers.The L9779WD output ports to be considered are the DO, CAN-RX, K_RX,OUT_VRS, RST, WDA_INT. RST and WDA_INT are open drain structures.

The L9779WD input ports have a fixed voltage level which is compatible with both 3.3 V and 5 V µC-port voltages.

As the VDD_IO is an external supply, it is monitored and is evaluated for the reset generation.

Concerning the max ratings, the VDD_IO pin should be specified similarly to the VDD5 pin up to 19V.

The operating range would be at least from 2.9 V to 5.5 V.

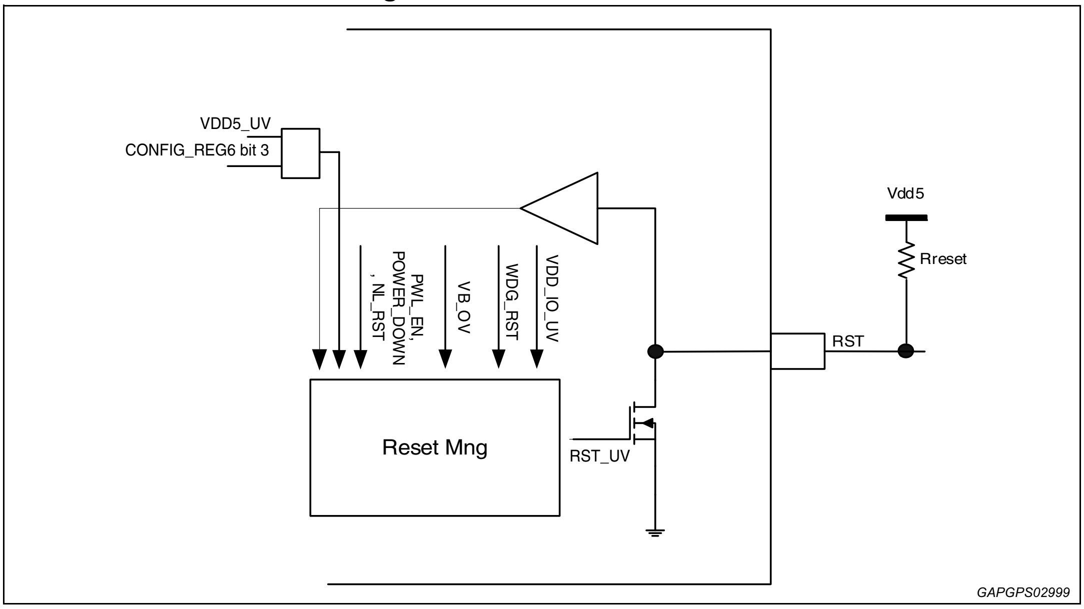
The VDD_IO supply has a voltage monitoring similar to a VDD3V3 monitoring with min-threshold 2.9 V and max-threshold 3.1V for low-voltage monitoring. Low-threshold is adapted to VDD3 supply, even though both 3.3 V and 5 V supplies are possible. The VDD_IO monitoring must be included in the RST logic to create a RST low output in case of VDD_IO low voltage.

Table 8. VDD_IO electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
VDD_IO	I_{VDD_IO}	Input current of VDD_IO pin	VB=14V,all VDD_IO related pin without load	-	-	5	mA
	V_{VDD_IO}	Operation range	-	2.9	-	5.5	V
	V_{VDD_IO}	Maximum rating	-	-0.3	-	19	V
	$V_{VDD\_IO\_UV}$	Under voltage threshold	-	2.9	3.0	3.1	V
	$tf_{\_VDD\_IO\_UV}$	Under voltage filter time	Tested by scan	3	-	10	µs

6.4 Smart reset circuit

Figure 13. Smart reset circuit



6.4.1 Smart reset circuit functionality description

The RST pin is an input/output active when low. As output pin the Smart Reset circuit takes into account several events of the device in order to generate the proper reset signal at RST pin for the microcontroller and for a portion of the internal logic as well. As input pin RST when driven low by external source for more than Trst_flt, it is used to reset the same portion of logic of the device.

The sources of reset are:

- VDD5 undervoltage disabled by MSC CONFIG_REG6 bit3 = high, default is low i.e. enabled
- Power down
- Power latch, KEY_ON
- VB overvoltage
- VDDIO undervoltage
- WDG_RST, query and answer watchdog reset

Smart reset circuit generates RST signal monitoring the VDD5 according to the graph shown below: when VDD5 falls below VDD_UV_LOW threshold for a time longer than TfUV_reset Smart Reset circuit asserts a RST signal (driven low) and the flag CRK_RST is latched and resets every Read Diag operation. When VDD5 recovers to a voltage greater than VDD_UV_HIGH RST pin is deasserted after Td_UV_rst. The RST pin is also asserted at the first power-on phase when the KEY_ON pin goes from low to high, as a consequence of the VDD5 absence.

Smart reset circuit generates an RST signal at power down independently of filtering time and VDD5 voltage level. During power latch mode if NL_RST bit is set and KEY_ON signal goes low to high again (before microcontroller was able to write PWL_EN_N=0), RST_PIN is asserted for time TNL.

Smart reset circuit monitors VB over voltage and generates RST signal if the over voltage lasts more than t_{VBOV2}. When over voltage lasts more than t_{VBOV1} and less than t_{VBOV2}, RST is not asserted, but all drivers are switched off without losing any configuration. In both cases the flag VB_OV is latched and resets every Read Diag operation.

When RST is asserted to reset the µC, also all logic will be reset except logic involved in reset management, power up management, and power down management units. As a consequence all flags are cleared except those set by the smart reset unit, all drivers are disabled except the low battery drivers, all configuration registers are cleared and OUT_DIS bit goes to 1. A more detailed description of the module under reset can be found in the next table. The *Table 9* summaries also relations with other conditions that switch off drivers and regulator.

Table 9. Internal reset

Event	RST pin driven low	Logic under reset	Logic not reset	Power-up/down manager output	Information FLAG
Power down	Yes	Internal registers Interfaces drivers LB interfaces drivers LB internal registers MSC_act CAN & K-LINE & VRS	Smart reset function Power-up/down manager	MRD=OFF VDD5=OFF V3V3=OFF VTRACK1,2=OFF	N/A
Power latch +KEY_ON rising edge	Yes For TNL	Internal registers Interfaces drivers LB interfaces drivers LB internal registers MSC_act CAN & K-LINE & VRS	Smart reset function Power-up/down manager	MRD=ON VDD5=ON V3V3=ON VTRACK1,2=ON	TNL_RST
VDD5 under voltage t<THOLD	Yes	Internal registers Interfaces drivers MSC_act CAN & K-LINE & VRS	LB interfaces drivers LB internal registers Smart reset function Power-up/down manager	MRD=ON VDD5=ON V3V3=ON VTRACK1,2=ON	CRK_RST
VDD5 under voltage t>THOLD	Yes	Internal registers Interfaces drivers LB interfaces drivers LB internal registers MSC_act CAN & K-LINE & VRS	Smart reset function Power-up/down manager	MRD=ON VDD5=ON V3V3=ON VTRACK1,2=ON	VDD5UV_RST

Table 9. Internal reset (continued)

Event	RST pin driven low	Logic under reset	Logic not reset	Power-up/down manager output	Information FLAG
VDD5 over voltage	No	Interfaces drivers MSC_act	Internal registers LB interfaces drivers LB internal registers CAN & K-LINE & VRS Smart reset function Power-up/down manager	MRD=ON VDD5=ON V3V3=ON VTRACK1,2=ON	VDD5_OV
VB over voltage tTBOV1<t<tTBOV2	No	Interfaces drivers LB interfaces drivers MSC_act	Internal registers LB internal registers CAN & K-LINE & VRS Smart reset function Power-up/down manager	MRD=ON VDD5=ON V3V3=ON VTRACK1,2=ON	OV_RST
VB over voltage t>tTBOV2	Yes	Internal registers Interfaces drivers LB interfaces drivers LB internal registers MSC_act CAN & K-LINE & VRS	Smart reset function Power-up/down manager	MRD=ON VDD5=OFF V3V3=OFF VTRACK1,2=OFF	OV_RST
RST driven low externally t<THOLD	Yes	Internal registers Interfaces drivers MSC_act CAN & K-LINE & VRS	LB interfaces drivers LB internal registers Smart reset function Power-up/down manager	Keep state	N/A
RST driven low externally t>THOLD	Yes	Internal registers Interfaces drivers LB interfaces drivers LB internal registers MSC_act CAN & K-LINE & VRS	Smart reset function Power-up/down manager	Keep state	N/A

Table 9. Internal reset (continued)

Event	RST pin driven low	Logic under reset	Logic not reset	Power-up/down manager output	Information FLAG
Software reset sent by the µC through MSC	No	Internal registers Interfaces drivers LB interfaces drivers LB internal registers MSC_act CAN & K-LINE & VRS	Smart reset function Power-up/down manager	MRD=ON VDD5=ON V3V3=ON VTRACK1,2=ON	N/A
MSC activity watch-dog	No	Interfaces drivers	Internal registers LB interfaces drivers LB internal registers CAN & K-LINE & VRS MSC_act Smart reset function Power-up/down manager	MRD=ON VDD5=ON V3V3=ON VTRACK1,2=ON	TRANS_F

Legend:

Internal registers = configuration registers

Interfaces driver = control registers (OUT_DIS), LS/HS drivers, ext-MOS, IGBT

LB internal registers = include dedicated configuration bit for Low battery drivers

LB interfaces driver = control registers (OUT_DIS) + interface drivers logic for Low battery drivers

MSC_ac = MSC activity watch-dog

Smart reset logic = include VDD5 undervoltage and some time counter (TNL, TD_UV_RST, THOLD)

Power-up/down manager = include the logic for regulator control and monitoring and MRD managing.

CAN & K-LINE & VRS

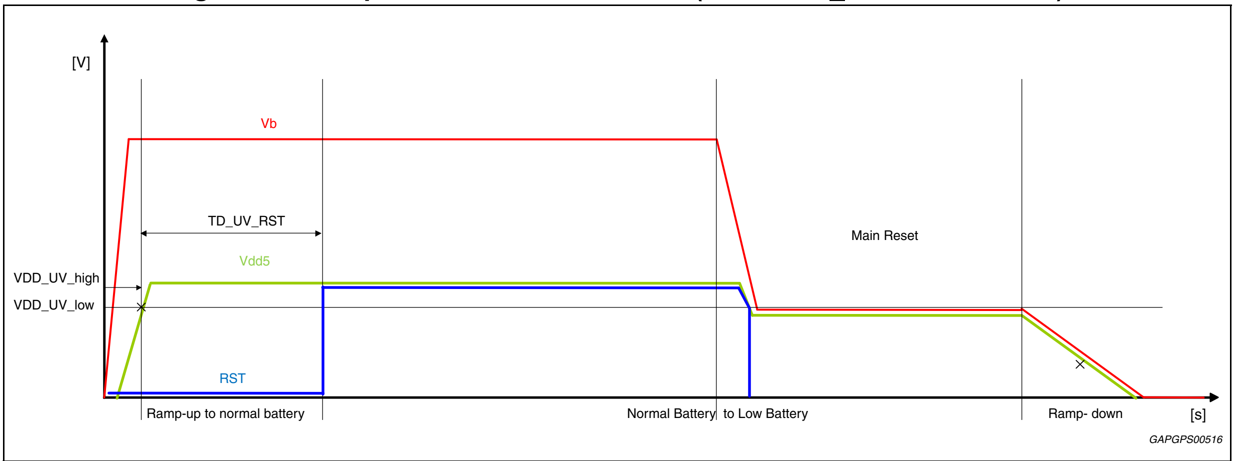
Table 10. RST pin external components required

Pin	Symbol	Parameter	Value	Note
RST	R_{reset}	Pull_up reset reference	4.7 kΩ ± 5 %	-

Table 11. RST pin electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
As output							
RST	VUV_LO	Output low voltage	1 < VDD5 < VDD_UV R_{reset} = 4.7K	-	-	0.4	V
	IUVres_max	Input current	VDD5 = VDD_UV V_{UV_reset} = 0.6 V	1	-	-	mA
	Ilk_{UV_reset}	Input leakage current	V_{UV_reset}> VDD_UV	-	-	1	µA
	TD_UV_RST	Power-on reset delay	Tested by scan	17	-	30	ms
	TNL	Power latch mode exit delay	Tested by scan	1.4	2	2.6	ms
As input							
RST	RST_L	RST Input low voltage	-	-0.3	-	1.1	V
	RST_H	RST input high voltage	-	2.3	-	VDD+0.3	V
	Trst_flt	Reset filter time	Tested by scan	7.5	10	12.5	µs
	R_{RST_PU}	RST pull-up resistor	-	50	-	250	kΩ

Figure 14. RST pin as a function of VDD5 (if CONFIG_REG6 bit3 = Low)



6.4.2 VDD5_UV detection modes

VDD5_UV on RST unmasked without enabling VDD5_UV on MSC-SDO

Mode 1 is the default mode. A VDD5_UV event crates a reset of the whole system which has the advantage that no special undervoltage topics concerning system behavior has to be cared about. Disadvantage concerns requirements for being functional down to low U_{bat}.

Masking VDD5_UV on RST without enabling VDD5_UV on MSC-SDO

Advantage of this **mode 2** is that the system remains fully functional even in a VDD5_UV condition. This is especially interesting for systems whose requirements are to be functional down to low U_{bat}. However it must be considered that also external components are still functional at low U_{bat}. In **mode 2** a VDD_UV condition is only detected by polling the monitoring flag CRK_RST.

Masking VDD5_UV on RST and enabling VDD5_UV output on MSC-SDO

Advantage of this **mode 3** compared to **mode 2** is that a VDD5_UV event is detected fast as no software polling of MSC register flag is necessary. This might be useful for external functions who must be reset fast in case of a VDD_UV event. Advantage compared to **mode 1** is that the µC is not reset and therefore VDD5_UV recovery can be performed faster.

If a VDD5_UV event occurs, MSC-SDO will go to low level. SDO will keep low permanently even if VDD5 recovers. So it is guaranteed that even short VDD5_UV events are not missed. The VDD5_UV condition is detected due to a MSC-SDO low pulse longer than the length of an upstream frame. Upon detection the µC will have to go to its VDD5_UV handling routine. There the µC will at first have to disable output of VDD5_UV on SDO for re-enabling MSC communication and then start polling the CRK_RST flag to check if undervoltage condition has healed or not. When undervoltage condition has healed and CRK_RST flag is back to normal, recovery process can continue and the output of VDD5_UV on MSC-SDO is enabled again for fast detection of an eventual next VDD5_UV condition.

6.5 Thermal shut down

There are 4 temperature sensors:

- OT1 for VTRK1,2
- OT2 for OUT1...10, OUT13…20, OUT21…28, IGN1…4.
- OT3 for MRD
- OT4 for V3V3

When OT1 is higher than $\theta_{junction}$ for t_{OT} time VTRK1,2 are switched off if they are in current limitation.

When OT1 is lower than $\theta_{junction}$ - $\theta_{HYSTERESISv}$ for t_{OT} time, the device should return to normal operation automatically.

When OT2 is higher than $\theta_{junction}$ for t_{OT} time all the OUTx and IGNx are switched off.

When OT2 is lower than junction - $\theta_{HYSTERESISv}$ for t_{OT} time, the device should return to normal operation automatically.

When OT3 is higher than $\theta_{junction}$ for t_{OT} time the MRD is switched off.

When OT3 is lower than $\theta_{junction}$ - $\theta_{HYSTERESISv}$ for t_{OT} time, the device should return to normal operation automatically.

When OT4 is higher than $\theta_{junction}$ for t_{OT} time the V3V3 is switched off if it is in current limitation.

When OT4 is lower than $\theta_{junction}$ - $\theta_{HYSTERESISv}$ for t_{OT} time, the device should return to normal operation automatically.

Thermal warning information from OT1,OT2,OT3,OT4 is latched and communicated by MSC.

Thermal warning information is reset when it is read.

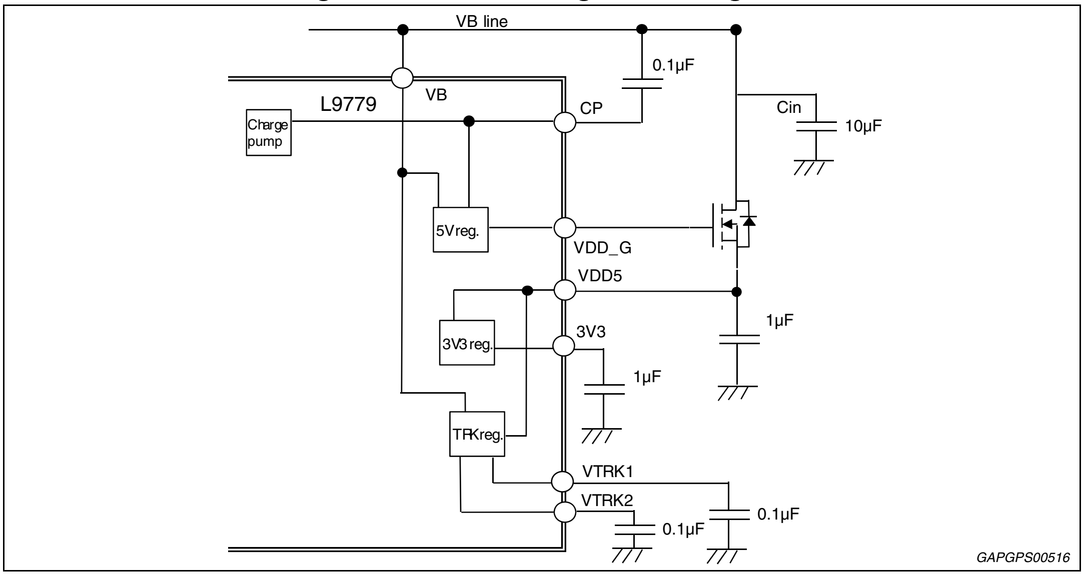
The latch behavior affects only flags bit, while drivers and supplies use the OTx just after the filter to return to normal operation.

Table 12. Temperature information

Parameter	Value	Unit
$\theta_{junction}$	165 to 185	°C
$\theta_{HYSTERESIS}$	5-10	°C
t_{OT}	20	µs

6.6 Voltage regulators

Figure 15. Structure regulators diagram



The structure of regulators is showed in the above figure.

The 5 V voltage is obtained through a linear regulator using an external N-Mos. The precision is ± 2% with Imax = 400 mA. The high precision is obtained with a pre-trimmed reference voltage. The under-voltage condition is monitored through the Smart Reset circuit. In addition there is an overvoltage monitor that after t_VDD5_OV time switches off the drivers except the MRD, OUT13, OUT14, OUT21, OUT25. To switch on again the output it is necessary to send again the START command and to write the CONTROL registers.

It is present a VDD5 over voltage flag, VDD5_OV, that is latched and cleared after reading. This flag does not inhibit the drivers switch on.

The 3.3 V voltage is obtained through a linear regulator. The precision is ± 2% with Imax = 100 mA.

Over-current protection is provided and operates together with thermal sensor OT4.

The condition that switches off the V3V3 is the logic and of both Thermal Warning and Over Current.

The under-voltage condition is monitored and the non latched information is available V3V3_UV bit.

VTRK1, 2 are two voltage regulators in tracking (±20 mV) with the VDD5 voltage for Sensors Supply. They can supply sensors with a Imax = 100 mA. The output voltages can be used in parallel.

VTRK supplies are protected from over voltage due to short to VB with back to back protection and non latched information is available VTRACK_DIAG bit.

Over-current protection is provided as well and operates together with thermal sensor OT1.

The condition that switches off the VTRK 1, 2 is the logic of thermal warning and over current.

The non latched information is available for overload and over temperature conditions in VTRACK_DIAG bit.

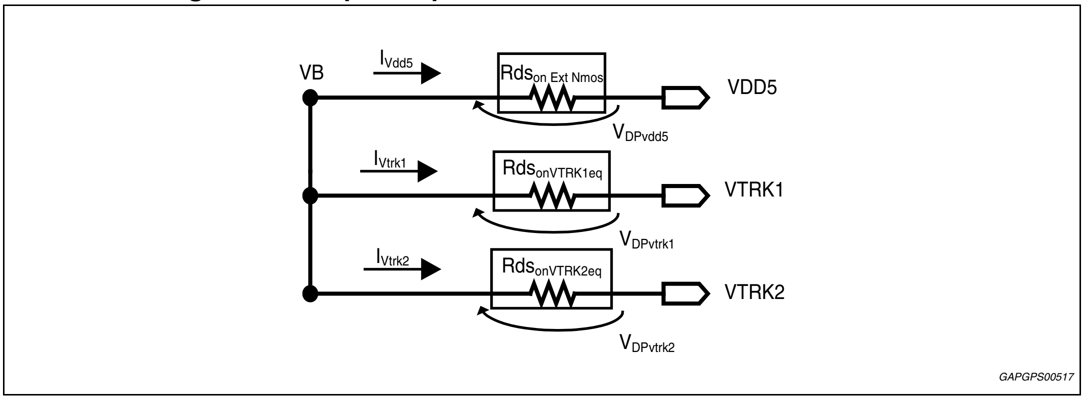
If the VB voltage is lower than regulated VDD5 and higher than 4.15 V the value of VDD5 and VTRK1, 2, could be calculated by the following method:

$V_{DPVDD5} = (Rds_{on\ ExtNmos}) \cdot (I_{VDD5} + I_{V3V3})$

$V_{DPvtrk1} = (Rds_{onVTRK1}) \cdot I_{VTRK1}$

$VDP_{vtrk2} = (Rds_{onVTRK2}) \cdot I_{VTRK2}$

Figure 16. Graphic representation of the calculation method



VDD5 = VB- (V_{DPVdd5})

VTRK 1, 2 = VB- $(V_{DPVtrk1,2})$

While V3V3 keeps working as expected till VB = 4.15 V

Table 13. Voltage regulators external components required

Pin	Symbol	Parameter	Min	Typ	Max	Suggested part number
VTRK1	C_{TRK1}	External VTRK1 capacitor	100 nF	-	1 µF	C1005X7R1C104K--0.1 µF C1608X7R1H104K--0.1 µF
VTRK2	C_{VTRK2}	External VTRK2 capacitor	100 nF	-	1 µF	
VDD5	C_{VDD5}	External VDD5 capacitor	1 µF	-	10 µF	C2012X7R1E105K-- 1 µF C1608X7R1C105K-- 1 µF C3216X7R1H105K--1 µF C3225X7R1E106K--10 µF C3225X7R1C106K--10 µF
	Ext MOS	External N-MOS	-	-	-	IRFZ24NSTRL; STD20NF06L (testing reference); NTD18N06L; HUF76419D3

Table 13. Voltage regulators external components required (continued)

Pin	Symbol	Parameter	Min	Typ	Max	Suggested part number
V3V3	C_{V3V3}	External V3V3 capacitor	1 µF	-	10 µF	C2012X7R1E105K--1 µF C1608X7R1C105K--1 µF C3216X7R1H105K--1 µF C3225X7R1E106K--10 µF C3225X7R1C106K--10 µF
CP	CP	External charge pump capacitor	-20%	100nF	+20%	-

Capacitor legend:

1H → 50 V

1E → 25 V

1C → 16 V

X7R → -40 to 125 °C ±15%

K → -40 to 125 °C ±10%

Note: Others N-MOSFET can be used provided that they have similar threshold voltage and input capacitance; however regulator transient performances may have deviation to be checked.

PCB layout Note: The Cin capacitor on VB line should be put as close as possible to the drain of external MOS. The suggestion PCB layout is as below.

Figure 17. Circuit and PCB layout suggested

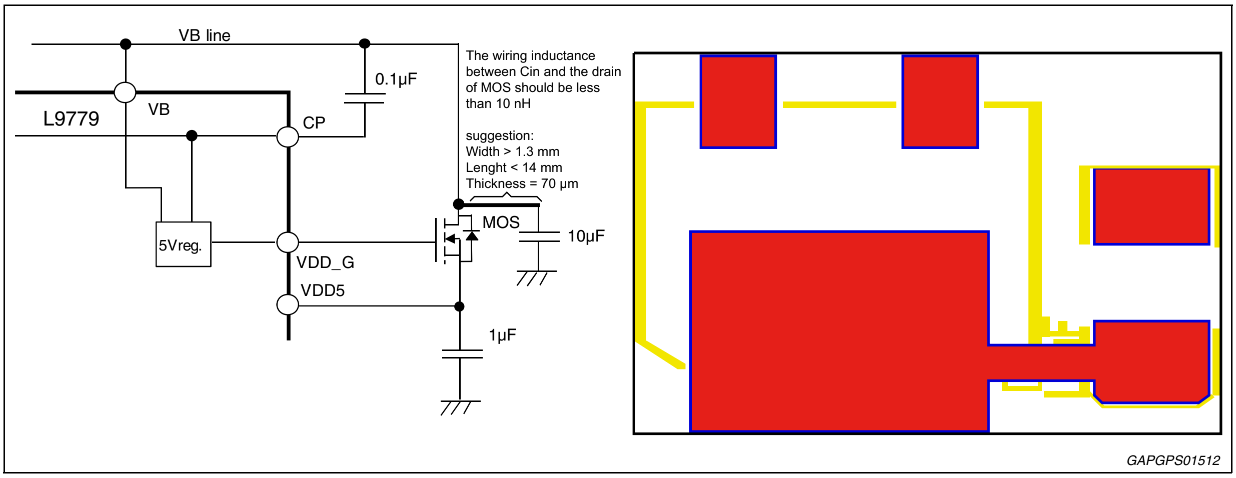


Table 14. VB Power supply electrical characteristics

Pin	Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VB	I_b	Quiescent current from VB pin	VB = 16 V Min. load on regulator outputs(1)	-	-	50	mA
	I_{Leak}	Standby current	VB = 16V; VKEY_ON = GND Guaranteed at room temp.	-	-	10	µA
			VB = 16V; VKEY_ON = GND Guaranteed at hot temp.	-	-	100	
	VB_UV_H	Under voltage switch on threshold high	MRD, Low battery channels switch-on in power up	-	-	4.8	V
	VB_UV_L	Under voltage switch off threshold Low	MRD, Low battery channels switch-off	3.5	-	4.145	
	VB_OV_UP	Over voltage switch off threshold	-	-	-	32	V
	VB_OVh	Over voltage threshold hysteresis	-	0.3	-	1	V
	VB_OV_DOWN	Over voltage switch off threshold	-	28.5	-	-	V
	t_{VBOV1}	Filter time for drivers turn-off	Tested by scan	63	85	107	µs
	t_{VBOV2}	Filter time for regulators turn-off	Tested by scan	11	15	19	ms

1. Min. load on regulator output is Vtrk1 = 1 mA,Vtrk2 = 1 mA,V3V3 = 5 mA,VDD5 is open.(5 mA on V3V3 is from VDD5)

Figure 18. VB overvoltage diagram

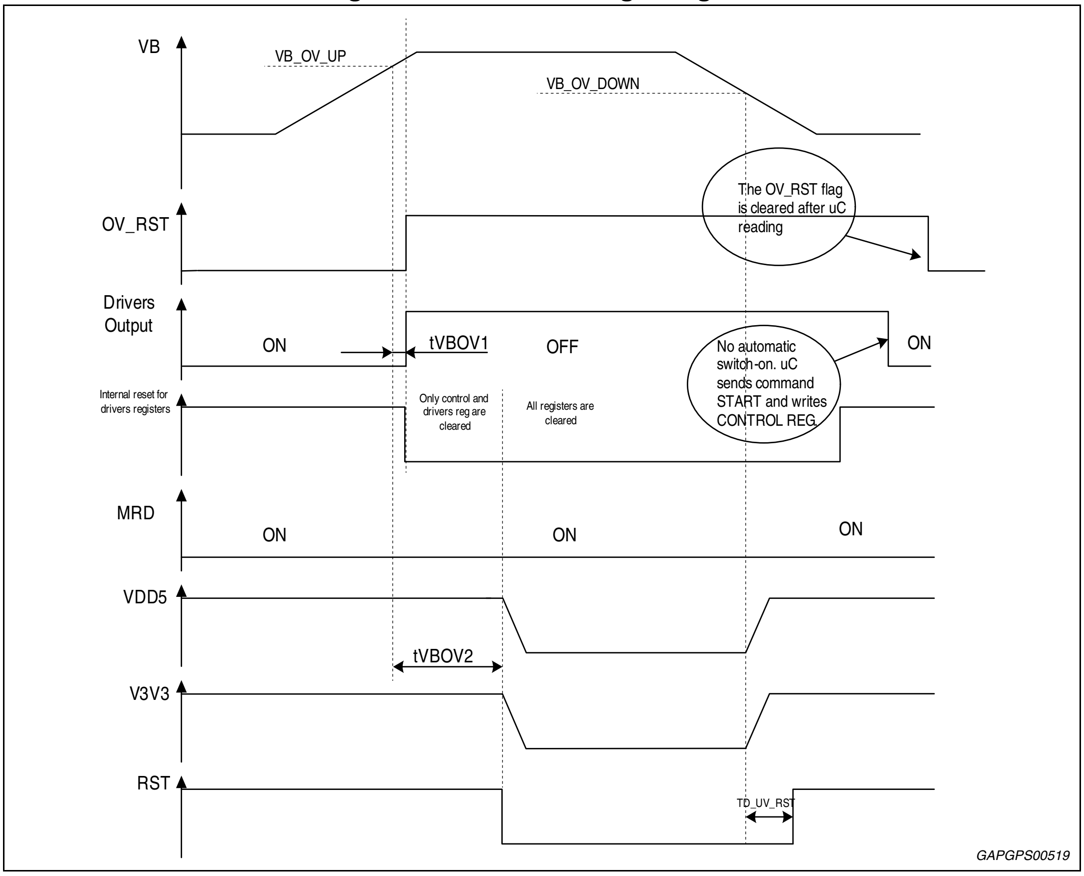


Table 15. Linear 5 V regulator electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
VDD5	VDD5	Output voltage 5 V	I_{VDD5} = 5 to 400 mA V_{bat} = 6-18 V	4.9	5	5.1	V
	VDD5	Transient load regulation	Square wave on VDD5, ΔI_{DD5}= ±100 mA; F_0 = 5 kHz; tr = tf = 0.5 µs; within the output current range NO reset occurs. C_{out} =1 µF C_{out} =10 µF	4.8 4.85	5 5	5.2 5.15	V
	$Sr_{power-up5}$	Output voltage slew rate at power-up	I_{vdd5} = 50 mA; C_{out} =10 µF	5	15	25	V/ms
	V_{line_5}	Line regulation voltage	I_{VDD5} = 5 to 400 mA 6 V < Vb < 18 V	-	-	25	mV
	V_{load_5}	Load regulation voltage		-	-	25	mV
	$VDD5_{Drift}$	Total output VDD5 voltage drift	C_{out} =1 µF (parameter validated in reliability test)	-	-	100	mV

Table 15. Linear 5 V regulator electrical characteristics (continued)

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
VDD5	SVR_{VDD5}	Supply voltage 5 V rejection	C_{out} =10 µF; 4 Vpp, VB mean 9 V, f = 20 kHz	40	-	-	dB
	VDD_OS	Max overshoot at switch on	V_{bat} = 18 V C_{out} = 1 µF R_{out} =100 Ω	-	-	5.2	V
		Max overshoot exiting from cranking	Not tested, is guaranteed by design.	-	-	5.2	V
	Tdelay_REG	-	Tested by scan[1]	0.75	1	1.25	ms
	VDD_UV_low	VDD5 under voltage low threshold	-	4.5	-	VDD5 (typ.) -150mV	V
	VDD_UV_hys	VDD5 under voltage hysteresis	-	50	-	-	mV
	VDD_UV_high	VDD5 under voltage high threshold	-	4.5	-	VDD5 (typ.) -40 mV	V
	VDD_OV_high	VDD5 over voltage high threshold	-	5.8	-	6.2	V
	VDD_OV_hys	VDD5 over voltage hysteresis	-	310	-	460	mV
	VDD_OV_low	VDD5 over voltage low threshold	-	5.5	-	5.9	V
	t_VDD5_OV	VDD5 overvoltage filter time	Tested by scan[1]	75	100	125	µs
	TfUV_Reset	VDD5 under voltage reset filter	Tested by scan[1]	25	50	75	µs
VDD_G	VDD_G	External device voltage at pin VDD_G	VB = 4.5 V	9.5	-	-	V
	Vgs_clamp	External N-DMOS Vgs clamp	Iclamp = 20 mA	-	VDD5 +10	-	V
	Ig	Driver capability	VB = 6-18 V Open loop, VDD5 = VDD_G = 0 V	500	-	-	µA
	Ig_rdson	Driver capability	VB = 4.5 V = VDD_G, open loop, VDD5 = 0 V (charge pump current capability to keep ext MOS in Rdson mode during crank)	160	-	-	µA
-	Fcp	Oscillator frequency	VB = 6-18 V	Fcp (typ.) -5%	9.984	Fcp (typ.) +5%	MHz

1. All tests by scan parameters have 25% tolerance.

6.7 Charge pump

The L9779WD charge pump could be active if the battery supply voltage is smaller than 12 V or be permanently active by setting the capful bit enable or disable. Charge pump provides a permanent voltage of at least 5 V above Ubat when Ubat is higher than 6 V with an external load current at pin CP of 50 μA additional to the L9779WD internal loads.

Once Ubat overvoltage is detected (VB_OV_th > 28 V), the charge pump will be switched off automatically no matter the cp_off bit status.

Figure 19. VDD5 overvoltage diagram

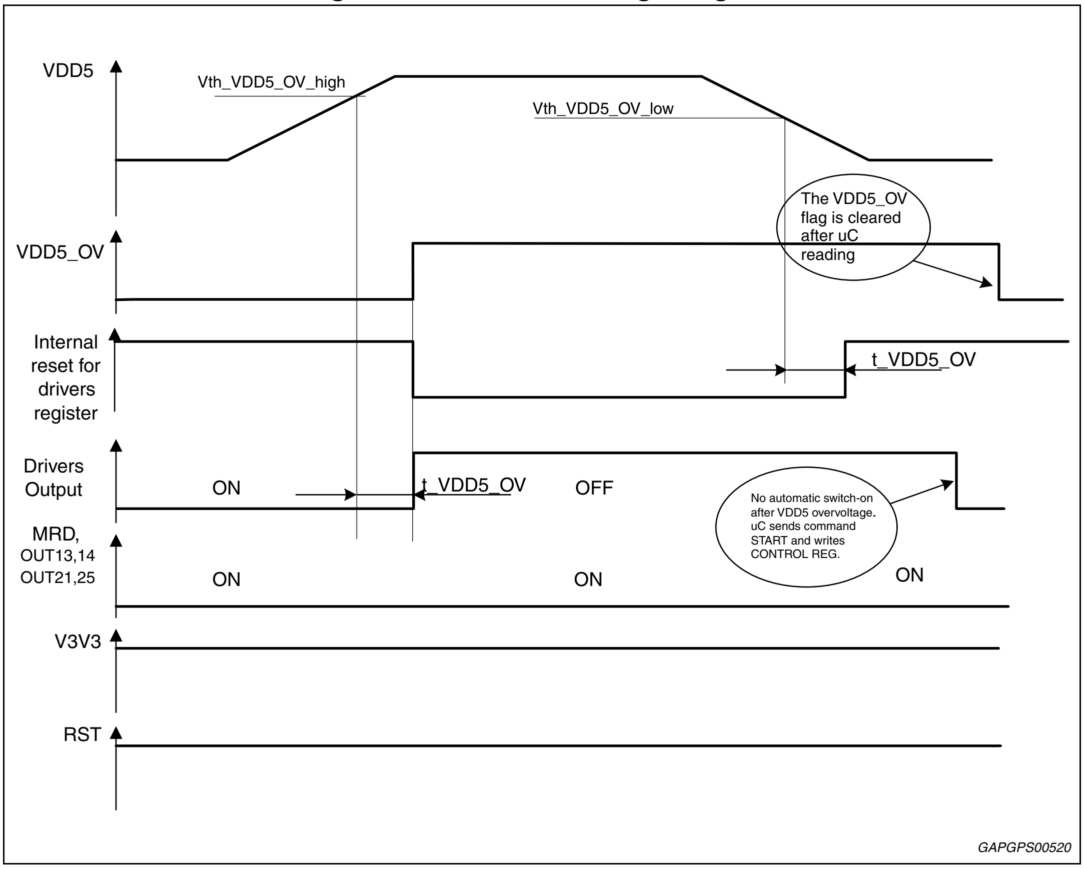


Figure 20. VDD5 vs battery: ramp-up diagram

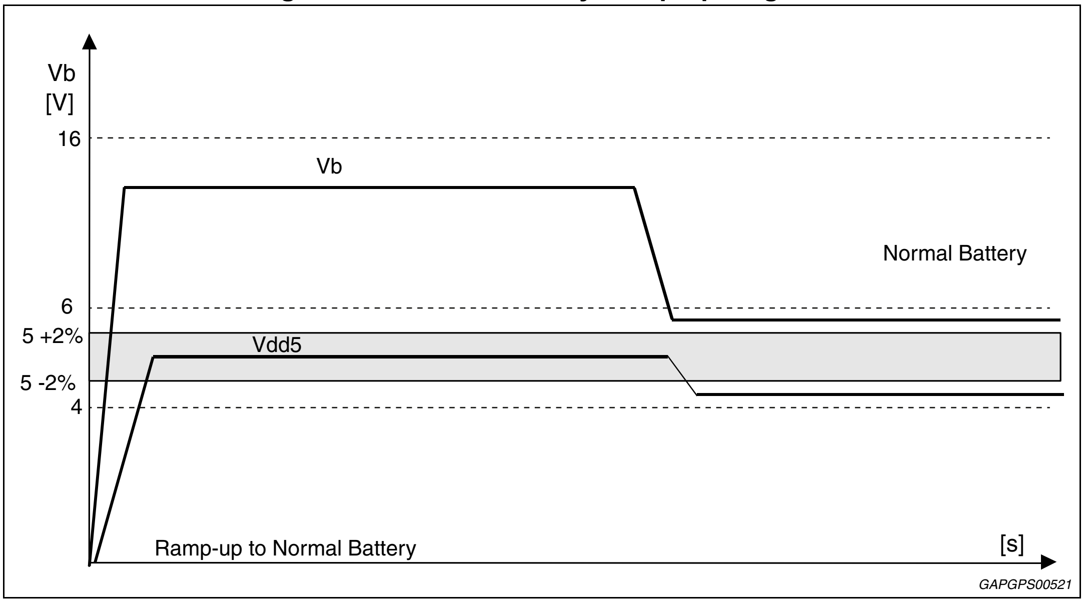


Figure 21. VDD5 vs battery (ramp-down diagram)

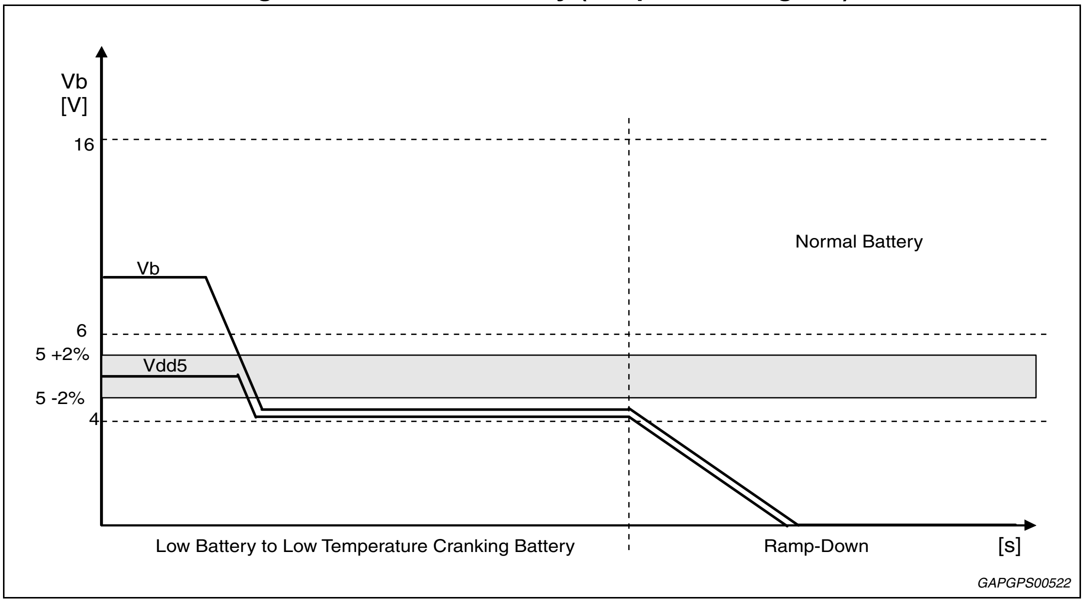


Table 16. Linear 3.3 V regulator electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V3V3	V3V3	Output voltage 3.3 V	IV3V3 = 5-100 mA VB = 6-18 V	3.23	3.3	3.36	V
	V3V3	Output voltage 3.3 V	Square wave on V3V3, ΔIV3V3 = ±20 mA; f0 = 5 kHz; tr = tf = 0.5µs; within the output current range	3.2	3.3	3.36	V
	$Sr_{power-up5}$	Output voltage slew rate at power-up	I_{V3V3} = 12.5 mA C_{out} = 4.7 µF	4	12	20	V/ms

Table 16. Linear 3.3 V regulator electrical characteristics (continued)

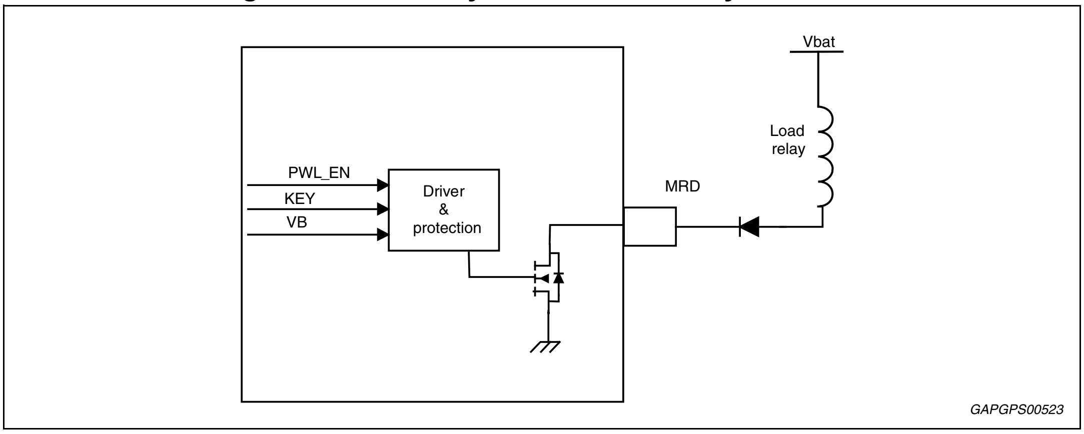
Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V3V3	I_{V3V3_MAX}	Output current limitation V3V3	V3V3 = 3 V VB = 6-18 V	200	-	500	mA
	V_{line_3}	Line regulation voltage	IV3V3 = 5-100 mA 6V < VB < 18 V	-	-	25	mV
	V_{load_3}	Load regulation voltage	IV3V3 = 5-100 mA 6V < VB < 18 V	-	-	25	mV
	$V3V3_{Drift}$	Total output 3V3 voltage drift	C_{out} = 4.7 µF (parameter validated by reliability test)	-	-	100	mV
	$SVRV_{3V3}$	Supply voltage 3.3 V rejection	C_{out} = 4.7 µF; 4 Vpp, VB mean 9 V, f = 20 kHz	40	-	-	dB
	V_{drop_out}	-	VDD5 = 3.3 V; IV3V3 =100 mA	-	-	200	mV
	V3V3_OS	Max overshoot at switch on	-	-	-	3.45	V
	-	Max overshoot exiting from cranking*[1]	Not tested, it is guaranteed by design	-	-	3.45	V
	TD_Start_V3V3	Delay between VDD5> VDD_UV_high and V3V3 switch on	Tested by scan	-	-	1	ms

Table 17. 5V tracking sensor supply electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
VTRK_1 VTRK_2	ΔVTRK	Output voltage tracking error	VB = 6-18 V 1 mA < I_{VTRK} < 100 mA	VDD5 -20	-	VDD5 +20	mV
	I_{VTRK_MAX}	Output current limitation VTRK1,2	VTRK = -1V	160	-	400	mA
	V_{LINE_trk}	Line regulation voltage VTRK	VB = 6-18 V 1 mA < I_{VTRK} < 100 mA Ctrk = 1 µF	-	-	20	mV
	V_{load_trk}	Load regulation voltage VTRK	VB = 6-18 V 1 mA < I_{VTRK} < 100 mA Ctrk = 1 µF	-	-	20	mV
	I_{sink_VTRK}	Short circuit reverse current	Output shorted to Vbat +2 V	-	-	4	mA
	I_{TH_UVTRK}	Over current threshold VTRK	VB = 6-18 V	101	-	I_{VTRK_MAX}	mA
	V_{TH_OVTRK}	V threshold over voltage VTRK	Ramp on tracking output	5.3	-	-	V
	$SVR_{\_VTRK}$	Supply voltage tracking rejection	C_{out} = 4.7 µF; VDD5 = 5 V 4 Vpp, VB mean 9 V, f = 20 kHz	40	-	-	dB
	Rds_{on}	-	VB = 4.8 V; $I_{VTRK1,2}$ = 100 mA	-	-	3600	mΩ
	Vos	Over shoot during power up	Cload ≥ 470 nF tested with 1 µF	-	-	5.5	V
			Cload < 470 nF tested with 100 nF	-	-	6	V
	V_{ov_filter}	Over voltage filter time	Test by scan	48	64	80	µs

6.8 Main relay driver

Figure 22. Main relay driver controlled by L9779WD



6.8.1 Main relay driver functionality description

Main relay driver MRD is controlled by L9779WD depending on the voltage levels at pins KEY_ON, VB and the power latch mode set by the µC as described in the previous sections.

The output stage MRD for main-relay-control is realized with a low-side-switch with integrated clamping at VCL voltage realized with a zener diode.

When VB is present (VB>VB_LV) the MRD driver is protected, in ON condition, against the over temperature fault. When the temperature is above junction the MRD is switched off. After $\theta_{HYSTERESIS}$ the MRD returns to normal operation automatically.

In case of MRD short to battery without VB present i.e. during start-up sequence, when the current exceeds the IOVC value, this pin will be switched off after a certain filter time TFILTEROVC; to turn on MRD again it is necessary a high to low transition on KEY_ON pin. Refer to scenario 5 (*Figure 29*).

In case of MRD short to battery with VB present i.e. during normal mode, when the current exceeds the IOVC value, this pin will be switched off after a certain filter time TFILTEROVC; the uC can try to turn on the MRD using the command MRD_REACT until the VB voltage is above VB_UV. Below this threshold the MRD retries to switch on, then if the fault is still present the MRD switches off and to turn it on again it is necessary a high to low transition on KEY_ON pin. Refer to scenario 6-7-8 (*Figure 30*, *31* and *32*).

In every condition the bit MRD_OVC reports that the MRD is currently off due to a previous over current event.

Diagnosis of MRD short to ground may be done as described in the power up/down management unit, switching off the MRD keeping alive all other regulators.

Table 18. Main relay driver electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
MRD	R_{DS-on}	Drain –source resistance	I_{load} = 0.4 A; Vbat = 0 & 13.5 V	-	-	2.4	Ω
	$IOUT_{lk\ MRD}$	Output leakage current	Vpin = 13.5 V; Vbat = 0 & 13.5 V	-	-	10	µA
	VS/R	Voltage S/R on/off	R = 21 Ω, C = 10 nF; Vbat = 0 & 13.5 V	1	-	10	V/µs
	Vcl	Output clamping voltage	Vbat = 0 & 13.5 V	42	-	55	V
	Imax	Output current	Design info		-	0.6	A
	IOVC	Over current threshold	Vbat = 0 & 13.5 V	0.7	-	1.4	A
	TFILTEROVC	Over current filtering time	Test by SCAN	5.25	7	8.75	us
	VB_UV	VB threshold for MRD active	Vbat = 0 & 13.5 V	-	-	4.15	V
	$PW_{clampSP}$	Clamp single pulse ATE test	I_{load} = 0.5 A; single pulse	-	-	15	mJ
	$PW_{clampRP}$	Clamp repetitive pulses reliability test	I_{load} = 0.25 A Freq =1 Hz; 1 Mpulse	-	-	4	mJ

6.8.2 MRD scenarios

Figure 23. Scenario 1a: Standard on/off MRD driver with NO power latch mode bit PSOFF = 0

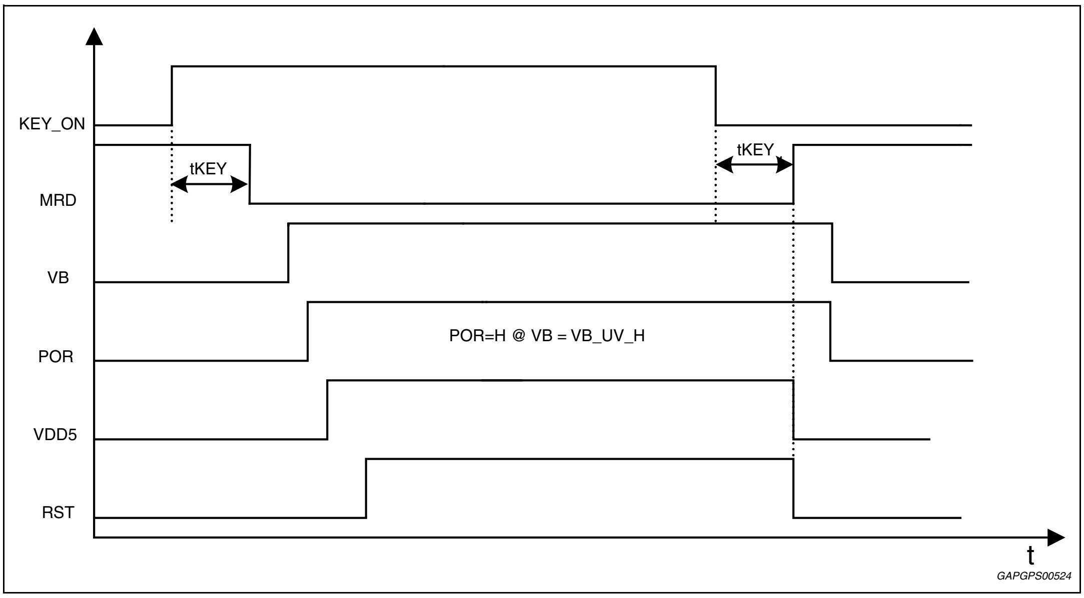


Figure 24. Scenario 1b: Standard on/off MRD driver with NO power latch mode bit PSOFF = 1

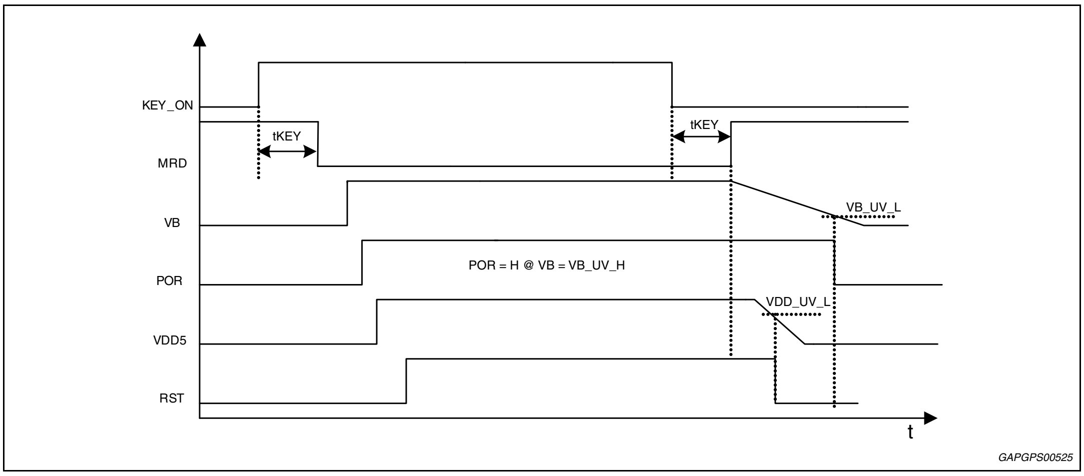


Figure 25. Scenario 2: Standard on/off MRD driver with power latch mode bit PSOFF = 0

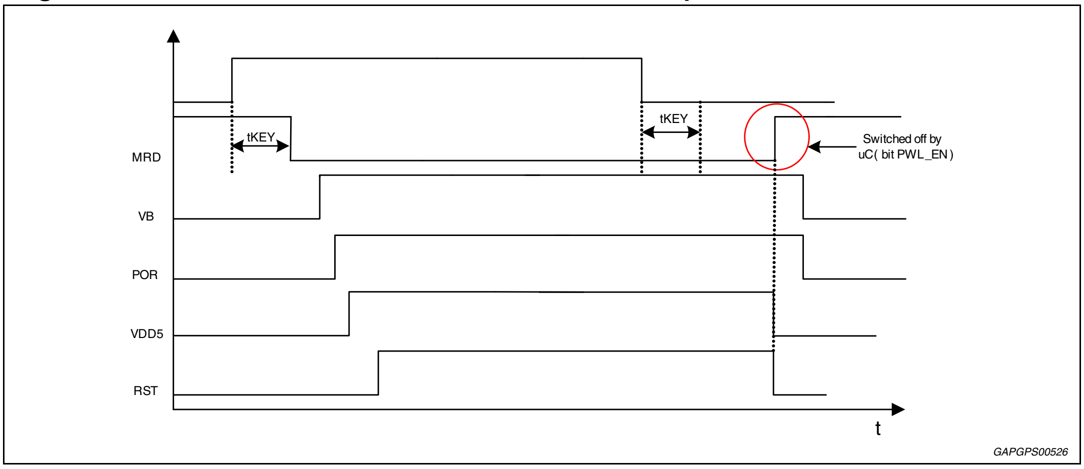


Figure 26. Scenario 3a: Deglitch concept on KEY_ON at start-up

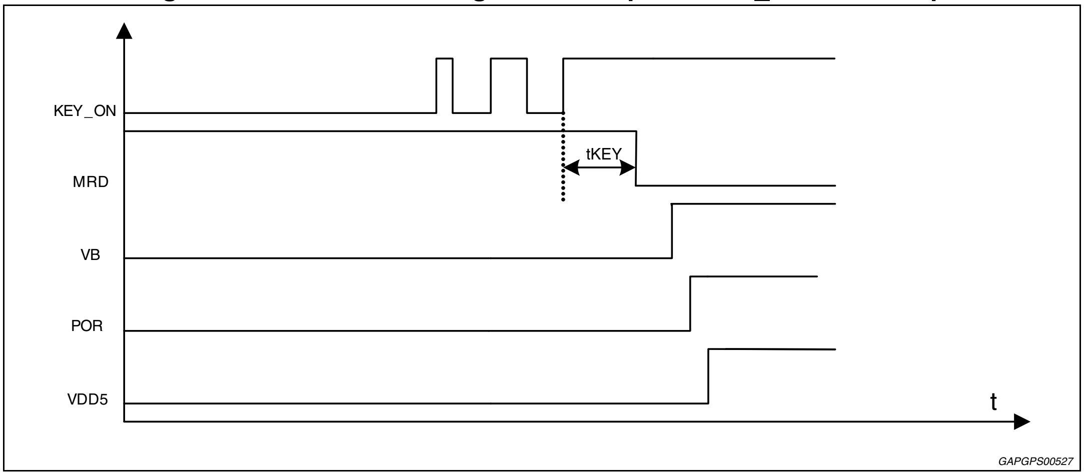


Figure 27. Scenario 3b: Deglitch concept on KEY_ON during ON phase

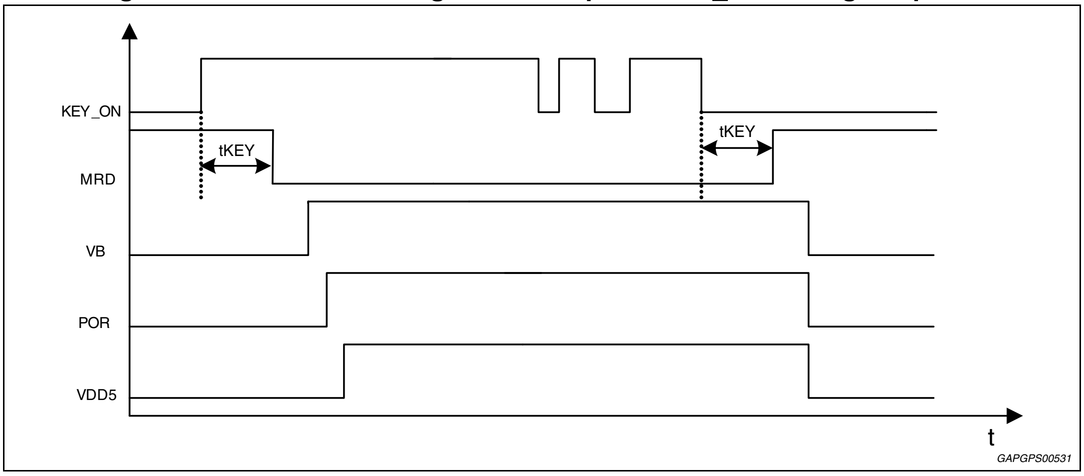


Figure 28. Scenario 4: Non standard on, KEY_ON removed before VB present

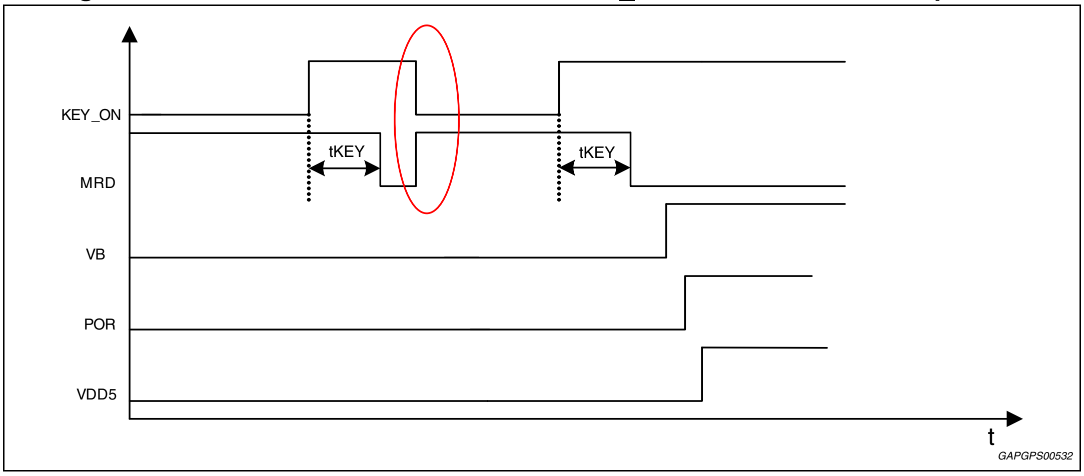


Figure 29. Scenario 5: MRD overcurrent without VB

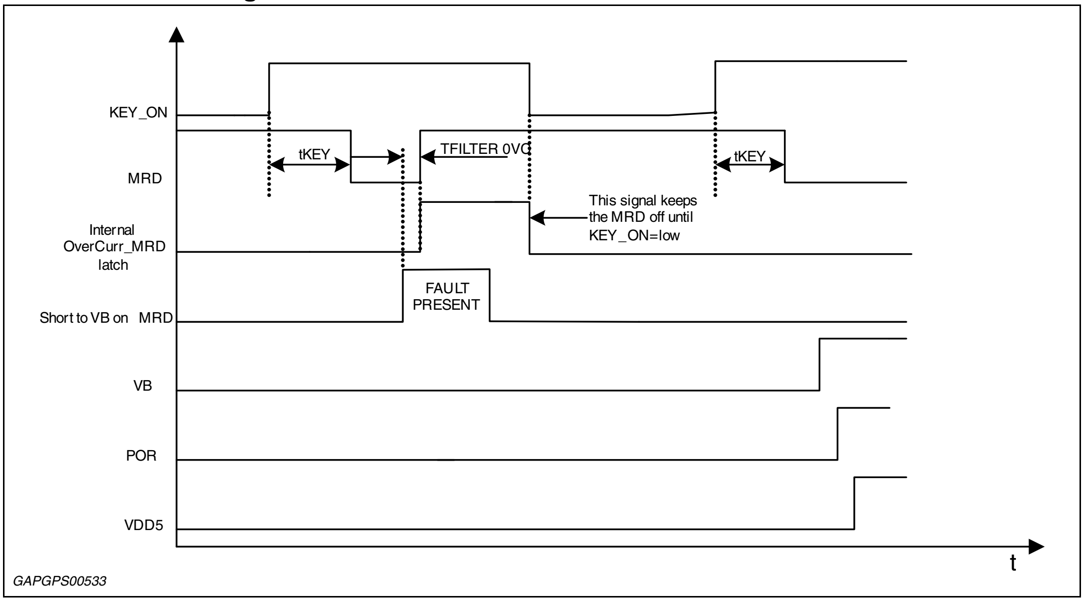


Figure 30. Scenario 6: permanent MRD overcurrent with VBPOR restart

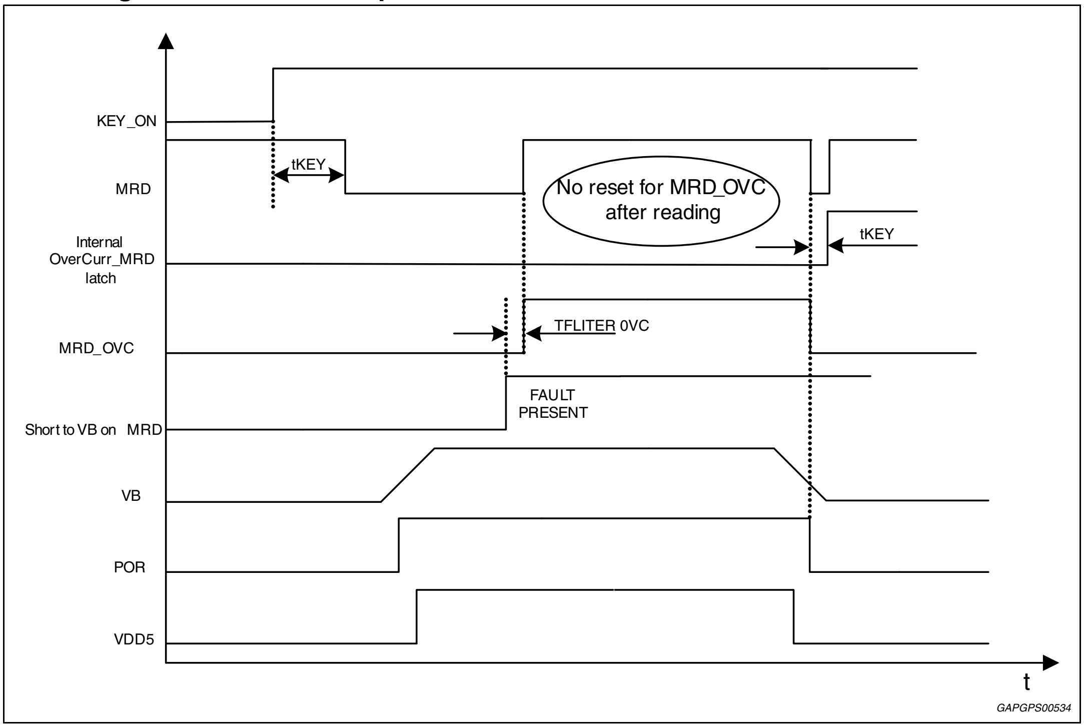


Figure 31. Scenario 7 (temporary MRD overcurrent with VB POR restart)

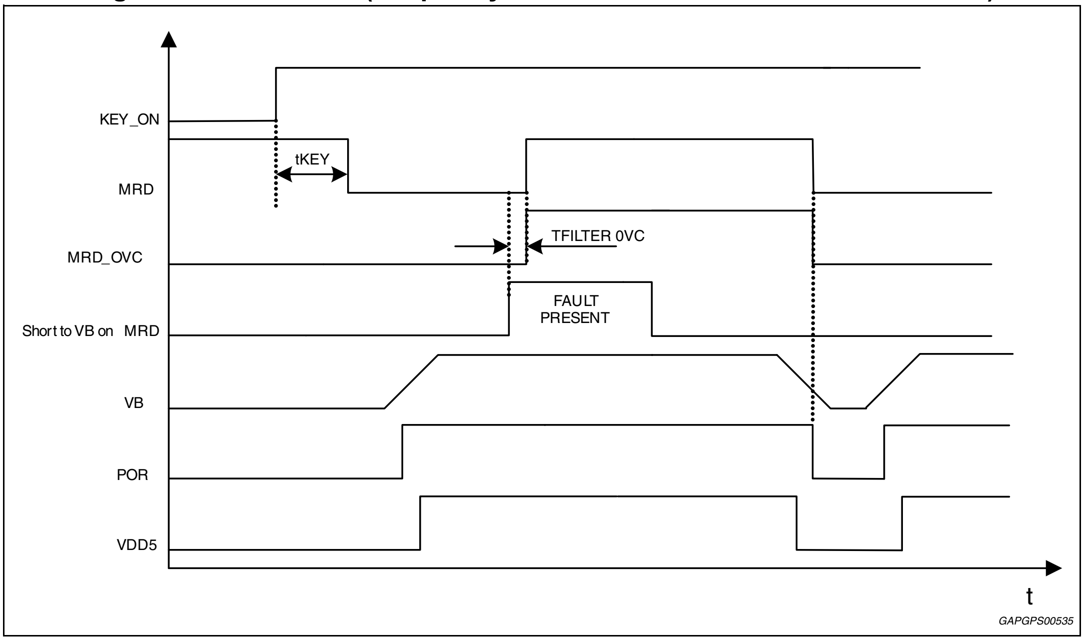
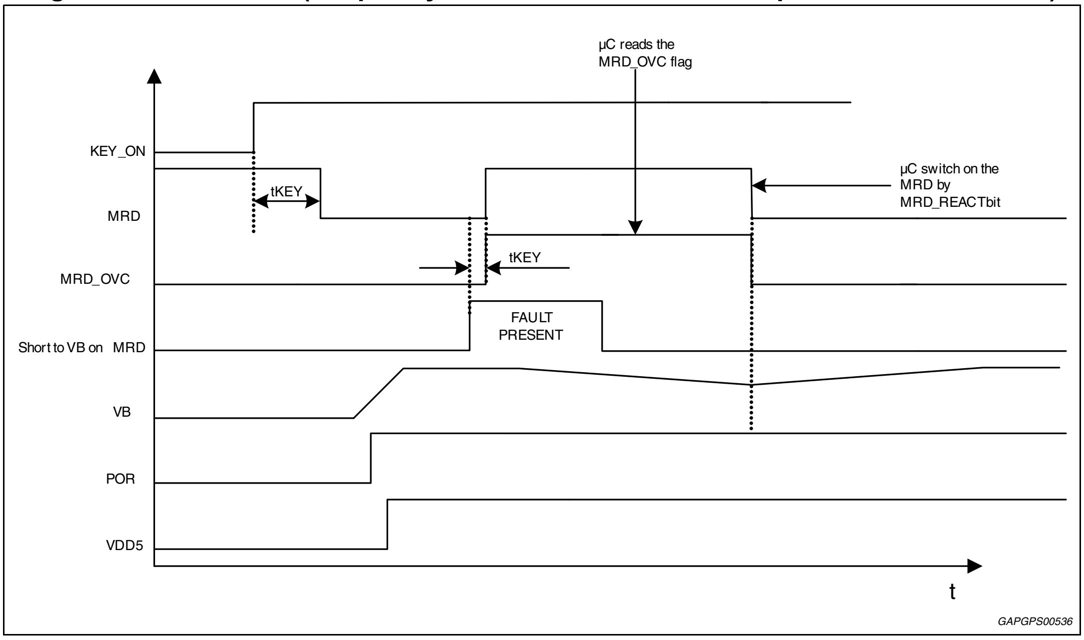


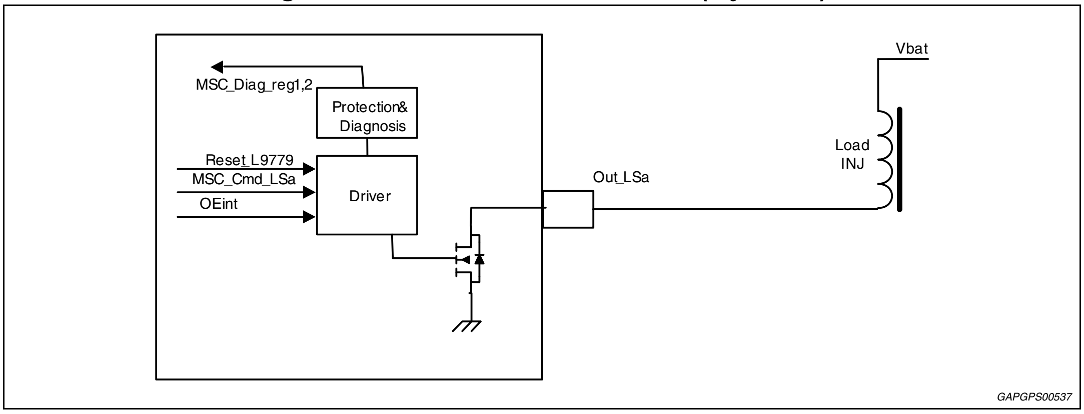
Figure 32. Scenario 8 (temporary MRD overcurrent with VB µC commands restart)



6.9 Low-side switch function (LSa, LSb, LSd)

6.9.1 LSa function OUT 1 to 5 (Injectors)

Figure 33. LSa function OUT 1 to 5 (Injectors)



LSa functionality description

LSa are 5 protected low-side drivers with diagnosis and over current protection circuit.

They are driven via MicroSecond Channel interface.

The maximum current for OUT1 to 4 is 2.2 A while for OUT5 is 3 A.

When Reset_L9779 signal or OUT_DIS bit is asserted OUT_LSa is switched off.

When an over current fault occurs, the driver switches off with faster slew rate in order to reduce the power dissipation.

The turn on/off time is fixed and the slew-rate is controlled.

Max Cload = 20 nF.

Table 19. LSa electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT 1 to 5	$R_{DS\text{-}on\ LSa}$	Drain source resistance	I_{load} = 1.25 A	-	-	0.72	Ω
	$IOUT_{lk}$	Output leakage current	Vpin = 13.5 V	-	-	10	µA
	VS/R	Voltage S/R on/off	Load: 8 Ω, 10 nF From 80% to 30% of V_{OUT}	2	-	6	V/µs
	VS/R GateKill	FAST VR/S off when an OVC fault happens	Load: 8 Ω, 10 nF From 80% to 30% of V_{OUT}	5	-	20	V/µs
	$T_{Turn\text{-}on\_ LSa}$	Turn-on delay time	From command to 80% VOUT, Load: 8 Ω, 10 nF	-	-	6	µs
	$T_{Turn\text{-}off\_ LSa}$	Turn-off delay time	From command to 30% VOUT, Load: 8 Ω, 10 nF	-	-	6	µs
	Vcl	Output clamping voltage	I_{load} = 1.25 A	53	58	63	V
	$PW_{clampSP}$	Clamp single pulse ATE test	I_{load} = 1.25 A single pulse	-	-	25	mJ

Table 19. LSa electrical characteristics (continued)

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT 1 to 4	$PW_{clampRP}$	Clamp repetitive pulses Freq = 50 Hz (to be verified)	Tc ≤ 30°C; I_OUT_n ≤ 1.8 A 13 Mio cycles	-	-	7.5	mJ
			Tc ≤ 65°C; I_OUT_n ≤ 1.4 A 130 Mio cycles	-	-	4	
			Tc ≤ 80°C; I_OUT_n ≤ 1.4 A 214 Mio cycles	-	-	4	
			Tc ≤ 100°C; I_OUT_n ≤ 1.4 A 175 Mio cycle	-	-	4	
			Tc ≤ 115°C; I_OUT_n ≤ 1.4 A 45 Mio cycle	-	-	4	
			Tc ≤ 130°C; I_OUT_n ≤ 1.0 A 65 Mio cycle	-	-	3	
			Tc ≤ 145°C; I_OUT_n ≤ 1.0 A 6 Mio cycle	-	-	3	
	Reverse voltage	Body diode reverse current voltage drop (valid for OUT5 also)	I = -2.2 A	-0.5	-	-1.2	V
OUT5	$PW_{clampSP}$	Clamp single pulse	Iload = 1.25 A single pulse	-	-	25	mJ
	$PW_{clampRP}$	Clamp repetitive pulses Freq = 30 Hz	Tc < 30°C; I_OUT5 < 0.7 A 21 Mio cycles	-	-	17	
			Tc < 65°C; I_OUT5 < 0.7 A 70 Mio cycles	-	-	14	
			Tc < 80°C; I_OUT5 < 0.7 A 115.5 Mio cycles	-	-	14	
			Tc < 90°C; I_OUT5 < 0.7 A 63 Mio cycles	-	-	14	
			Tc < 100°C; I_OUT5 < 0.7 A 31.5 Mio cycles	-	-	14	
			Tc < 105°C; I_OUT5 < 0.7 A 10.5 Mio cycles	-	-	14	
			Tc < 110°C; I_OUT5 < 0.7 A 7 Mio cycles	-	-	14	
			Tc < 115°C; I_OUT5 < 0.7 A 5.95 Mio cycles	-	-	14	
			Tc < 120°C; I_OUT5 < 0.7 A 5.25 Mio cycles	-	-	12	
			Tc < 125°C; I_OUT5 < 0.7 A 4.9 Mio cycles	-	-	12	
			Tc < 130°C; I_OUT5 < 0.7 A 4.55 Mio cycles	-	-	12	

Table 19. LSa electrical characteristics (continued)

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT5	$PW_{clampRP}$	Clamp repetitive pulses Freq = 30 Hz	Tc < 135°C; I_OUT5 < 0.7 A 4.55 Mio cycles	-	-	12	mJ
			Tc < 140°C; I_OUT5 < 0.7 A 3.5 Mio cycles	-	-	12	
			Tc < 145°C; I_OUT5 < 0.7 A 3.5 Mio cycles	-	-	12	

Table 20. LSa diagnosis electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT 1 to 5	$R_{open\ load}$	Min resistor value open load detection	Not tested	500	-	-	kΩ
	I_{max}	Output current	Not tested	-	2.2	-	A
	I_{OVC}	Over current threshold	-	3	-	6	A
	$T_{FILTEROVC}$	Over current filtering time	Tested by scan	2	3	4	µs
	$T_{FILTERdiaggoff}$	Filtering open load and short to gnd diag. off	Tested by scan	35	50	65	µs
	T_{d_mask}	Diagnosis Mask time after switch-off	Tested by scan	300	-	500	µs
	V_{HVT}	Open load threshold voltage	-	$V_{Outopen}$ +120mV	-	3	V
	$V_{Outopen}$	Open load output voltage	Open load condition	2.3	-	2.7	V
	V_{LVT}	Output short-circuit to GND voltage range threshold	-	1.9	-	$V_{Outopen}$ -200mV	V
	I_{OUT_PD}	Output diagnostic pull down current Off state	Vpin = 5 V	50	-	110	µA
OUT 1 to 5	I_{OUT_PU}	Output diagnostic pull up current Off state	Vpin = 1.5 V	110	160	210	µA
	I_{topen}	Open load threshold current	-	30	-	90	µA

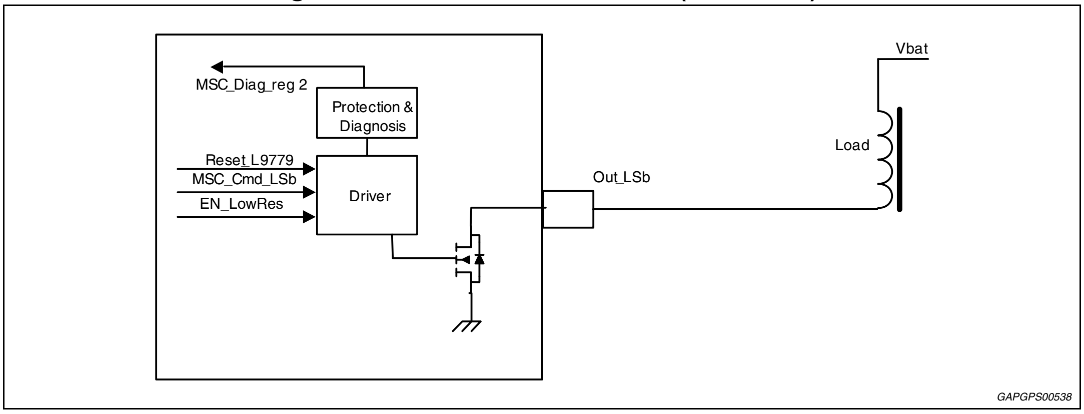
For OUT 5 only the following parameters are different with respect to OUT1 to 4.

Table 21. LSa diagnosis electrical characteristics (OUT 5)

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT 5	I_{max}	Output current	Not tested	-	3	-	A
	I_{OVC}	Over current threshold	-	3.7	-	6.9	A

6.9.2 LSb function OUT6, 7 (O2 heater)

Figure 34. LSb function OUT6, 7 (O2 heater)



LSb functionality description

LSb are 2 protected low-side drivers with diagnosis and over current protection circuit.

They are driven via MicroSecond Channel interface.

The turn on/off time is fixed and the slew-rate is controlled.

When an over current fault occurs, the driver switches off with faster slew rate in order to reduce the power dissipation.

The turn on/off time is fixed and the slew-rate is controlled.

Max Cload = 20 nF.

Table 22. LSb electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT 6, 7	$R_{DS\text{-}on\ LSb}$	Drain source resistance	T = -40°C, I_{load} = 3 A	0.05	-	0.16	Ω
			T = 25°C, I_{load} = 3 A	0.13	-	0.23	Ω
			T = 130°C, I_{load} = 3 A	0.21	-	0.47	Ω
	I_{OUTlk}	Output leakage current	-	-	-	10	µA
	VS/R	Voltage S/R on/off	R = 4.5 Ω, C = 10 nF From 80% to 30% of V_{OUT}	0.5	-	2.5	V/µs
	VS/R GateKill	FAST VR/S off when an OVC fault happens	Load: 8 Ω, 10 nF From 80% to 30% of V_{OUT}	5	-	20	V/µs
	$T_{Turn\text{-}on\_ LSb}$	Turn-on delay time	From command to 80% V_{OUT} Load: 4.5 Ω, 10 nF	-	-	7.5	µs
	$T_{Turn\text{-}off\_ LSb}$	Turn-off delay time	From command to 20% V_{OUT} Load: 4.5 Ω, 10 nF	-	-	7.5	µs
	V_{cl}	Output clamping voltage	I_{load} = 1.5 A	41	45	49	V
	$PW_{clampSP}$	Clamp single pulse ATE test	I_{load} = 1.5 A; single pulse	-	-	25	mJ

Table 22. LSb electrical characteristics (continued)

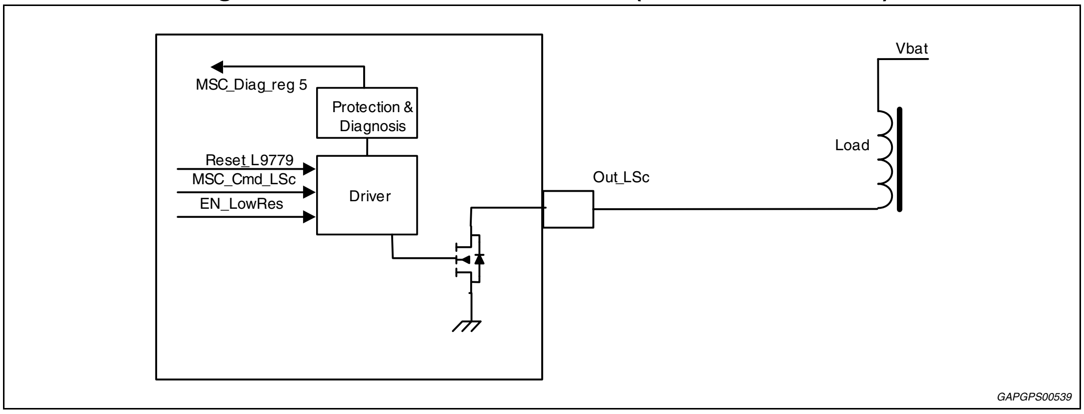
Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT 6, 7	$PW_{clampRP}$	Clamp repetitive pulses Freq = 5 Hz Reliability Test	Tc ≤ 30 °C; I_OUT_n ≤ 1.8 A 13 Mio cycles	-	-	7.5	mJ
			Tc ≤ 65°C; I_OUT_n ≤ 1.4 A 130 Mio cycles	-	-	4	
			Tc ≤ 80°C; I_OUT_n ≤ 1.4 A 214 Mio cycles	-	-	4	
			Tc ≤ 100°C; I_OUT_n ≤ 1.4 A 175 Mio cycle	-	-	4	
			Tc≤ 115°C; I_OUT_n ≤ 1.4 A 45 Mio cycle	-	-	4	
			Tc ≤ 130°C; I_OUT_n ≤ 1.0 A 65 Mio cycle	-	-	3	
			Tc ≤ 145°C; I_OUT_n ≤ 1.0 A 6 Mio cycle	-	-	3	
	Reverse voltage	Body diode reverse current voltage drop	I = -5 A	-1.3	-1	-0.5	V

Table 23. LSb diagnosis electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT6, 7	I_{max}	Output current	Not tested	-	5	-	A
	I_{OVC}	Over current threshold	T = -40°C	8.6	-	12.4	A
			T = 25°C	8	-	11.2	A
			T = 130°C	7.8	-	9.9	A
	$T_{FILTEROVC}$	Over current filtering time	Tested by scan	1.5	-	2.5	µs
	$T_{FILTERdiaggoff}$	Filtering open load and short to GND diag. off	Tested by scan	7	-	13	µs
	T_{d_mask}	Diagnosis mask delay after switch-off	Tested by scan	300	-	500	µs
	V_{HVT}	Open load threshold voltage	-	$V_{Outopen}$ +120mV	-	3	V
	$V_{Outopen}$	Open load output voltage	Open load condition	2.3	-	2.7	V
	V_{LVT}	Output short-circuit to GND threshold voltage	-	1.9	-	$V_{Outopen}$ -200mV	V
	I_{OUT_PD}	Output diagnostic pull down current OFF STATE	Vpin = 5 V	50	-	110	µA
	I_{OUT_PU}	Output diagnostic pull up current OFF STATE	Vpin = 1.5 V	-210	-	-108	µA
	I_{topen}	Open load threshold current	-	30	-	90	µA

6.9.3 LSc function OUT19, 20 (low current drivers)

Figure 35. LSc function OUT19, 20 (low current drivers)



LSc functionality description

LSc are 2 protected Low-Side drivers with diagnosis and over current protection circuit. The off state diagnosis (open load and short to GND) detection can be switched off by OFF_LCDR bit.

They are driven via MicroSecond Channel.

When Reset_L9779 signal or OUT_DIS bit is asserted OUT_LSc is switched off.

When an over current fault occurs, the driver switches off with faster slew rate in order to reduce the power dissipation.

The turn on/off time is fixed. During turn-off the slope is fixed by external RC load.

Max Cload = 20 nF.

Table 24. LSc electrical characteristics

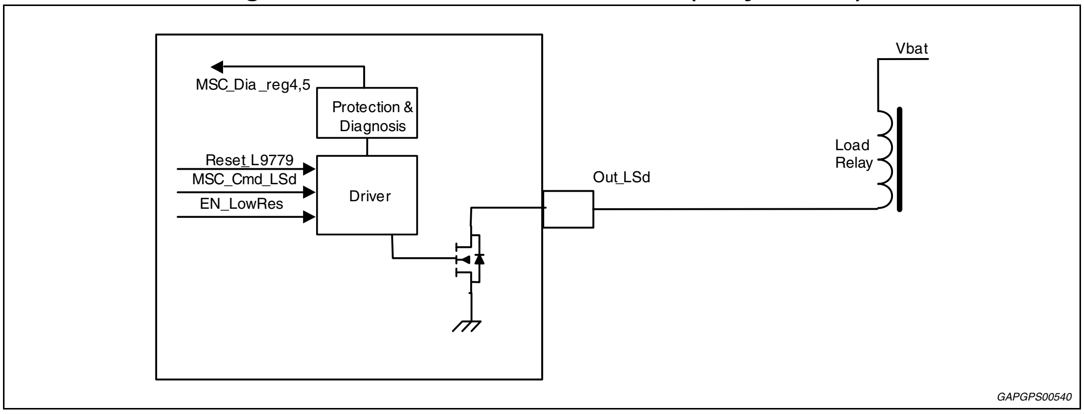
Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT 19, 20	$R_{DS\text{-}on\ LSc}$	Drain source resistance	Iload = 50 mA	-	-	20	Ω
	$IOUT_{lk}$	Output leakage current	Vpin = 13.5 V @hot	-	-	10	µA
	$T_{Turn\text{-}on\_LSb}$	Turn-on delay time	From command to 80% V_{OUT}; Load: 250 Ω, 10 nF	-	-	5	µs
	$T_{Turn\text{-}off\_LSb}$	Turn-off delay time	From command to 30% V_{OUT}; Load: 250 Ω, 10 nF	-	-	5	µs
	V_{cl}	Output clamping voltage	I_{load} = 50 mA	40	45	50	V
	$PW_{clampSP}$	Clamp single pulse ATE test	-	-	-	3.5	mJ
	$PW_{clampRP}$	Clamp repetitive pulses Reliability Test	Tc ≤ 145 °C; I_OUT_n ≤ 0.03 A 0.5 Mio cycles	-	-	0.2	mJ
	Reverse current	Body diode reverse current voltage drop	I = -50 mA	-0.5	-1	-1.1	V

Table 25. LSc diagnosis electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT19,20	I_{OVC}	Over current threshold	-	70	-	130	mA
	$T_{FILTEROVC}$	Over current filtering time	Tested by scan	2	4	5	µs
	$T_{FILTERdiagoff}$	Filtering open load and short to GND diag. off	Tested by scan	35	50	65	µs
	Td_mask	Diagnosis mask delay after switch-off	Tested by scan	300	-	500	µs
	V_{HVT}	Open load threshold voltage	-	$V_{Outopen}$ +160mV	-	3	V
	$V_{Outopen}$	Output open load voltage	-	2.3	-	2.7	V
	V_{LVT}	Output short-circuit to GND threshold voltage	-	1.9	-	$V_{Outopen}$ -200mV	V
	I_{OUT_PD}	Output diagnostic pull down current Off state	Vpin = 5 V	50	-	110	µA
	I_{OUT_PU}	Output diagnostic pull up current Off state	Vpin = 1.5 V	110	160	210	µA
	I_{topen}	Open load threshold current	-	30	-	110	µA
	$V_{S/R\ ON}$	Voltage R On	R = 270 Ω C_{load} = 10 F From 80% to 30% of V_{OUT}	2	-	6	V/µs
	$V_{S/R\ OFF}$	Voltage R Off		5	-	14	V/µs

6.9.4 LSd function OUT13 to 18 (relay drivers)

Figure 36. LSd function OUT13 to 18 (relay drivers)



LSd functionality description

LSd are 6 protected Low-Side drivers with diagnosis, and over current protection circuit.

They are driven via MicroSecond Channel interface.

When Reset_L9779 signal or OUT_DIS bit is asserted OUT_LSd is switched off.

The turn on/off time is fixed and the slew-rate is controlled.

OUT13 and OUT14 are able to remain active also during crank pulse when the battery voltage on the VB pin goes below the level VB_LV for a period of time THOLD, this time lapse calculation is triggered by the falling edge of RST. In this situation VDD5 is below undervoltage threshold (VDD_UV) and the micro controller is in reset condition. During the THOLD time the VDD5 supply and the micro controller have to recover and take over control of the output. Otherwise the output is switched OFF after the THOLD time.

The low battery functionality can be enabled/disabled through bit OUT13_EN_LB and OUT14_EN_LB of CONF_REG7.

Table 26. LSd electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT 13 to 18	$R_{DS\text{-}on\ LSd}$	Drain source resistance	I_{load} = 0.6 A	-	-	1.5	Ω
	$IOUT_{lk}$	Output leakage current	Vpin = 13.5 V	-	-	10	µA
	$V_{S/R}$	Voltage S/R on/off	R = 21 Ω, C = 10 nF From 80% to 30% of V_{OUT}	2	-	6	V/µs
	$V_{S/R\ GateKill}$	FAST $V_{R/S}$ off when an OVC fault happens	Load: 8 Ω, 10 nF; From 80% to 30% $V_{OUT;}$	5	-	30	V/µs
	$T_{Turn\text{-}on\_LSd}$	Turn-on delay time	From command to 80% V_{OUT} Load: 21 Ω, 10nF	-	-	6	µs
	$T_{Turn\text{-}off\_LSd}$	Turn-off delay time	From command to 30% VOUT Load: 21 Ω, 10 nF	-	-	6	µs
	V_{cl}	Output clamping voltage	I_{load} = 0.6 A	40	45	50	V

Table 26. LSd electrical characteristics (continued)

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT 13 to 18	$PW_{clampSP}$	Clamp single pulse ATE test	I_{load} = 0.6 A; single pulse	-	-	15	mJ
	$PW_{clampRP}$	Clamp repetitive pulses Freq = 1 Hz (to be verified) Reliability Test	Tc ≤ 30 °C; I_OUT_n ≤ 0.45 A 1 Mio cycles	-	-	6.5	mJ
			Tc ≤ 80 °C; I_OUT_n ≤ 0.3 A 25 Mio cycle	-	-	6.5	
			Tc ≤ 100°C; I_OUT_n ≤ 0.3A 20 Mio cycle	-	-	6.5	
			Tc ≤ 130°C; I_OUT_n ≤ 0.3 A 5 Mio cycle	-	-	5.5	
	Reverse current	Body diode reverse current voltage drop	I = -0.6 A	-0.5	-1	-1.1	V

Min/Max of Reverse Current will be add after BA characterization.

Table 27. LSd diagnosis electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT 13 to 18	$R_{open\ load}$	Min resistor value open load detection	Not tested	500	-	-	kΩ
	I_{max}	Output current	Not tested	-	0.6	-	A
	I_{OVC}	Over current threshold	-	1	-	2	A
	$T_{FILTEROVC}$	Over current filtering time	Tested by scan	2	4	5	µs
	$T_{FILTERdiagoff}$	Filtering open load and short to GND diag. off	Tested by scan	35	50	65	µs
	T_{d_mask}	Diagnosis mask delay after switch-off	Tested by scan	300	-	500	µs
	V_{HVT}	Output voltage ok range threshold	-	$V_{Outopen}$ +120mV	-	3	µs
	$V_{OUTOPEN}$	Output open load voltage	Open load condition	2.3	-	2.7	V
	V_{LVT}	Output short-circuit to GND threshold voltage	-	1.9	-	$V_{Outopen}$ -200mV	V
	I_{OUT_PD}	Output diagnostic pull down current off state	V_{pin} = 5 V	50	-	110	µA
	I_{OUT_PU}	Output diagnostic pull up current off state	V_{pin} = 1.5 V	-210	-	-108	µA

Table 27. LSd diagnosis electrical characteristics (continued)

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT 13 to 18	I_{topen}	Open load threshold current	-	30	-	90	µA
OUT13, 14	T_{HOLD}	Switch on to off delay during low battery voltage operation	Tested by scan	400	-	800	ms
	VB_UV	VB voltage threshold for low battery function	-	-	-	4.15	V

Figure 37. Behavior of OUT13, 14, 21, 25 with VB = VB_LV for a time shorter than Thold and with a valid ON condition

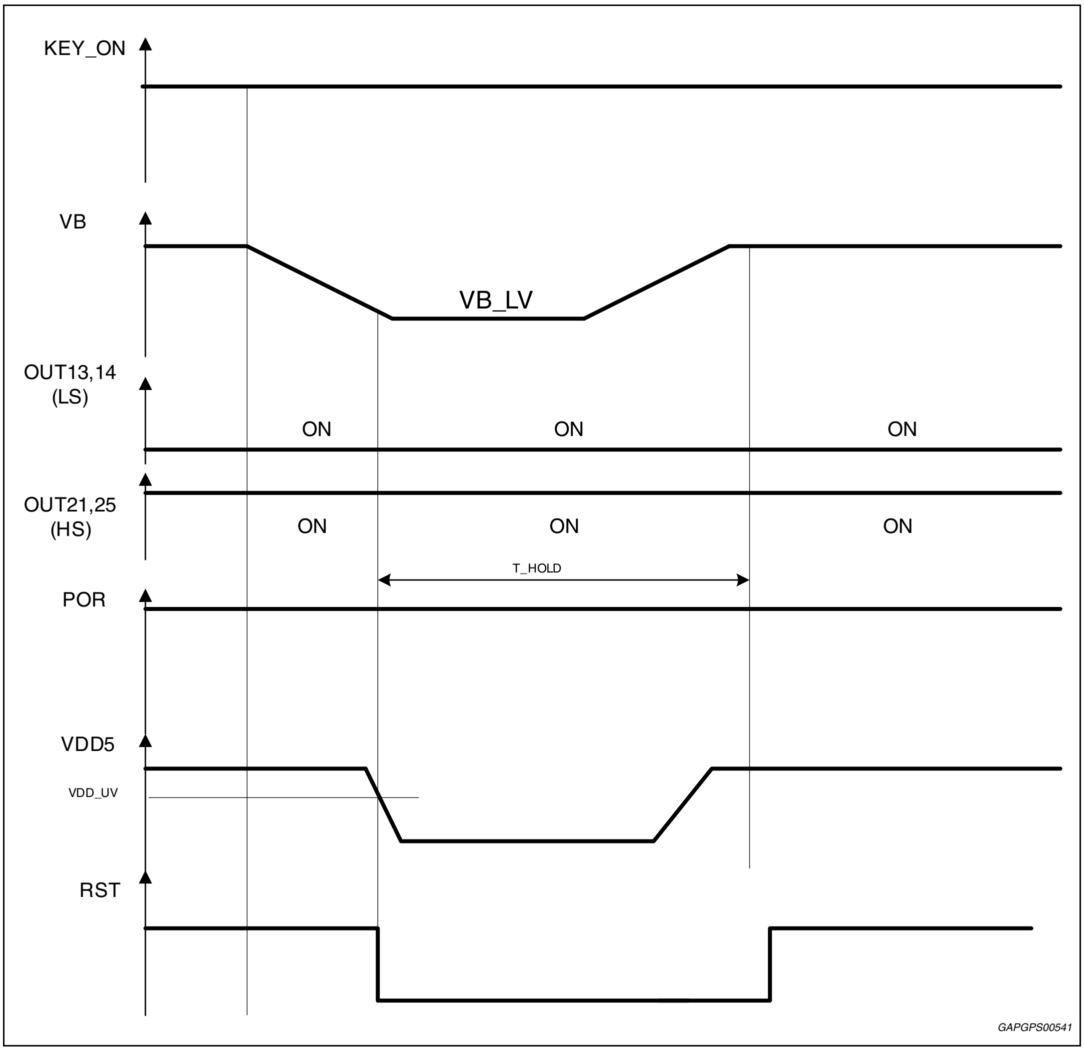


Figure 38. Behavior of OUT13, 14, 21, 25 with VB = VB_LV for a time longer than Thold and with a valid ON condition

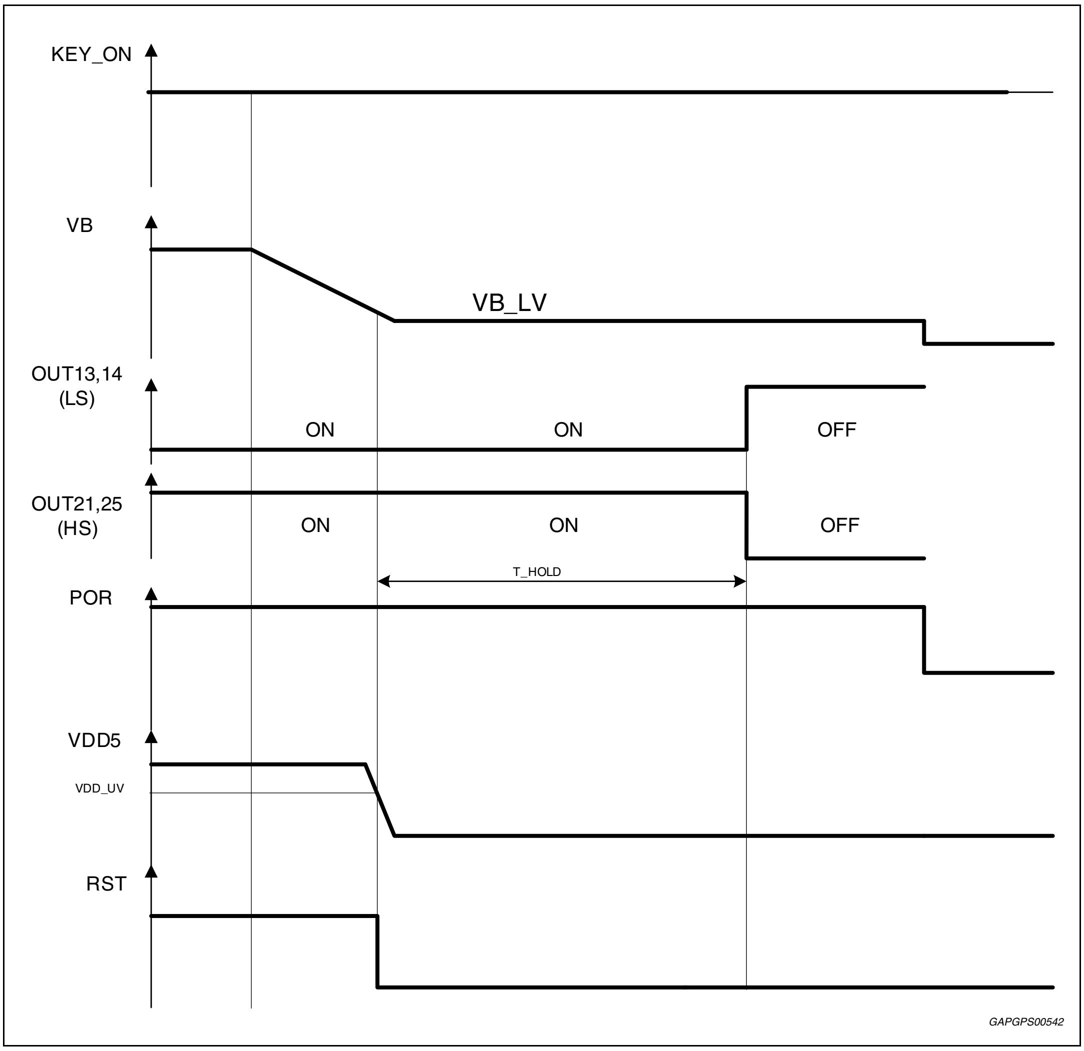
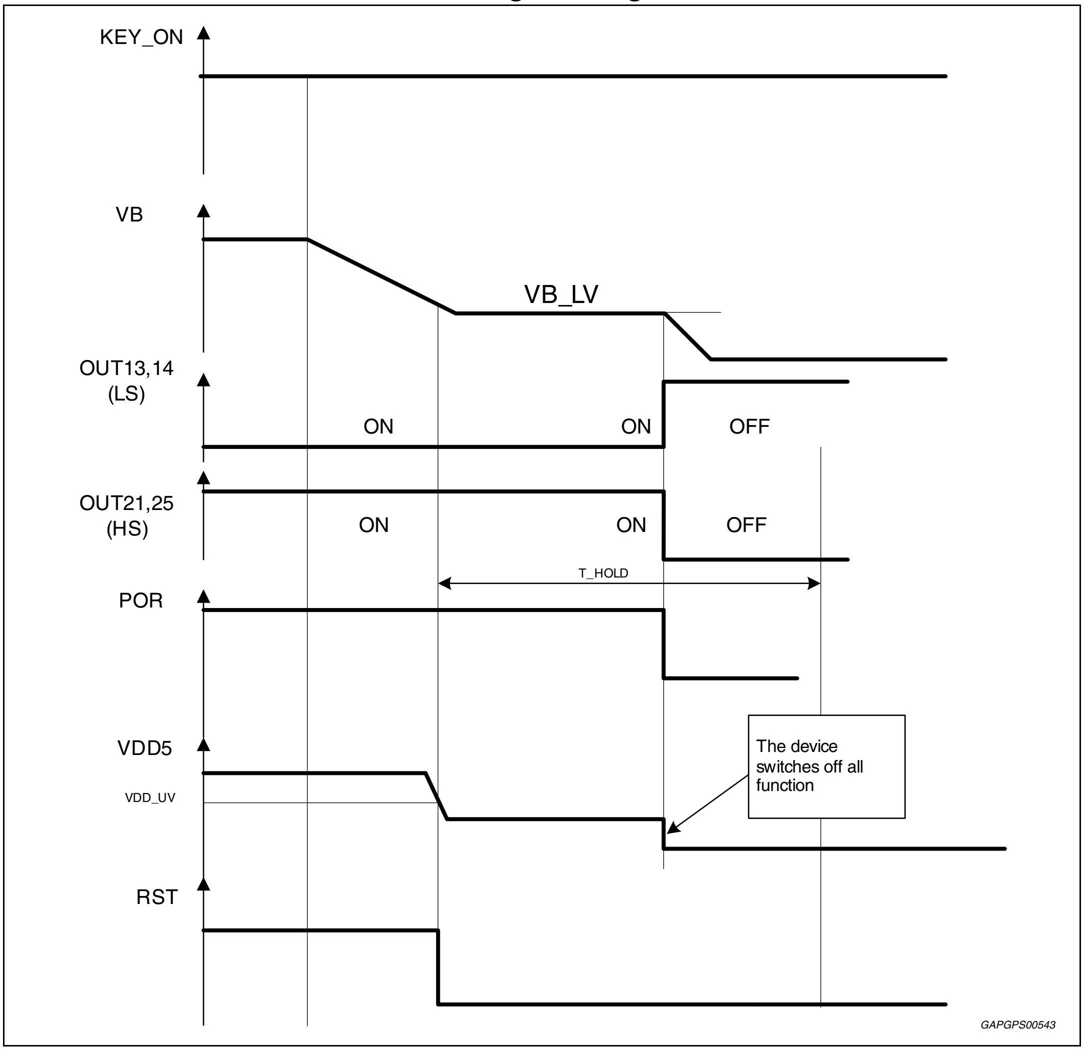


Figure 39. Behavior of OUT13, 14, 21, 25 with VB that drops lower than POR threshold during cranking



6.10 LSa, LSb, LSc, LSd diagnosis

Each channel locally detects and writes its own fault or no-fault condition (codified on 2 bit according to the table FAULT ENCODING CONDITION).

- short circuit to battery or overcurrent for all the outputs during ON condition.
- open load or short to GND during OFF condition.

The faults are latched and reset every Read Diag operation.

In OFF condition the first fault detected is latched and can be overwritten only by the ON condition fault.

Channel “on”

Short to Vb:

Current diagnosis is the result of a comparison between driver load current and internal IOVC thresholds.

If: I_{LOAD} > IOVC for t > $T_{FILTEROVC}$ the driver is switched off and the fault is set, latched and reset every Read Diag operation.

When the fault occurs the driver is switched off with a controlled slew-rate.

The driver switches on AGAIN in the following conditions:

- If command goes LOW and then HIGH again
- If command remains active the driver is switched automatically on at every Read Diag operation.

Short to GND:

Not available.

Open Load:

Not available.

Channel “off”

Short to Vb:

Not available.

Short to GND & open load:

In open load condition an internal circuit drives the OUTx voltage to VOUTOPEN with a maximum pull-up/down current of IOUT_PU and IOUT_PD.

Diagnosis is done comparing driver output voltage with internal voltage thresholds VHVT and VLVT: if the voltage is below VLVT a short to GND is detected, if the voltage is above VLVT and below VHVT an open load is detected and if the voltage is above VHVT no fault is present.

Diagnosis status is masked for Td_mask time after the off event occurs to allow the output voltage to reach the proper value.

Short to GND and open load are filtered with $T_{FILTERdiagoff}$ time.

Diag status is latched and reset at every Read Diag operation.

For LSc(OUT19,20) the IOUT_PD/IOUT_PU can be switched off by OFF_LCDR bit and therefore the Open Load and Short To GND detections are not available.

Figure 40. LSx diagnosis circuit

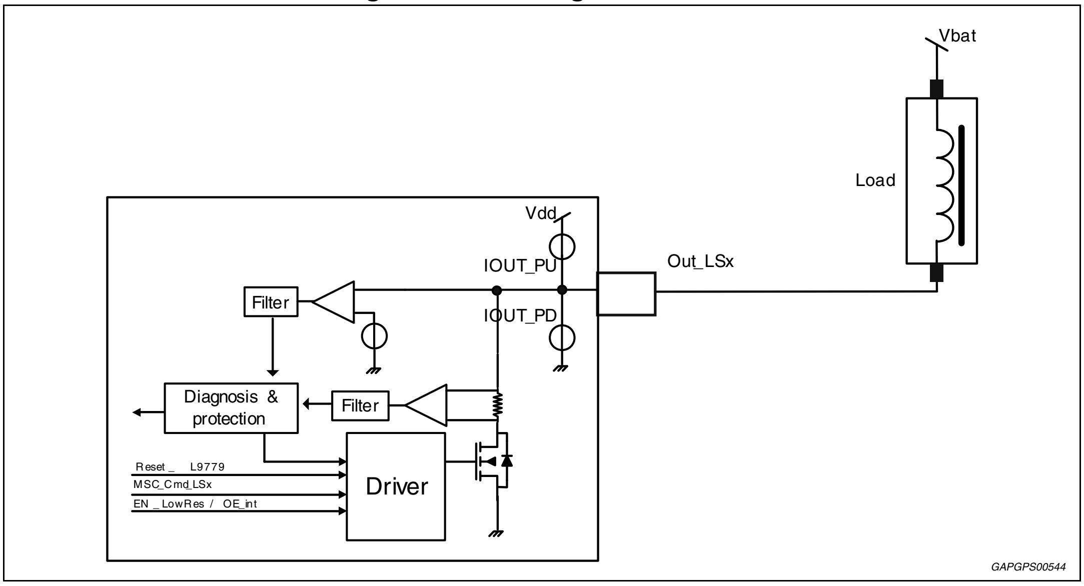


Table 28. Fault encoding condition

Bit n	Bit n+1	Description
1	1	Power stage OK no Fail
0	1	Open Load OL
1	0	Short circuit to VB/over current SGB
0	0	Short circuit to GND SCG

Figure 41. Fault encoding condition diagram

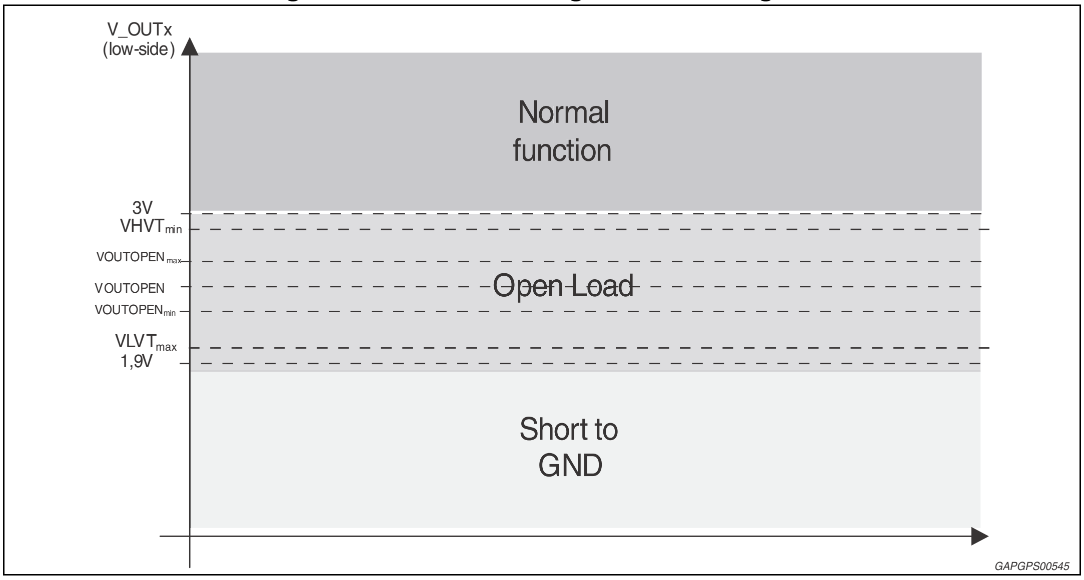
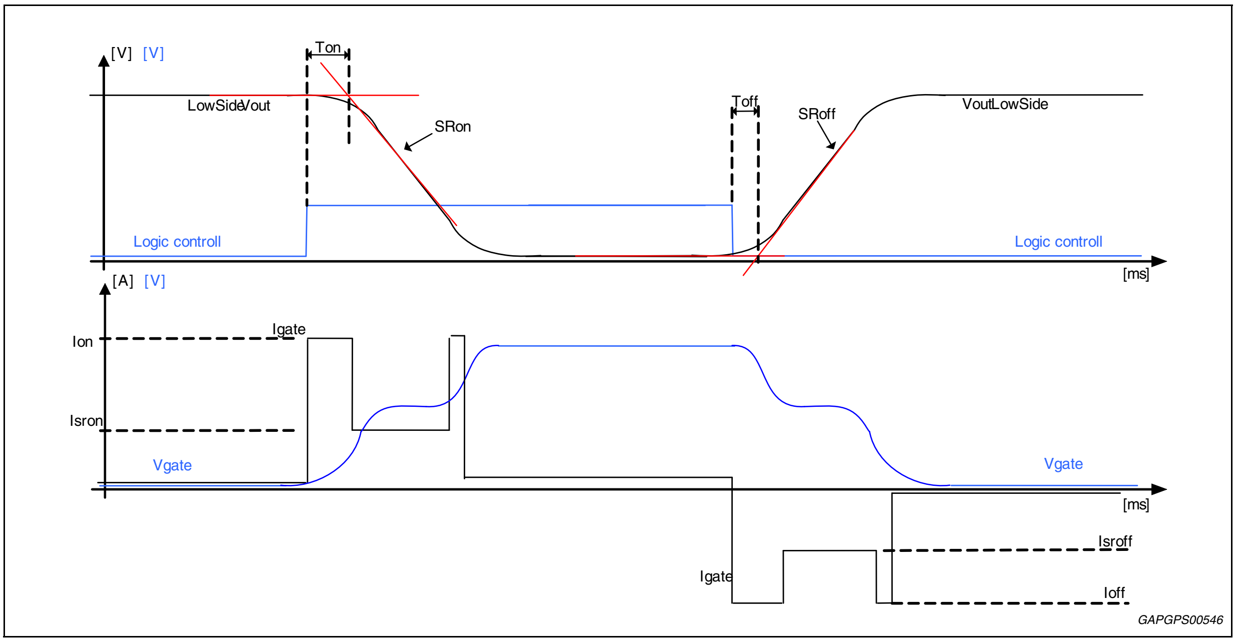
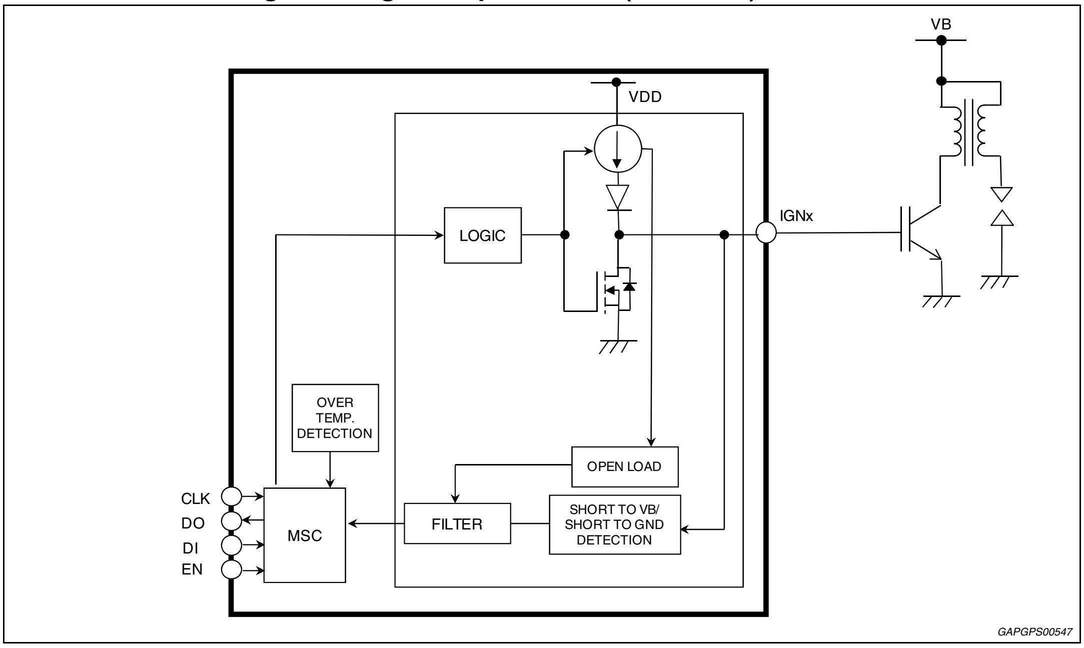


Figure 42. LSx ON/OFF slew rate control diagram



6.11 Ignition pre-drivers (IGN1 to 4)

Figure 43. Ignition-pre drivers (IGN1 to 4) circuit



6.11.1 Ignition pre-drivers functionality description

The 4 ignition pre-drivers are push-pull output with diagnosis and over current protection circuit. They can drive IGBT Darlington transistors.

The load is switched on with a current and switched off with I_LS_cont current.

They are driven via MicroSecond Channel.

When Reset_L9779 signal or OUT_DIS bit is asserted, output IGNx becomes high impedance.

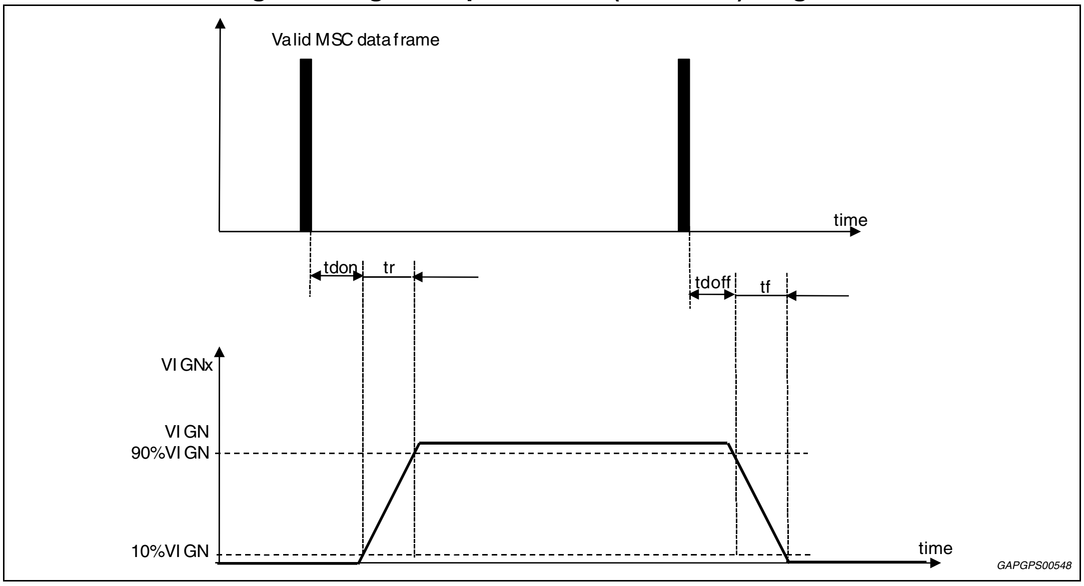
By MSC command it is possible to have the low-side stage always off, in this case there is an external pull down resistor that discharges.

The IGNx output in Off phase. This Bit is present in config2(0) and its name is LS_IGN_OFF.

Table 29. Ignition pre-drivers electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
IGN1 to 4	VDD5	Supply voltage range	Info only	4.9	-	5.1	V
	Vign	Output voltage high level	I_cont = 15 mA	4.35	-		V
	I_{leak_out}	Leakage current	-	-10	-	10	µA
	-I_lim	High-side current limitation	-	19	-	33	mA
	I_LS_cont	LS path continuous current capability	Add also the R_{DSON} Test	-	-	30	mA
	I_LS_RDS on	LS RDSON	-	3	-	14	Ω
	IOVC	High side over current detection	-	7	-	14	mA
	VLVT	Output short-circuit to Gnd threshold voltage	-	1.6	1.8	2	V
	Vign_scb	SCB detection voltage	-	VDD5 +0.1V	-	VDD5 +2V	-
	Iol	OL detection current	-	100	-	850	µA
	T_{don}	Output on delay time	CIgn = 10 nF	-	-	10	µs
	T_{ign_filt}	OVC/Open load diagnosis filter time, Test by scan	-	50	-	100	µs
	T_r	Output on rise time	CIgn = 10 nF	-	-	10	µs
	T_{doff}	Output off delay time	CIgn = 10 nF	-	-	10	µs
	T_f	Output off fall time	CIgn = 10 nF	-	-	10	µs
	R_{load}	Resistive load	For info only	1	-	10	kΩ
	C_{out}	Output capacitance loads	For info only	4	-	15	nF

Figure 44. Ignition-pre drivers (IGN1 to 4) diagram



6.11.2 Ignition pre-driver diagnosis

Each channel locally detects and writes its own fault or no-fault condition (codified on 2 bit according to *Table 28: Fault encoding condition*).

The detected faults are:

- IGNx short circuit to battery (SCB)
- IGNx open load (OL)
- IGNx short to GND (SCG)

Short to GND

This diagnosis is made in two different ways based on the status of IGN_DIA_SGEN.

If IGN_DIA_SGEN = 1

When the IGNx is on, if for a time longer than Tign_filt, the current is bigger than IOVC, the short to GND fault is detected and the IGNx output becomes high impedance, the fault is latched and is reset at every Read Diag operation.

If IGN_DIA_SGEN = 0

When the IGNx is on, if for a time longer than Tign_filt, the voltage of IGNx is lower than VLVT, the short to GND fault is detected and the IGNx output becomes high impedance, the fault is latched and is reset at every Read Diag operation.

The high impedance is removed and IGNx is driven by the command:

- – after a Read Diag operation
- – if command is switched OFF and ON again.

Open load

When IGNt is on, if for a time longer than Tign_filt, the current is below Iol the open-load fault is detected, latched and it is reset at every Read Diag operation. IGNx remains always driven.

Short circuit to battery

When the load is on, if the voltage of IGNx is bigger than the Vign_scb threshold for a time longer than Tign_filt the SCB fault is detected and the output IGNx becomes high impedance.

When the load is off, if the voltage of IGNx is bigger than the Vign_scb threshold for a time longer than Tign_filt the SCB fault is detected and the output IGNx becomes high impedance.

The SCB fault has a higher priority with respect to the OL fault.

According to the IGN_DIA_MODE bit, two behaviors are possible:

1. Latch mode

   The fault is latched and is reset at every Read Diag operation.

   The high impedance is removed and IGNx is driven by the command:

   – after a Read Diag operation

   – if the command is switched OFF and ON again.

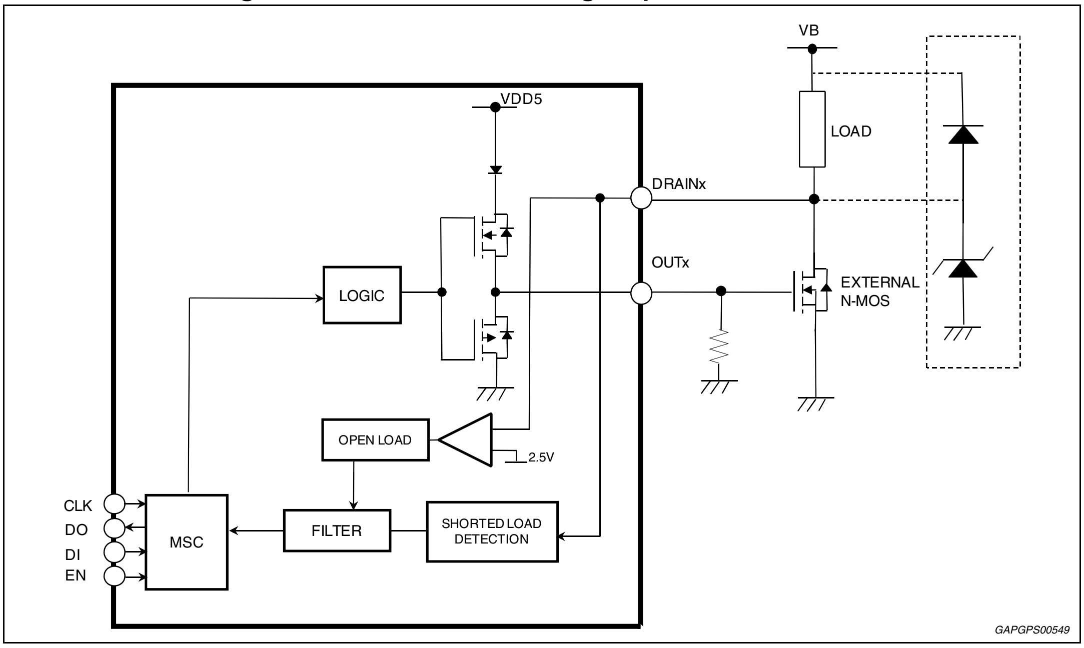
2. No latch mode

   The fault is not latched and if the voltage of IGNx is lower than the Vign_scb threshold for a time longer than Tign_filt the fault state disappears and the high impedance is removed.

6.12 External MOSFET gate pre-drivers

2x external N-MOS gate drivers are available.

Figure 45. External MOSFET gate pre-drivers circuit



The pre-drivers are designed with the following diagnostic features:

- Open load detection during off state
- Short circuit detection during on state
- Programmable drain threshold and filter time for short fault detection.

By monitoring the drain voltage of the external MOS each pre-driver is able to detect an open load and short to GND in the off state and a shorted load to VB in the on state. All faults are reported through MSC communication.

An open load fault is detected when the drain voltage is less than the Vopen threshold. A shorted load fault is reported when the drain voltage is greater than the programmed threshold voltage for a time longer than the tshort programmed time. The output is switched off and the fault bit is set.

The filter time and threshold voltage are programmed through MSC.

A suitable clamping device must be put external in order to protect the device.

Table 30. External MOSFET gate pre-drivers

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
DRAIN8_9, OUT8_9	V_{ON}	Output voltage high level	-	VDD5 -0.5V	-	VDD5	-
	I_{leak_L}	Leakage current of push-pull low-side	-	-	-	1	µA
	I_{leak_H}	Leakage current of push-pull high-side	-	-	-	1	µA
	I_{drive}	Turn-on current	-	22	-	12	mA
	I_{drive}	Turn-off current	-	12	-	22	mA
	R_{gate}	External resistive pull-down	Application note	-	200	-	kΩ
	V_{HVT}	Output voltage ok range threshold	-	$V_{Outopen}$ +120mV	-	3	-
	$V_{OUTOPEN}$	Output open load voltage	Open load condition	2.3	-	2.7	V
	V_{LVT}	Output Short-circuit to Gnd threshold voltage	-	1.9	-	$V_{Outopen}$ -200mV	V
	I_{DRAIN_PD}	Output diagnostic pull down current off state	Vpin = 5 V	50	-	110	µA
	I_{DRAIN_PU}	Output diagnostic pull up current off state	Vpin = 1.5 V	110	160	210	µA
	I_{topen}	Open load threshold current	-	30	-	90	µA
	$T_{FILTERdiagoff}$	Filtering open load and short to gnd diag. off, Test by scan	-	37	50	63	µs
	T_{d_mask}	Diagnosis Mask Delay after switch-off, Test by scan	-	300	-	500	µs
	T_{delay}	Output on-off delay time Cout = 10 nF	From command to 10% of transition	-	-	2.2	µs
	Vshort	Short to VB fault detection voltage threshold. Programmable from 0.15 V to 2.5 V	-	-20%	0.15(1)	+20%	V
				-20%	0.3	+20%	
				-20%	0.45	+20%	
				-15%	0.5 (default)	+15%	
				-15%	1	+15%	
				-15%	1.5	+15%	
				-15%	2	+15%	
				-15%	2.5	+15%	

Table 30. External MOSFET gate pre-drivers (continued)

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
DRAIN8_9, OUT8_9	Tshort	Short to VB fault filter time. Programmable from 1.3 µs to 170 µs, Test by scan	-	-25%	1.3	+25%	µs
					2.6		
					5.2 (default)		
					10		
					21		
					42		
					84		
					170		

1. 0.172 for OUT8.

6.12.1 External MOSFET gate pre-drivers diagnosis

Each channel locally detects and writes its own fault or no-fault condition (codified on 2 bit according to the *Table 28: Fault encoding condition*).

- Short circuit to battery or overcurrent for all the outputs during ON condition.
- Open load or short to GND during OFF condition.

The faults are latched and reset at every Read Diag operation.

In “off” conditions the first fault detected is latched and can be overwritten only by the ON condition fault.

Channel “on”

Short to Vb:

Current diagnosis is the result of a comparison between Drain pin voltage and the internal Vshort threshold selected by MSC.

If: Vdrain> Vshort for t > T_{SHORT}

the driver is switched off and the fault is set, latched and reset at every Read Diag operation.

When the fault occurs the driver is switched off with a controlled slew-rate.

The drivers switches on AGAIN in the following conditions:

- – If command goes LOW and than HIGH again
- – If command remains active driver is switched automatically on at every Read Diag operation.

Short to GND:

Not available.

Open load:

Not available.

Channel "off"

Short to Vb:

Not available.

Short to GND and open load:

In open load conditions an internal circuit drives the DRAINx voltage to VOUTOPEN with a maximum pull-up/down current of IOUT_PU and IOUT_PD.

Diagnosis is done comparing driver output voltage with internal voltage thresholds VHVT and VLVT: if the voltage is below VLVT a short to GND is detected, if the voltage is above VLVT and below VHVT an open load is detected and if the voltage is above VHVT no fault is present.

Diagnosis status is masked for Td_mask time after the off event occurs to allow the output voltage to reach the proper value.

Short to GND and Open load are filtered with $T_{FILTERdiagoff}$ time.

Diag status is latched and reset every Read Diag operation.

6.13 Configurable power stages (CPS) (OUT21 to 28)

6.13.1 Configurable power stages functionality description

L9779 has 4 low-side N-channel power stages and 4 high-side P-channel power stages [OUT21 to OUT28] that can be arranged as follows using the CPS_CONF1,2 bit (default H-bridge):

- Eight individual power stages (four low-side and four high-side power stages). Low side can be connected in parallel (in pair) to obtain a low side driver with about 0.75 Ω R_{dson} resistance:

  OUT22 with OUT24 and OUT27 with OUT28.

  For three reasons outputs are switched in parallel:

  a) to increase current capability (please see electrical characteristic)

  b) to reduce power dissipation (please see electrical characteristic)

  c) to increase clamp energy capability (please see electrical characteristic) The max. clamping energy is probably less than the sum of the corresponding max. clamping energies.

  Parallel connection of Low-side power stages is possible as the control bit to turn-on and off the power stages is allocated in the same register. Unlike the H-bridge configuration, no coherency check is done.

  OUT21 and OUT25 are able to remain active also during crank pulse during which the battery voltage on the VB pin goes below the level VB_LV for a period of time THOLD, this time lapse calculation is triggered by the falling edge of RST In this situation VDD5 is below undervoltage threshold (VDD_UV) and the micro controller is in reset condition. During the THOLD time the VDD5 supply and the micro controller have to recover and take over control of the output. Otherwise the output is switching to OFF condition after the THOLD time.
  The low battery functionality can be enabled/disabled through bit OUT21_EN_LB and OUT25_EN_LB of CONF_REG7.
  For the behavior of OUT21, 25 during cranking refer to behavior of OUT13, 14.

Note: The bit OUT21,25_EN_LB has priority over CPS_CONFx bit, this means that if one of OUT21,25_EN_LB is set to 1 the OUT21…28 become independent power stages.

- Two H-Bridge for stepper motor driving (no half-bridge arrangement is possible).
  The over current threshold is the same as the single power stages.

When configured for stepper motor driving the motor movement is controlled through bit EN, DIR and PWM (see *Table 31*).

In stepper motor configuration HS and LS power stages (OUT21...OUT28) can be used as single power stages, and any of them can be connected in parallel to each other (same type).

If the bit EN=1, the writing of bit PWM from 0 to 1 lead to the next step of the turn on sequence. The writing of bit PWM to 0 left unchanged the MOS of the bridge that is ON. The step is done only if the PWM bit goes from 0 to 1.

The order of the turn-on sequence is defined by the bit DIR.

Table 31. Configuration of the stepper motor

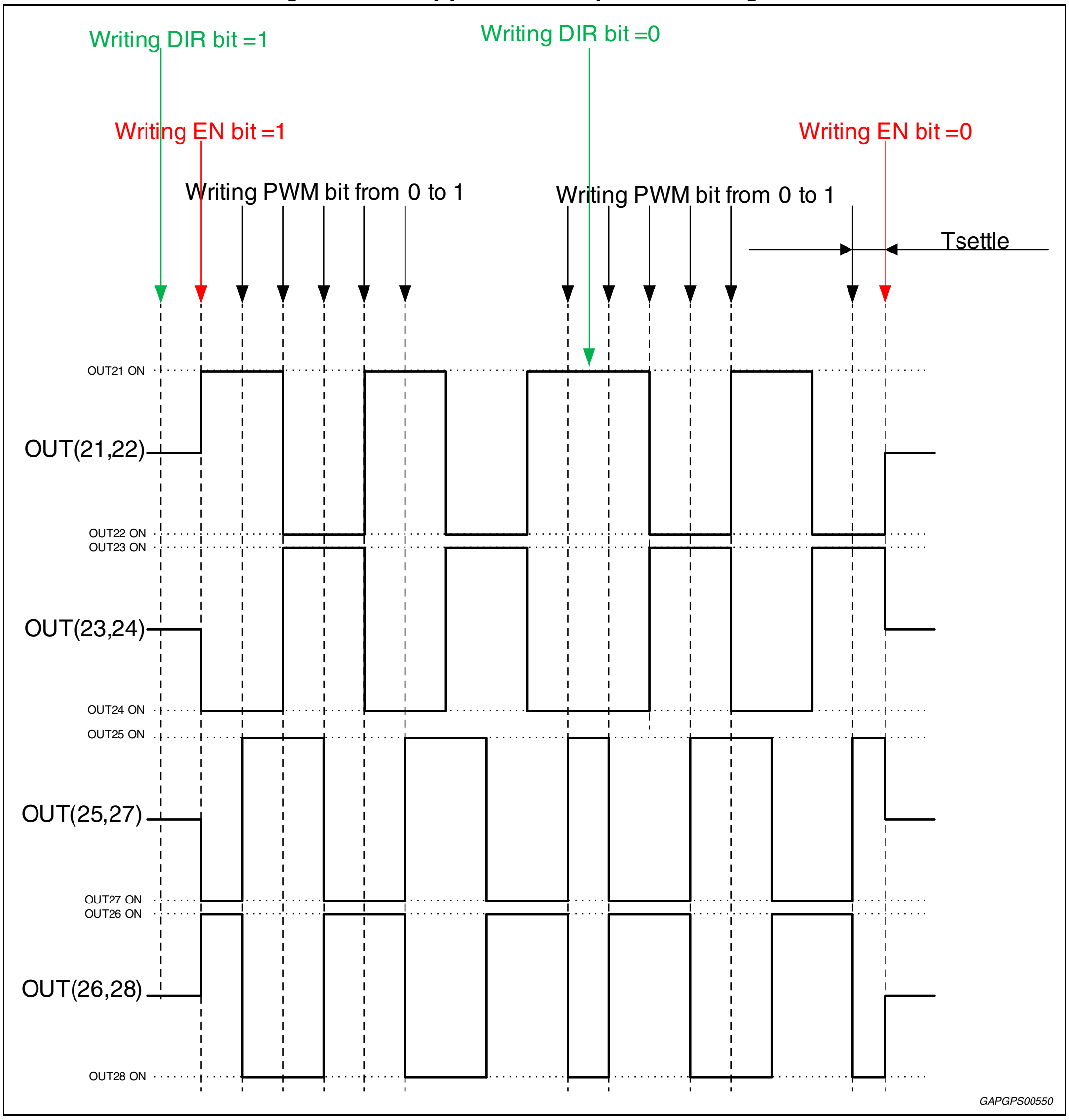
PWM	EN	DIR	H-bridge 1 Power on	H-bridge 2 Power on
X	0	X	None	None
1	1	1	OUT21, OUT24	OUT26, OUT27
1	1	1	OUT21, OUT24	OUT25, OUT28
1	1	1	OUT23, OUT22	OUT25, OUT28
1	1	1	OUT23, OUT22	OUT26, OUT27
1	1	0	OUT21, OUT24	OUT26, OUT27
1	1	0	OUT23, OUT22	OUT26, OUT27
1	1	0	OUT23, OUT22	OUT25,OUT28
1	1	0	OUT21, OUT24	OUT25,OUT28

The initial stepper position, after power-on, is the one with OUT21 and OUT24 ON in Hbridge1 and with OUT26 and OUT27 ON in Hbridge2.

If configured as H-bridges the internal logic prohibits that the low-side and the high-side switch of the same half-bridge will be switched on simultaneously.

In the below diagram the stepper motor operation is available.

Figure 46. Stepper motor operation diagram



The writing of DIR bit and PWM bit cannot be done in the same time, at least two consecutive MSC frames are necessary.(if done the stepper will move one step in the old direction).

The writing of EN bit and PWM bit cannot be done in the same time, at least two consecutive MSC frames are necessary. (If done it is supposed that only the EN bit has been received).

Table 32. H-bridge1 configurable power stages OUT [21 to 24]

H-bridge1	Comment	Nominal current	Ron max	Switch off current (min.)	Clamping (typ.)
OUT21	High-side P-Ch	0.6 A	1.5 Ω	1 A	N/A
OUT22	Low-side N-Ch	0.6 A	1.5 Ω	1 A	45 V

Table 32. H-bridge1 configurable power stages OUT [21 to 24] (continued)

H-bridge1	Comment	Nominal current	Ron max	Switch off current (min.)	Clamping (typ.)
OUT23	High-side P-Ch	0.6 A	1.5 Ω	1 A	N/A
OUT24	Low-side N-Ch	0.6 A	1.5 Ω	1 A	45 V

Table 33. H-bridge2 configurable power stages OUT [25 to 28]

H-bridge2	Comment	Nominal current	Ron max	Switch off current (min.)	Clamping (typ.)
OUT25	High-side P-Ch	0.6 A	1.5 Ω	1 A	N/A
OUT26	High-side P-Ch	0.6 A	1.5 Ω	1 A	N/A
OUT27	Low-side N-Ch	0.6 A	1.5 Ω	1 A	45 V
OUT28	Low-side N-Ch	0.6 A	1.5 Ω	1 A	45 V

Figure 47. Configurable power stages OUT [21 to 24] can be configured to create the H-bridge1

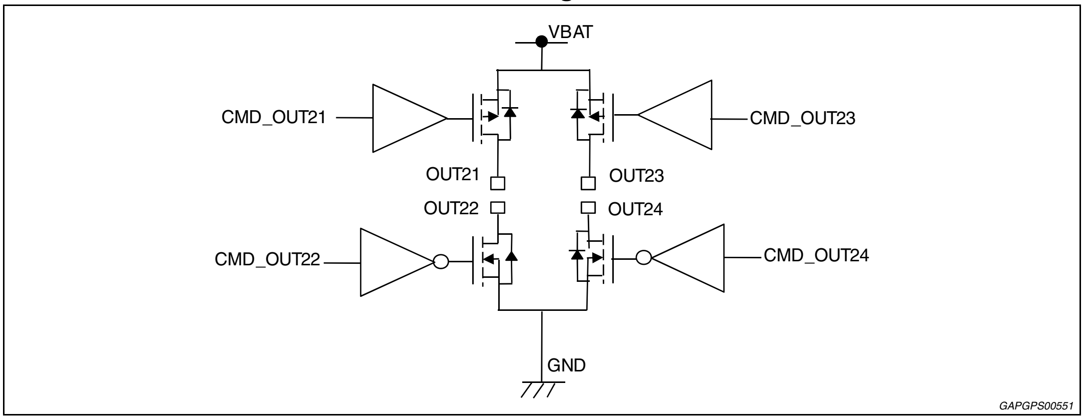
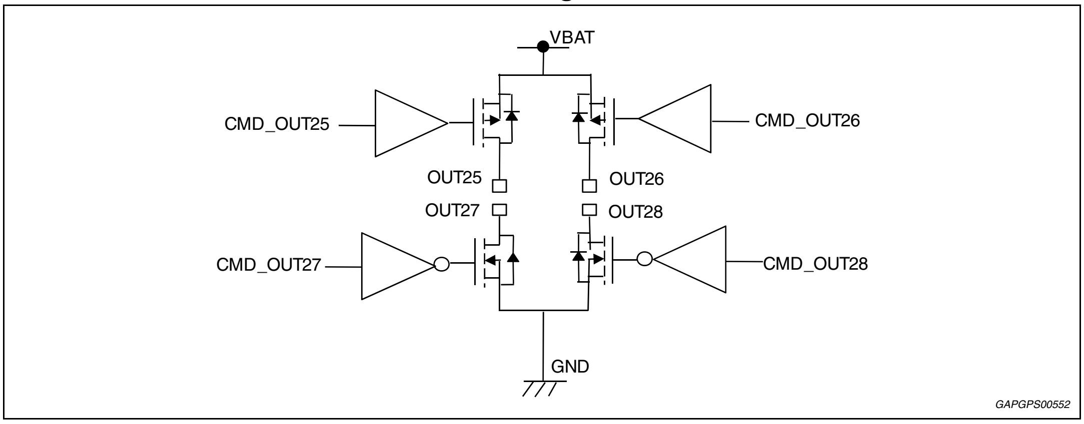


Figure 48. Configurable power stages OUT [25 to 28] can be configured to create the H-bridge2



Stepper counter

In order to keep trace of the stepper movement in L9779WD a 10-bit register is available (5 bits in the STEP_CNT_H and 5 bits in the STEP_CNT_L)

The value of this register after the power-up is 512 and:

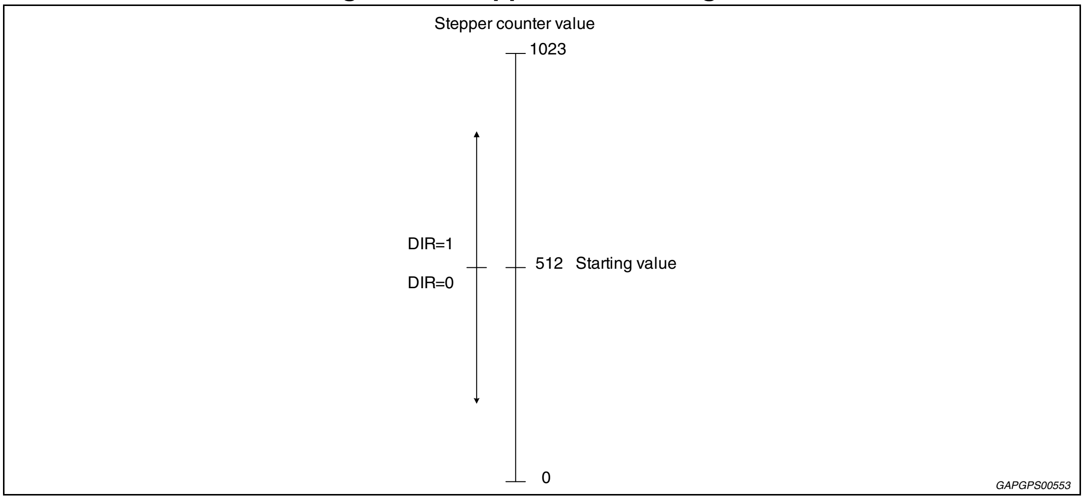
- with DIR=1 the value is increased by one for each step of the motor
- with DIR=0 the value is decreased by one for each step of the motor.

When the counter reaches the max or min value it remains at that value unless the direction is inverted.

In the STEP_CNT_H and STEP_CNT_L registers there are two bits used to check if the content of the register is referred to the same motor step.

The stepper counter is reset by power-on reset and software reset.

Figure 49. Stepper counter diagram



Driver parallel configuration

Low side drivers can be connected in parallel to increase the current driving capability. High side drivers behave similarly.

Configurations are set by CONFIG_REG7 and CONFIG_REG10.

6.13.2 Diagnosis of configurable power stages (CPS)

All CPS have fault diagnostic functions:

- Short-circuit to battery voltage: (SCB) can be detected if switches are turned on
- Short-circuit to ground: (SCG) can be detected if switches are turned off
- Open load: (OL) can be detected if switches are turned off
- Over temperature: (OT) will be detected with the general thermal warning(OT2)

Diagnosis is different for configuration as full-bridges or as single power stages. The faults are coded in different way and are stored in diagnostic registers.

In each configuration the registers can be read via MSC. With the beginning of each read cycle the registers are cleared automatically.

In each configuration there is one central diagnostic bit F2 for fault occurrence at any output.

6.13.3 Diagnosis of CPS [OUT21 to OUT28] when configured as H-bridges

Stepper motor driver OFF diagnosis (output in high impedance state).

In OFF condition Short to GND/Short to VB or Open Load condition is continuously detected through a deglitch filter Tdgc_off, after Tmask_step masking time to filter ON/ OFF transition. To avoid false diagnostic due to motor residual movement, the off command (EN bit=0) must be sent Tsettle time after the last valid on command PWM bit written to 1 (one couple of HS and LS switched on). A fault longer than deglitch time is latched.

Off state diagnostic fault can be overwritten by on state fault.

Off state fault does not prevent the stepper from switching on. The latched fault is cleared by reading the diagnosis data registers via MSC - and so resetting the diagnosis registers.

An Off state due to a wrong command sent by MSC interface does not activate the Off diagnosis.

Stepper motor driver ON diagnosis (Output driven by MSC CONTR_REG bit)

In ON condition when over current fault is detected and validated after digital filtering time Tdgc_ON, the bridge is turned OFF and the fault is latched. The bridge is turned ON again by MSC command. The latched fault is cleared by reading the diagnosis data registers via MSC and so resetting the diagnosis registers.

Over current fault has higher priority over OFF condition faults.

Each Bridge has dedicated fault diagnosis register DIAG_H1, DIAG_H2.

In ON condition if the current in the load current is lower than I_OPEN_LOAD for a time longer than Tdgc_ol_on, an Open load condition is detected

It could be necessary two steps of the stepper motor operation to detect the real kind of fault, in this case as first diagnosis the fault is "Fault detection running" and with the next PWM command it is possible to understand if the fault is an OPEN LOAD or an OVERCURRENT/SHORT to GND.

The Faults "DETECTION_RUNNING" & "OPEN LOAD" are latched during the during rise & fall edge of low-side driver command, if the fault disappeared during these phases the fault condition is no latched:

- The FAULT DETECTION RUNNING is no latched, the fault comes back to 0 if the current becomes higher than open load threshold, before the switch off of low-side driver.
- The FAULT OPEN LAOD is no latched, the fault comes back to 0 if the current becomes higher than open load threshold, before the switch off of low-side driver.

A diagnostic read will clear the “fault detection running” flag. Anyway the diagnostic will restart.

Figure 50. Stepper motor driver “off” diagnosis time diagram

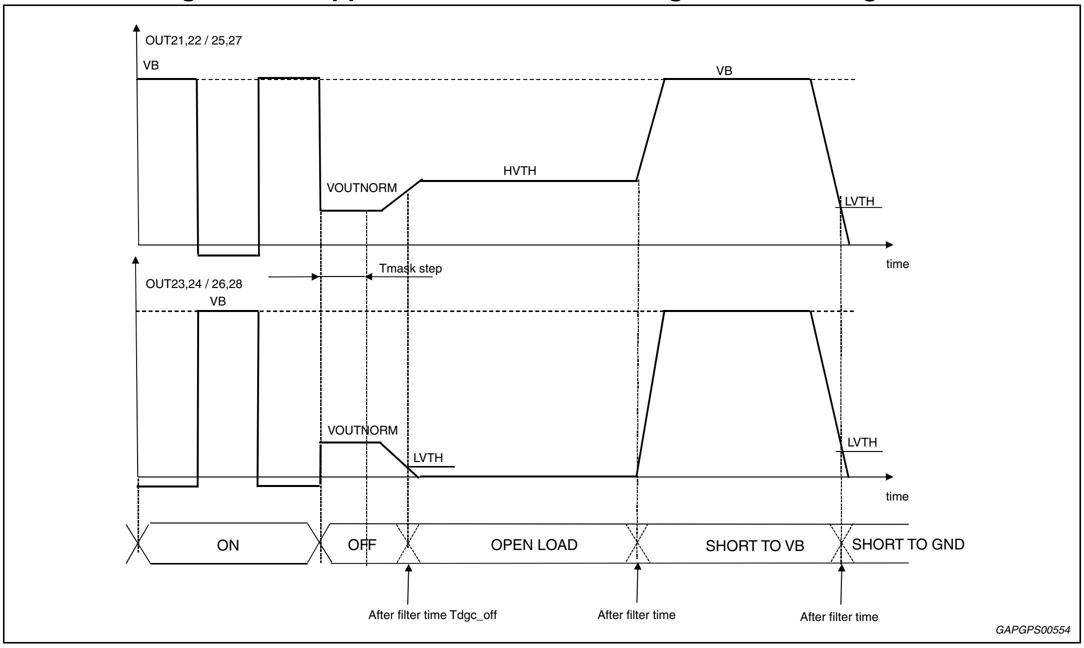
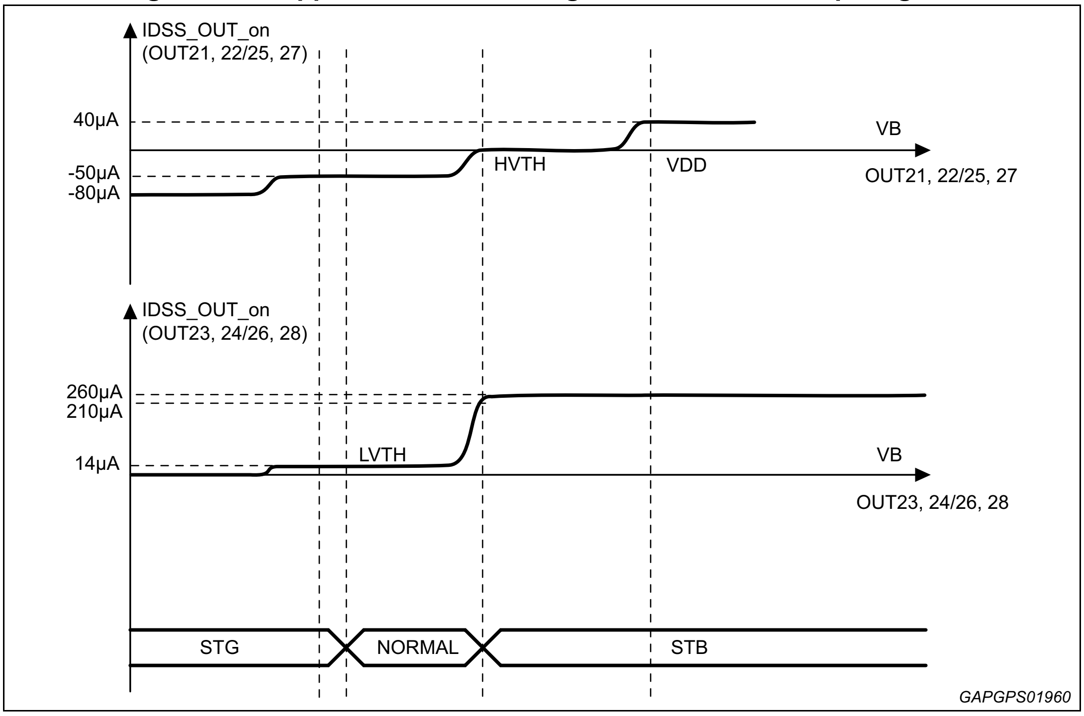


Figure 51. Stepper motor driver diagnosis I-V relationship diagram



Note: this wave shows the I/V relationship of pin current and pin voltage when OUTA(OUTC) short to OUTB(OUTD) and force the pin voltage from 0 V to VB in typical condition. For example, when pin voltage of OUTA = OUTB = 1.5 V, the pull up/down current is about -50 µA for OUTA and about 14 µA for OUTB. When pin voltage of OUTA = OUTB = 5 V, the pull up/down current is about 40 µA for OUTA and about 220 µA for OUTB.

Figure 52. Open load detection during "on" phase

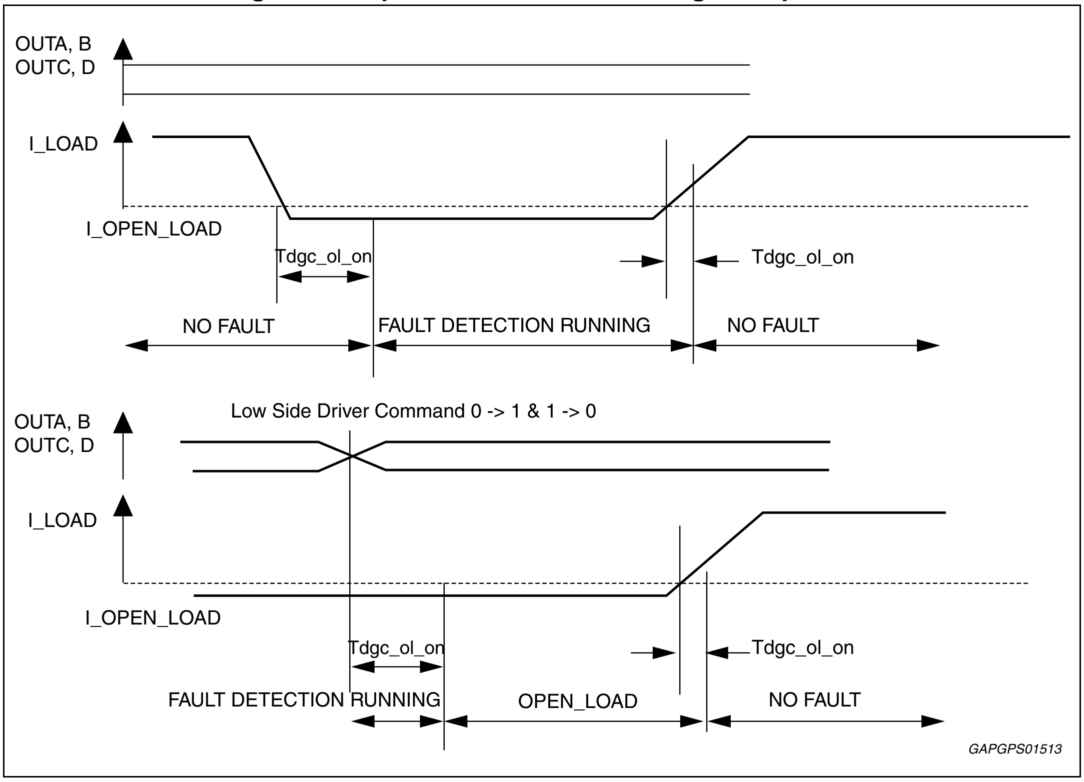


Figure 53. Open load detection during "on" phase

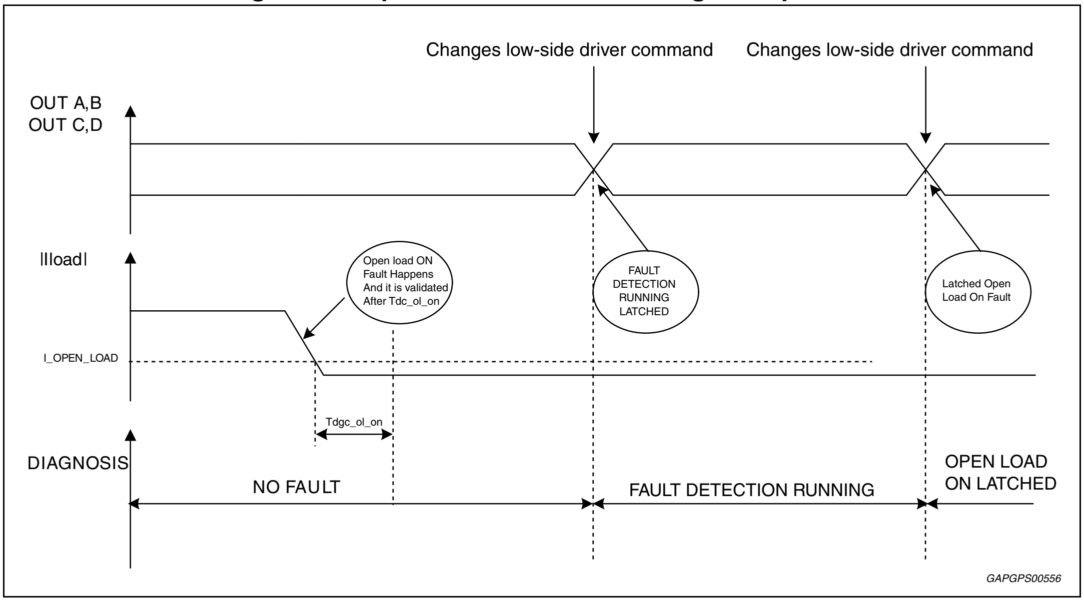


Figure 54. Short to GND detection during “on” phase

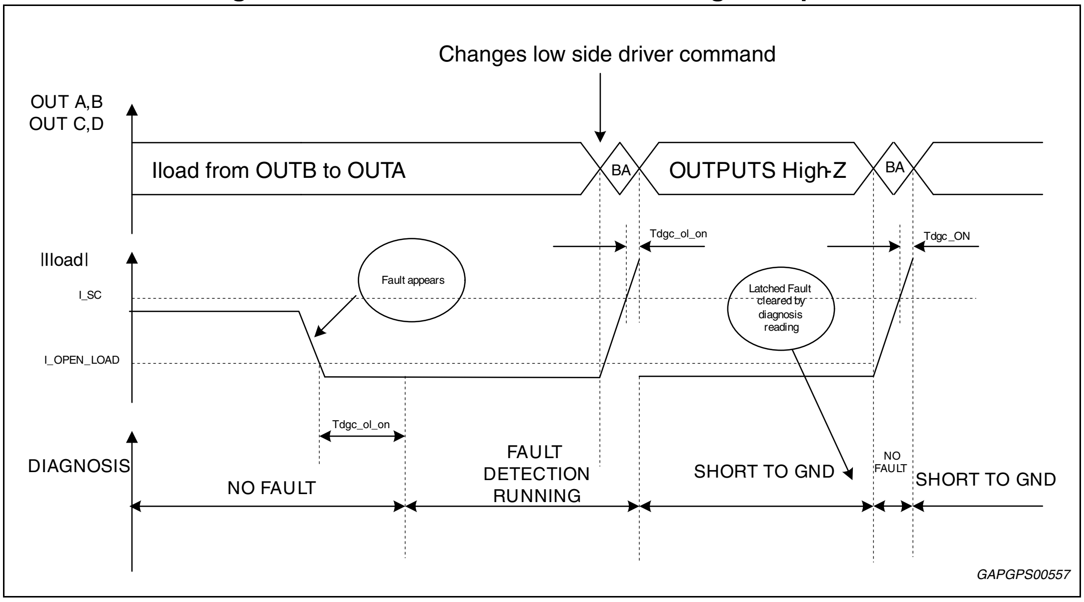


Table 34. Stepper configuration electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT 21 to 28	$V_{Outnorm}$	OUT(21,22), OUT(23,24), OUT(25,27), OUT(26,28) output voltage	OUT(21,22) short to OUT(23,24); OUT(25,27) short to OUT(26,28);	2.3	-	2.7	V
	H_{VTH}	Diagnostic high threshold	Driver in OFF condition	$V_{Outnorm}$ +120mV	-	3	V
	L_{VTH}	Diagnostic low threshold	Driver in OFF condition	1.9	-	$V_{Outnorm}$ -200mV	V
	I_{OVC}	Over current threshold	-	1	-	2.1	A
	I_OPEN_LOAD	Output open load threshold current	-	10	-	90	mA
	IOUT_PD_A+B or C+D	Output diagnostic pull down current OFF STATE	Vpin = 5 V	200	-	350	µA
	IOUT_PU_A+B or C+D	Output diagnostic pull up current OFF STATE	Vpin = 0 V	50	-	150	µA
	R_{openl}	Open load resistor threshold	Application note	150	-	-	kΩ
	Tdgc_ON	Deglitch filter time in ON condition	Test by scan	-25%	10	+25%	µs
	Tdgc_OFF	-	Test by scan	-25%	125	+25%	µs
	Tdgc_ol_on	-	Test by scan	-25%	20	+25%	µs

Table 34. Stepper configuration electrical characteristics (continued)

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT21…28	Tmask_step	-	Test by scan	-25%	1	+25%	ms
	Tsettle	-	For information only; No tested	100	-	-	ms
	T_PWM	Operating frequency	For information only; No tested	50	-	-	µs

6.13.4 Diagnosis of CPS [OUT21 to OUT28] when configured as single power stages

For the low side the diagnosis is the same as LSd.

For the high side the diagnosis is described below.

Each channel locally detects and writes its own fault or no-fault condition (codified on 2 bit according to *Table 28: Fault encoding condition*).

- Short circuit to battery or overcurrent for all the outputs during ON condition.
- Open load or short to GND during OFF condition.

The faults are latched and reset at every Read Diag operation.

In OFF condition the first fault detected is latched and can be overwritten only by the ON condition fault.

Channel “on”

Short to GND:

Current diagnosis is the result of a comparison between driver load current and internal Ilimit thresholds.

If:

$I_{LOAD} > I_{OVC}$ for $t > T_{FILTEROVC}$

the driver is switched off and the fault is set, latched and reset at every Read Diag operation.

When the fault occurs the driver is switched off with a controlled slew-rate.

The Drivers switches on AGAIN in the following conditions:

- – If command goes inactive and then active again
- – If command remains active driver is switched automatically on at every Read Diag operation.

Short to VB:

Not available.

Open load:

Not available.

Channel “off”

Short to GND:

Not available.

Short to VB & open load:

In open load condition an internal circuit drives the OUTx voltage to VOUTOPEN with a maximum pull-up/down current of IOUT_PU and IOUT_PD.

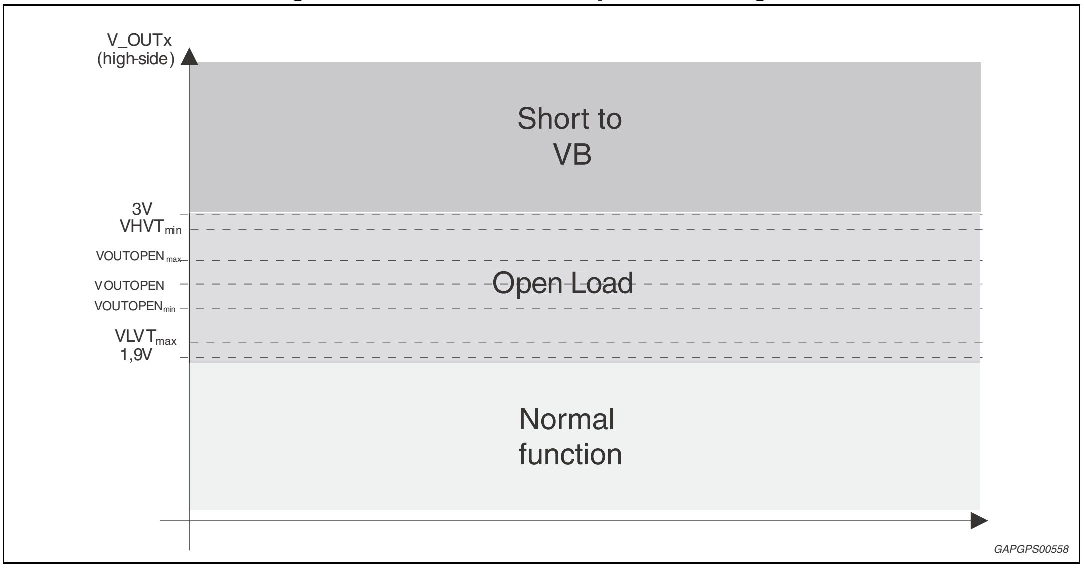
Diagnosis is done comparing driver output voltage with internal voltage thresholds VHVT and VLVT: if the voltage is above VHVT a short to VB is detected, if the voltage is above VLVT and below VHVT an open load is detected and if the voltage is below VLVT no fault is present.

Diagnosis status is masked for Td_mask time after the off event occurs to allow the output voltage to reach the proper value.

Short to GND and Open load are filtered with $T_{FILTERdiagoff}$ time.

Diag status is latched and reset at every Read Diag operation.

Figure 55. Short to VB & open load diagram



Electrical and diagnosis characteristics of [OUT22], [OUT24], [OUT27], [OUT28] when configured as single power stages

Same parameter and diagnosis function as LSd.

Table 35. Electrical and diagnosis characteristics of [OUT22], [OUT24], [OUT27], [OUT28] when configured as single power stages

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT22, 24,27,28	$R_{DS\text{-}on\ LSd}$	Drain source resistance	I_{load} = 0.6 A	-	-	1.5	Ω
	$IOUT_{lk}$	Output leakage current	Vpin = 13.5 V	-	-	10	µA
	$V_{S/R}$	Voltage S/R On/off	R = 21 Ω, C = 10nF From 80% to 30% of V_{OUT}	2	-	6	V/us
	$V_{S/R\ GateKill}$	Fast VR/S off when an OVC fault happens	Load: 8 Ω, 10nF - from 80% to 30% of VOUT	5	-	30	V/µs
	$T_{Turn\text{-}On\_\ LSd}$	Turn-on delay time	From command to 80% V_{OUT} Load: 21 Ω, 10nF	-	-	6	µs
	$T_{Turn\text{-}Off\_\ LSd}$	Turn-off delay time	From command to 30% V_{OUT} Load: 21 Ω, 10nF	-	-	6	µs
	$T_{FILTEROVC}$	Over current filtering time	Tested by scan	2	3	4	µs
	$T_{FILTERdiagoff}$	Filtering open load and short to GND diag. off	Tested by scan	8	10	12	µs
	T_{d_mask}	Diagnosis mask delay after switch-off	Tested by scan	350	400	450	µs
	1.5 Ω	Output clamping voltage	I_{load} = 0.6A	46	48	50	V
	$PW_{clampSP}$	Clamp single pulse ATE test	I_{load} = 0.6A; single pulse	-	-	15	mJ
	$PW_{clampRP}$	Clamp repetitive pulses Freq = 1 Hz (to be verified) Reliability Test	Tc ≤ 30 °C; I_OUT_n ≤ 0.45 A 1 Mio cycles	-	-	6.5	mJ
			Tc ≤ 80°C; I_OUT_n ≤ 0.3A 25 Mio cycle	-	-	6.5	
			Tc ≤ 100°C; I_OUT_n ≤ 0.3A 20 Mio cycle	-	-	6.5	
			Tc ≤ 130 °C; I_OUT_n ≤ 0.3 A 5 Mio cycle	-	-	5.5	
	Reverse voltage	Body diode reverse current voltage drop	I = -0.6 A	-0.5	-1	-1.1	V

Electrical characteristics of [OUT22], [OUT24], [OUT27], [OUT28] when configured as single power stages connected in parallel

When the low side drivers are connected in parallel (in pair) to obtain a low side driver with a lower resistance, OUT22 with OUT24 and OUT27 with OUT28, the following parameters should be considered:

Table 36. Electrical characteristics of [OUT22], [OUT24], [OUT27], [OUT28] when configured as single power stages connected in parallel (For information only)

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Out 22_24, 27_28	Imax	Output current	Not tested	-	1.2	-	A
	$R_{DS\text{-}on\ LSd}$	Drain source resistance	I_{load} = 1.2 A	-	-	0.75	Ω
	$IOUT_{lk}$	Output leakage current	(1)	-	-	10	µA
	VS/R	Voltage S/R on/off		2	-	6	-
	$T_{Turn\text{-}on}$	Turn-on delay time		-	-	6	µs
	$T_{Turn\text{-}off}$	Turn-off delay time		-	-	6	µs
	I_{OVC}	-		2	-	4.2	A
	$T_{FILTEROVC}$	Over current filtering time	Tested by scan	2	3	4	µs
	$T_{FILTERdiagoff}$	Filtering open load and short to GND diag. off	Tested by scan	8	10	12	µs
	T_{d_mask}	Diagnosis mask delay after switch-off	Tested by scan	350	400	450	µs
	$PW_{clampSP}$	Clamp single pulse	I_{load} = 1 A; single pulse(1)	-	-	25	mJ
	$PW_{clampRP}$	Clamp repetitive pulses	Reliability note: I_{load} = 0.6 A Freq =10 Hz; 36 Mpulse (1000h)	-	-	12	mJ
	IOUT_PD	Output diagnostic pull down current off state	Vpin = 5 V (1)	50	-	110	µA
	IOUT_PU	Output diagnostic pull up current off state	(1)	-210	-	-108	µA
	ΔV_{clamp}	Delta clamping voltage between low side to be parallelized		-250	-	+250	mV

1. Not to be tested, already covered by single low side measure and guaranteed by design.

Electrical characteristics of [OUT21], [OUT23], [OUT25], [OUT26] when configured as single power stages

If necessary an external free-wheeling diode must be used for the High side drivers.

Table 37. Electrical characteristics of [OUT21], [OUT23], [OUT25], [OUT26] when configured as single power stages

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Out 21,23,25,26	I_{max}	Output current	Not tested	-	0.6		A
	$R_{DS\text{-}on\ LSd}$	Drain source resistance	I_{load} = 0.6 A	-	-	1.5	Ω
	$IOUT_{lk}$	Output leakage current	Vpin = GND, VB = 13.5 V	-	-	10	µA
	VS/R	voltage S/R on/off	R = 21 Ω, C = 10 nF; from 70% to 20% of V_{OUT}	2	-	6	-
	$T_{Turn\text{-}on\_LSd}$	Turn-on delay time	From command to 70% V_{OUT} Load: 21 Ω, 10 nF	-	-	6	µs
	$T_{Turn\text{-}off\_LSd}$	Turn-off delay time	From command to 20% V_{OUT} Load: 21 Ω, 10 nF	-	-	6	µs

Diagnosis characteristic of [OUT21], [OUT23], [OUT25], [OUT26] when configured as single power stages

Table 38. Diagnosis characteristic of [OUT21], [OUT23], [OUT25], [OUT26] when configured as single power stages

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Out 21, 23, 25, 26	$R_{open\ load}$	Min resistor value open load detection	Not tested	500	-	-	kΩ
	I_{OVC}	Over current threshold	-	1		2	A
	$T_{FILTEROVC}$	Over current filtering time	Tested by scan	2	4	5	µs
	$T_{FILTERdiaggoff}$	Filtering open load and short to GND diag. off	Tested by scan	7	-	13	µs
	T_{d_mask}	Diagnosis mask time after switch-off	Tested by scan	1.2	-	1.6	ms
	$V_{OUTOPEN}$	Output open load voltage	Open load condition	2.3	-	2.7	V
	V_{HVT}	Output short-circuit to VB Voltage range threshold	-	$V_{OUTOPEN}$ +160mV	-	3	V
	V_{LVT}	Open load threshold voltage	-	1.9	-	$V_{OUTOPEN}$ -200mV	V
	I_{OUT_PD}	Output diagnostic pull down current off state	Vpin = 5 V	160	240	320	µA
	I_{OUT_PU}	Output diagnostic pull up current off state	Vpin = GND	30	50	70	µA
	I_{tOPEN}	Open load threshold current	-	100	-	200	-

Table 38. Diagnosis characteristic of [OUT21], [OUT23], [OUT25], [OUT26] when configured as single power stages (continued)

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
OUT21, 25	T_{HOLD}	Switch on to off delay during low battery voltage operation. Tested by SCAN	-	400	-	800	ms
	VB_LV	VB voltage threshold for low battery function	-	-	-	4.15	V

Note: When power stages are configured in parallel mode, some parameters change depending on CONFIG_REG7 and CONFIG_REG10 registers (refer to register configuration Table 39 & 40).

(CPS) CONFIG_REG10 (WR_CPS command 110011)

Table 39. CPS table single mode parallelism

Register bit	7	3	2	1	0	If not specified Output Drivers are set as single (not in parallel with any other) Over Current mask time increased to 8 µs (bit 6…4 set Low, they can be combined as per next table)	Enable by	Diagn on
2Low	0	0	0	1	0	OUT22 and OUT24 Low side Parallel	OUT24	OUT22
2Low 2Low	0	0	1	0	0	OUT22 and OUT24 Low side Parallel OUT27 and OUT28 Low side Parallel	OUT24 OUT27	OUT22 OUT27
4Low	0	1	0	0	0	OUT22 and OUT24 and OUT27 and OUT28 Low side Parallel	OUT24	OUT22
2High	0	0	1	1	0	OUT21 and OUT23 High side Parallel	OUT23	OUT21
2High 2high	0	1	1	1	0	OUT21 and OUT23 High side Parallel OUT25 and OUT26 High side Parallel	OUT23 OUT25	OUT21 OUT25
4High	0	1	0	1	0	OUT21 and OUT23 and OUT25 and OUT26 High side Parallel	OUT23	OUT21
3High	1	0	1	0	0	OUT23 and OUT25 and OUT26 High side Parallel	OUT23	OUT25
3Low	1	1	1	0	0	OUT24 and OUT27 and OUT28 Low side Parallel	OUT24	OUT24

Table 40. CPS table combined mode parallelism

Register bit	7	6	5	4	3	2	1	0	Over current mask time increased to 8 µs	Enable by	Diagn on
2Low 2High	0	0	0	1	0	0	1	0	OUT22 and OUT24 Low side Parallel OUT25 and OUT26 High side Parallel	OUT24 OUT25	OUT22 OUT25
2Low 2Low 2High	0	0	0	1	0	1	0	0	OUT27 and OUT28 Low side Parallel OUT22 and OUT24 Low side Parallel OUT25 and OUT26 High side Parallel	OUT27 OUT24 OUT25	OUT27 OUT24 OUT25
3Low 3High	1 1	1 0	1 1	1 0	0 1	1 1	0 0	0 0	OUT24 and OUT27 and OUT28 Low side Parallel OUT23 and OUT25 and OUT26 High side Parallel	OUT24 OUT23	OUT24 OUT25

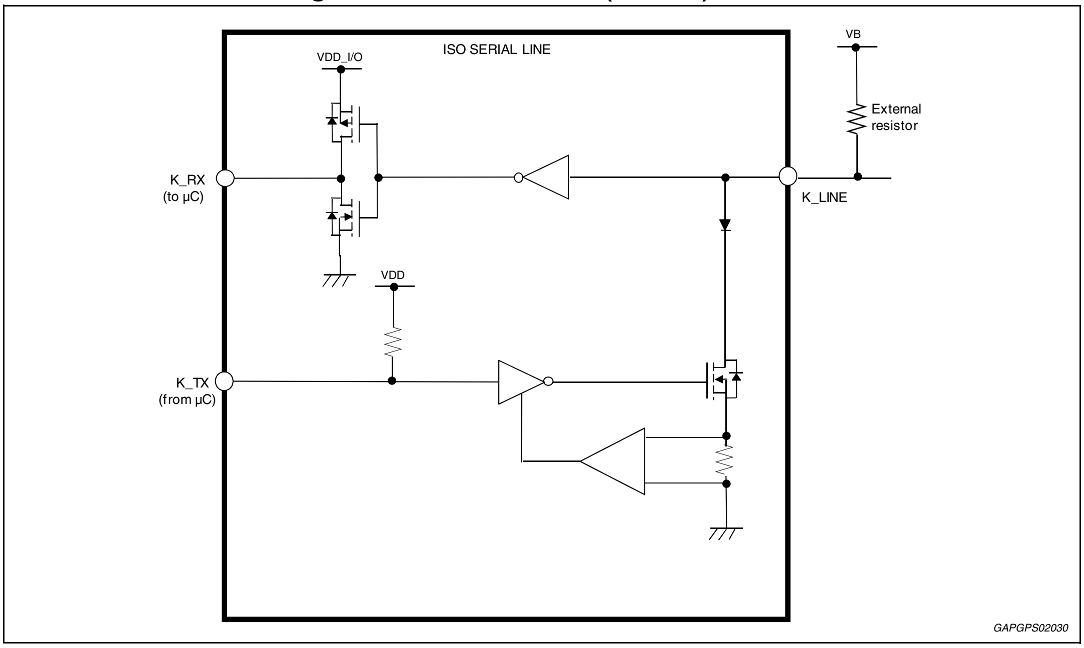
Table 40. CPS table combined mode parallelism (continued)

Register bit	7	6	5	4	3	2	1	0	Over current mask time increased to 8 μs	Enable by	Diagn on
4Low 4High	0 0	1 1	0 0	0 1	1 1	0 0	0 1	0 0	OUT22 and OUT24 and OUT27 and OUT28 Low side Parallel OUT21 and OUT23 and OUT25 and OUT26 High side Parallel	OUT24 OUT23	OUT22 OUT21
2Low 2High	0	0	1	1	0	1	1	0	OUT27 and OUT28 Low side Parallel OUT21 and OUT23 High side Parallel	OUT27 OUT23	OUT27 OUT21
2Low 2Low 2High 2High	0 0	1 0	1 1	1 0	0 1	1 1	0 1	0 0	OUT22 and OUT24 Low side Parallel OUT27 and OUT28 Low side Parallel OUT21 and OUT23 High side Parallel OUT25 and OUT26 High side Parallel	OUT24 OUT27 OUT23 OUT25	OUT22 OUT27 OUT21 OUT26
4Low 2High	0	1	0	1	0	1	1	0	OUT22 and OUT24 and OUT27 and OUT28 Low side Parallel OUT21 and OUT23 High side Parallel	OUT24 OUT23	OUT22 OUT21
4Low 2High	0	0	0	1	1	0	0	0	OUT22 and OUT24 and OUT27 and OUT28 Low side Parallel OUT25 and OUT26 High side Parallel	OUT24 OUT25	OUT22 OUT25
2Low 4High	0	1	0	0	0	0	1	0	OUT22 and OUT24 Low side Parallel OUT21 and OUT23 and OUT25 and OUT26 High side Parallel	OUT24 OUT23	OUT22 OUT25
2Low 4High	0	1	0	0	0	1	0	0	OUT27 and OUT28 Low side Parallel OUT21 and OUT23 and OUT25 and OUT26 High side Parallel	OUT27 OUT23	OUT27 OUT25
Half Bridge 2Low 2High	1	0	1	1	0	1	1	0	OUT22 and OUT24 Low side Parallel OUT21 and OUT23 High side Parallel	OUT24 OUT23	OUT22 OUT21

Note: When those four single Lside and four single Hside are configured as parallel configuration, for example 2 single Lside stage to 1 Lside stage or 4 single Lside stage to 1 Lside stage, the Rdson could be 1/2 or 1/4 as one single stage, the over current threshold could be roughly double or 4 times as single stage, but the over current detected filter time will be increased to 2 times as single stage from 4 μs typical to 8 μs typical by L9779WD itself, because each single stage will switch on its own overcurrent threshold no matter the configuration for off stage diagnostic, all thresholds will be kept as single stage whatever the configuration of those 4 Lside/Hside.

6.14 ISO serial line (K-LINE)

Figure 56. ISO serial line (K-LINE) circuit



6.14.1 ISO serial line (K-LINE) functionality description

The ISO serial line is an interface containing one bidirectional line for communication between the µP and an external diagnosis tester or anti-theft device. In case of ground loss the outputs K_LINE get in high impedance state and can withstand a negative voltage up to -18 V. Short circuit to Vb protection is provided: if the K_LINE pin is shorted to battery the output is switched off after a delay of tfilter_K_LINE and it is necessary an input change to turn on it again.

The negative transition at K_LINE pin can be driven with slew-rate limitation for optimizing the EMI behavior. This slew-rate limitation must be enabled via the ISO_SRC bit.

The K_TX signal is ignored (K_LINE pin to high level) until the RST pin is asserted.

KLINE can work up to 250 kHz input frequency in typical application condition.

Table 41. ISO serial line (K-LINE) functionality electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
K_TX	V_{KTXL}	K_TX input low voltage	-	-0.3	-	1.1	V
	V_{KTXH}	K_TX input high voltage	-	2.3	-	VDD +0.3	V
	R_{TX_KPU}	TX_KLINE pull-up resistor	-	50	-	250	kΩ
	I_{TXsink}	Transmitter input sink current	K_LINE = 0, K_TX = High	-	-	5	µA

Table 41. ISO serial line (K-LINE) functionality electrical characteristics (continued)

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
K_LINE	V_{KOUTL}	Transmitter output low voltage	Isink_K_LINE = 35 mA, K_TX = Low	-1	-	1.5	V
	I_{KOS}	Transmitter short circuit current	K_LINE = VB, K_TX = Low	60	-	165	mA
	$T_{filter\_K\_LINE}$	Overcurrent filter time	Test by SCAN	7	10	13	µs
	I_{KREV}	Reverse battery or GND loss current	Key_on = VB = 0 V K_LINE = -18 V	-	-	10	mA
		Under voltage current	Key_on = High, K_TX = Low, VB = 13.5 V, K_LINE = -1V	-	-	1	mA
	V_{KH}	Receiver input hysteresis	-	0.08*VB	-	0.3*VB	V
	V_{KINH}	Receiver input high voltage	-	0.7* VB	-	VB	V
	V_{KINL}	Receiver input low voltage	-	-1	-	0.35*VB	V
	V_{K_SR}	K_line voltage slew - rate	From off to on: VB = 13.5 V, R_{ext} = 510 Ω C = 10 nF to GND	5.3	-	8.8	V/µs
			From on to off	Depends on external RC load			-
	T_fT	Transmitter fall time	CK_LINE = 10 nF, RK_LINE = 510 Ω	-	-	10	µs
K_RX	V_{KRXL}	K_RX output low voltage	VDD_IO = 5 V or 3.3 V I_{sink} = 2 mA	-	-	0.5	V
	V_{KRXH}	K_RX output high voltage	VDD_IO = 5 V or 3.3 V I_{source} = 2 mA	VDD_IO -0.5	-	-	V
	T_rK	K_RX rise time	from 10% to 90% With 20 pF capacitive load	-	-	2	µs
	T_fK	K_RX fall time	from 90% to 10% 20 pF capacitive load	-	-	2	µs
K_TX, K_LINE	Tp_HLT	Transmitter turn-on delay time	CK_LINE = 10 nF, RK_LINE = 510 Ω	-	-	5	µs
K_LINE, K_RX	TpHLK	K_RX turn-on delay time	C_{load} = 20 pF	-	-	4	µs
	TpLHK	K_RX turn-off delay time	C_{load} = 20 pF	-	-	4	µs

Figure 57. ISO serial line switching waveform

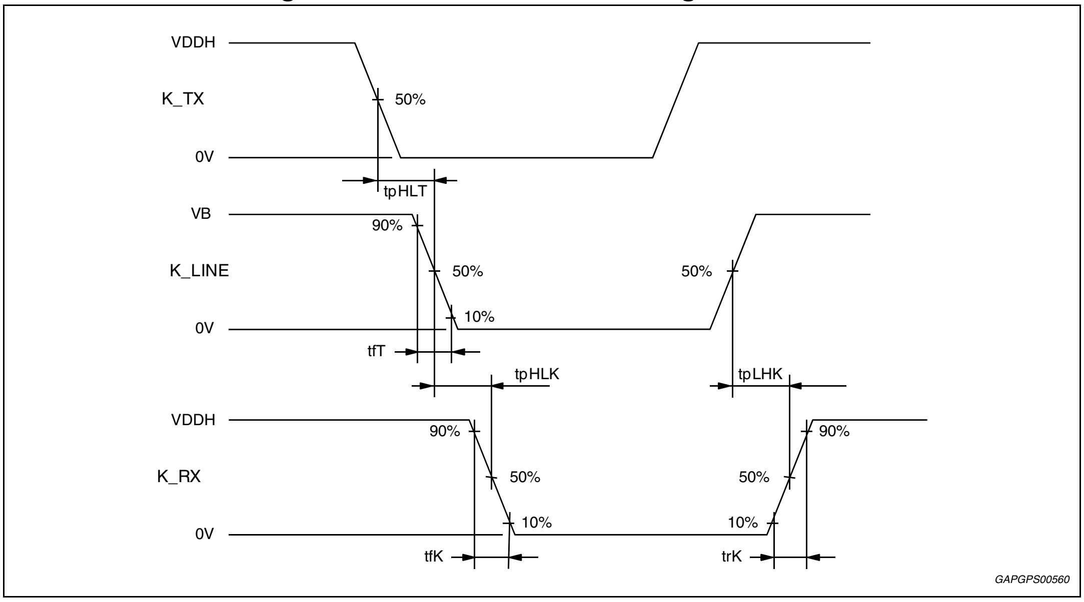
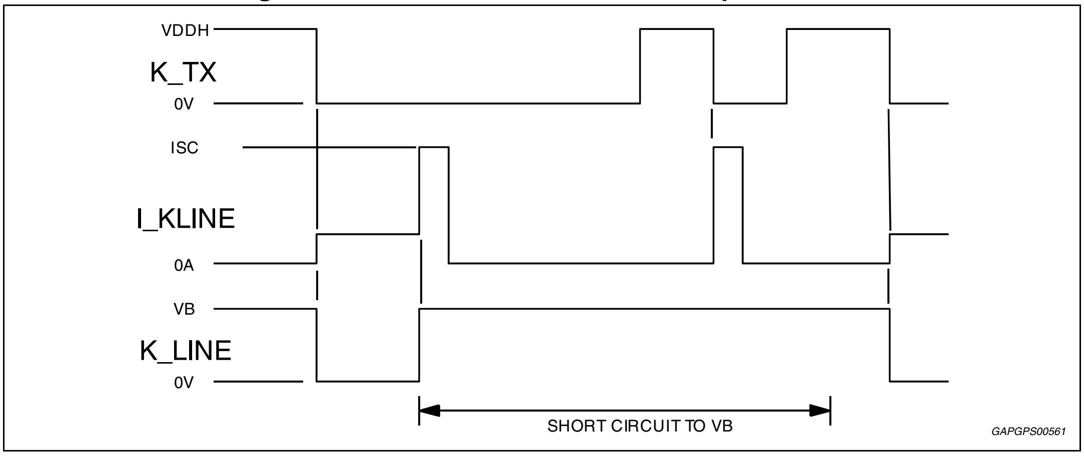
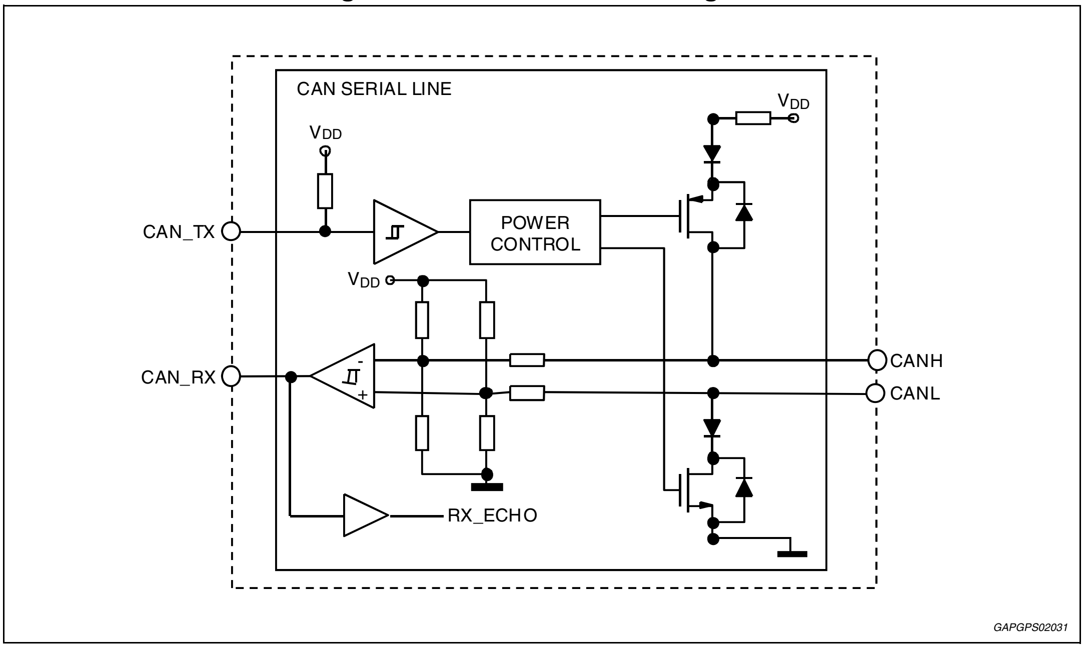


Figure 58. ISO serial line: short circuit protection



6.15 CAN transceiver

Figure 59. CAN transceiver diagram



6.15.1 CAN transceiver functionality description

The CAN bus transceiver allows the connection with a microcontroller through a high speed CAN bus with transmission rates up to 1Mbit/s. The transceiver has one logic input pin (CAN_TX), one logic output pin (CAN_RX) and two input/output pins for the electrical connections to the two bus wires (CANH and CANL). The microcontroller sends data to the CAN_TX pin and it receives data from the CAN_RX pin.

In case of power loss (VB pin disconnected) or ground loss (GND pins disconnected), the transceiver doesn't disturb the communication of the remaining transceivers connected to the bus. If CANL is shorted to ground, the transceiver is able to operate with reduced EMI/RFI performances.

TX or RX=0 means Dominant state of CANH and CANL; TX or RX=1 means Recessive state compliant to ISO11898-2.

- Speed communication up to 1Mbit/s
- Function range from +40 V to -18 V DC at CAN pins
- GND disconnection fail safe at module level
- GND shift operation at system level
- ESD: Immunity against automotive transients per ISO7637 specification
- Matched output slopes and propagation delay.

The CAN_TX signal is ignored (CAN to recessive state) until the RST pin is asserted.

CAN error handling

The L9779WD provides the following 4 error handling features that are realized in different stand alone CAN transceivers / micro controllers to switch the application back to normal operation mode.

If one of the below fault happens the status bit CAN_ERROR is set.

The error handling features can be disabled through the CAN_ERR_DIS bit.

1. Dominant CAN_TX time out

   If CAN_TX is in dominant state (low) for $t > t_{dom\ (TxD)}$ the transmitter will be disabled, status bit will be latched and can be read and cleared by MSC. The transmitter remains disabled until the status register is cleared.
2. CAN permanent recessive

   If CAN_TX changes to dominant (low) state but CAN bus (CAN_RX pin) does not follow for 4 times, the transmitter will be disabled, status bit will be latched and can be read and cleared by MSC. The transmitter remains disabled until the status register is cleared.
3. CAN permanent dominant

   If the CAN bus state is dominant (low) for $t > t_{CAN}$ a permanent dominant status will be detected. The status bit will be latched and can be read and cleared by MSC. The transmitter will not be disabled.
4. CAN_RX permanent recessive

   If CAN_RX pin is clamped to recessive (high) state, the controller is not able to recognize a bus dominant state and could start messages at any time, which results in disturbing the overall bus communication.

   Therefore, if RX_ECHO does not follow CAN_TX for 4 times the transmitter will be disabled. The status bit will be latched and can be read and optionally cleared by MSC. The transmitter remains disabled until the status register is cleared.

CAN transceiver electrical characteristics

Table 42. CAN transceiver electrical characteristics

Pin	Symbol	Description	Test conditions	Min	Typ	Max	Unit
CAN_TX	V_{TX_CANLOW}	Input voltage dominant level	Active mode	-0.3	-	1.1	V
	$V_{TX\_CANHIGH}$	Input voltage recessive level	Active mode	2.3	-	VDD +0.3	V
	V_{TX_CANHYS}	$V_{TX\_CANHIGH}$- V_{TX_CANLOW}	Active mode	0.25	0.5	-	V
	R_{TX_CANPU}	CAN_TX pull up resistor	Active Mode	50	-	250	kΩ
CAN_RX	V_{RX_CANLOW}	Output voltage dominant level	Active mode, VDD_IO = 5 V or 3.3 V, 2 mA	-	-	0.5	V
	$V_{RX\_CANHIGH}$	Output voltage recessive level		VDD_IO -0.5	-	-	V

Table 42. CAN transceiver electrical characteristics (continued)

Pin	Symbol	Description	Test conditions	Min	Typ	Max	Unit
CAN_H CAN_L	$V_{CANHdom}$	CANH voltage level in dominant state	Active mode; $V_{TXCAN} = V_{TXCANLOW}$; $R_L = 60\ \Omega$	2.75	-	4.5	V
	$V_{CANLdom}$	CANL voltage level in dominant state		0.5	-	2.25	V
	$V_{DIFF,domOUT}$	Differential output voltage in dominant state: $V_{CANHdom}$- $V_{CANLdom}$		1.5	-	3	V
	V_{CM}	Driver symmetry: $V_{CANHdom}+V_{CANLdom}$	$R_L = 60\ \Omega$; $C_{SPLIT} = 4.7$ nF;	0.9* V_{CANSUP}	V_{CANSUP}	1.1* V_{CANSUP}	V
	$V_{CANHrec}$	CANH voltage level in recessive state	$V_{TX\_CAN} = V_{TX\_CANHIGH}$; No load	2	2.5	3	V
	$V_{CANLrec}$	CANL voltage level in recessive state		2	2.5	3	V
	$V_{DIFF,recOUT}$	Differential output voltage in recessive state: $V_{CANHrec}$- $V_{CANLrec}$		-50	-	50	mV
	$V_{CANHL,CM}$	Common mode bus voltage	Application info: Measured with respect to the ground of each CAN node	-12	-	+12	V
	$I_{OCANH,dom}$	CANH output current in dominant state	Active mode; $V_{TX\_CAN} = V_{TX\_CANLOW}$; $V_{CANH} = 0$ V	-100	-75	-45	mA
	$I_{OCANL,dom}$	CANL output current in dominant state	Active mode; $V_{TX\_CAN} = V_{TX\_CANLOW}$; $V_{CANL} = 5$ V	45	75	100	mA
	$I_{Leakage}$	Input leakage current	Unpowered device; $V_{BUS} = 5$ V	0	-	250	µA
	R_{in}	Internal resistance	Active mode $V_{TX\_CAN} = V_{TX\_CANHIGH}$; No load	25	-	45	kΩ
	$R_{in,diff}$	Differential internal resistance	Active mode & STBY mode; $V_{TX\_CAN} = V_{TX\_CANHIGH}$; No load	50	-	85	kΩ
	C_{in}	Internal capacitance	Guaranteed by design	-	20	-	pF
	$C_{in,diff}$	Differential internal capacitance	Guaranteed by design	-	10	-	pF
	V_{THdom}	Differential receiver threshold voltage recessive to dominant state	Active mode	-	-	0.9	V

Table 42. CAN transceiver electrical characteristics (continued)

Pin	Symbol	Description	Test conditions	Min	Typ	Max	Unit
CAN_H CAN_L	V_{THrec}	Differential receiver threshold voltage dominant to recessive state	Active mode	0.5	-	-	V
	SR_H	CANH slew rate between 10% and 90%	-	5	-	35	V/µs
	SR_L	CANL slew rate between 10% and 90%	-	5	-	35	V/µs
	DIFF_SR	Slew rate difference between CANH and CANL	-	-	-	60	%
	SR_{VDIFF}	Slew rate of $V_{diff} = V_{CANH}$-V_{CANL}	-	12	-	100	V/µs
	V_{THhys}	V_{THdom} - V_{THrec} hysteresis	-	25	-	50	mV

Table 43. CAN transceiver timing characteristics

Symbol	Description	Test conditions	Min	Typ	Max	Unit
$t_{TXpd,hl}$	Propagation delay TX_CAN to RX_CAN (High to Low)	Active mode; 50% V_{TX_CAN} to 50% V_{RX_CAN}; C_L=100 pF; C_{RX_CAN} = 15 pF; R_L = 60 Ω; Guaranteed by design.	0	-	255	ns
		C_{RX_CAN} = 100 pF @T_{room} and T_{cold}	-	-	265	ns
		C_{RX_CAN} = 100 pF @T_{hot}	-	-	275	ns
$t_{TXpd,lh}$	Propagation delay TX_CAN to RX_CAN (Low to High)	Active mode; 50% V_{TX_CAN} to 50% V_{RX_CAN}; C_L = 100 pF; C_{RX_CAN} = 15 pF; R_L = 60 Ω; Guaranteed by design.	0	-	255	ns
		C_{RX_CAN} = 100 pF @T_{room} and T_{cold}	-	-	265	ns
		C_{RX_CAN} = 100 pF @T_{hot}	-	-	275	ns
$t_{dom(TX\_CAN)}$	TX_CAN dominant time-out	Tested by scan	525	700	875	µs
t_{CAN}	CAN permanent dominant time-out	Tested by scan	-	700	-	µs

Figure 60. CAN transceiver switching waveforms

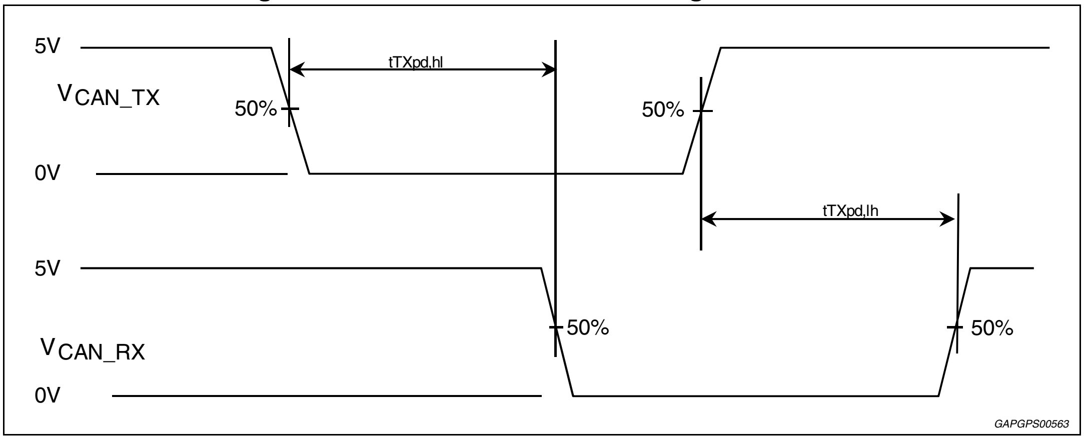
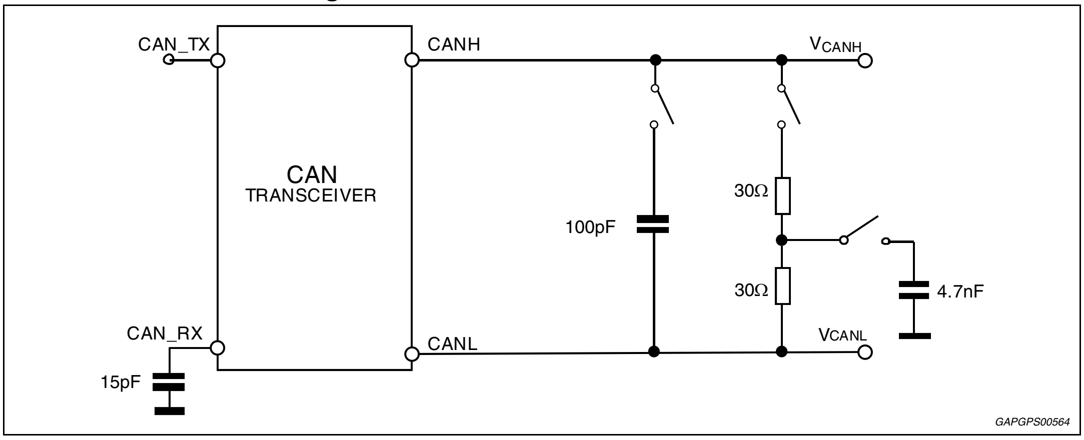
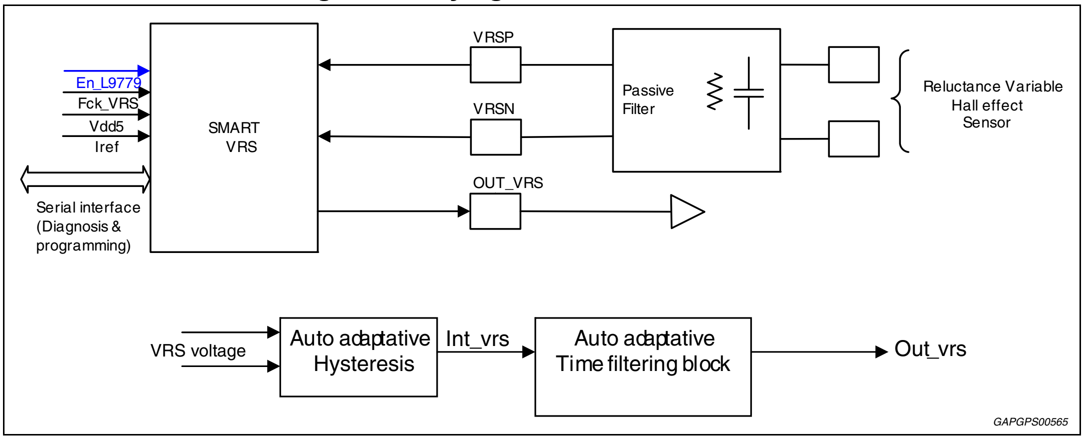


Figure 61. CAN transceiver test circuit



6.16 Flying wheel interface function

Figure 62. Flying wheel interface circuit



6.16.1 Flying wheel interface functionality description

The flying wheel interface is an interface between the microprocessor and the flying wheel sensor: it handles signals coming from magnetic pick-up sensor or Hall Effect sensor and feeds the digital signal to Microcontroller that extracts flying wheel rotational position, angular speed and acceleration.

This circuit implements an auto adaptative hysteresis and filter time algorithm that can be configured via MSC using VRS_mode bit.

If the auto adaptive hysteresis is OFF the hysteresis value can be selected using VRS_Hyst bit.

If fault is present (OL / SC GND / SC VB) the functionality is not guaranteed.

6.16.2 Auto-adaptative sensor filter

Two main VRS configuration sets are available for VRS, by means of CONFIG_REG1 register bit 1: fully adaptive VRS mode and limited adaptive VRS mode (default: 0).

For VRS configurations in both limited and fully adaptive mode, CONFIG_REG5 is used.

Auto-adaptative hysteresis (fully adaptive mode)

When enabled the auto adaptative hysteresis works as described below.

Input signals difference is obtained through a full differential amplifier; its output, DV signal, is fed to peak detection circuit and then to A/D converter implemented with 4 voltage comparators (5 levels) (Pvi).

Output of A/D is sent to Logic block (*Table 45: Hysteresis threshold precision*) that implements correlation function between Peak voltage and hysteresis value; hysteresis value is used by square filtering circuit which conditions DV signal.

Figure 63. Auto adaptative hysteresis diagram

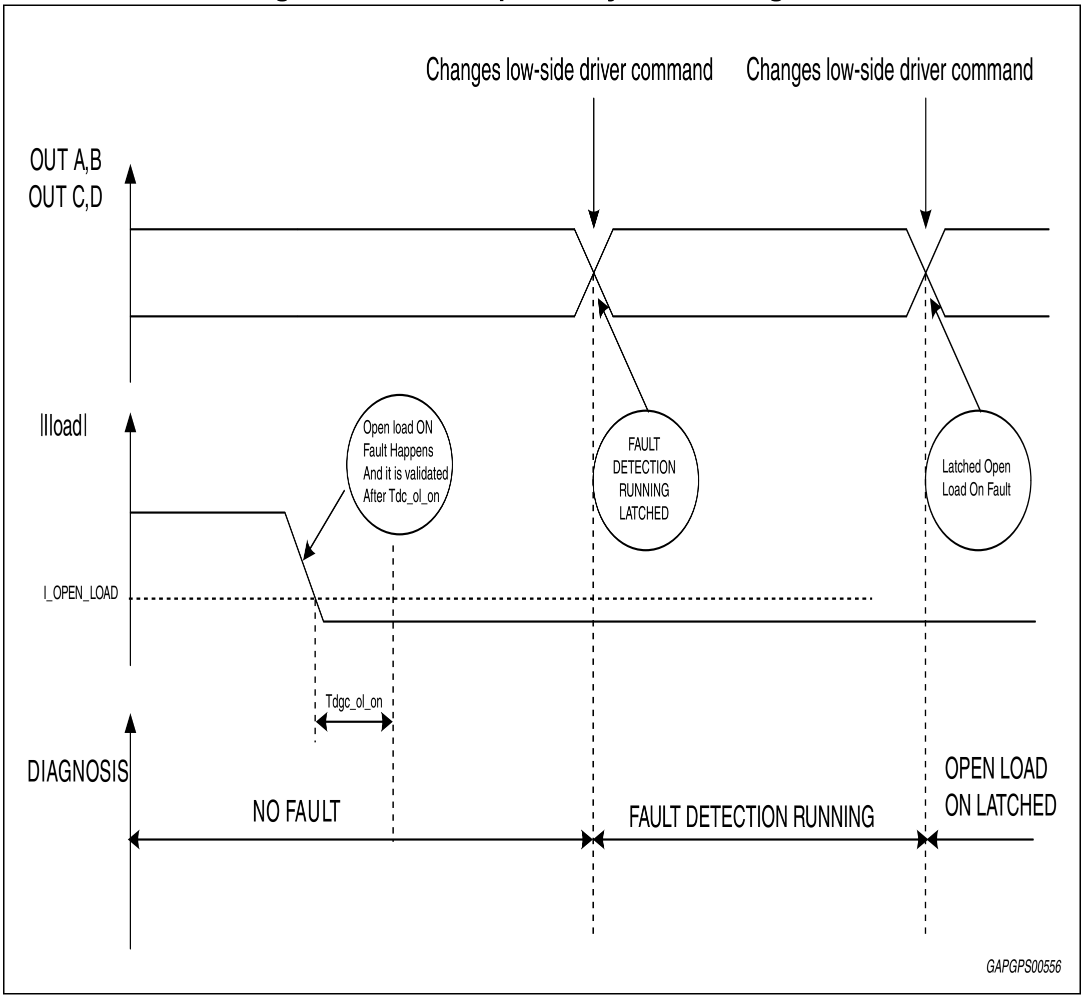


Figure 64. VRS interface block diagram

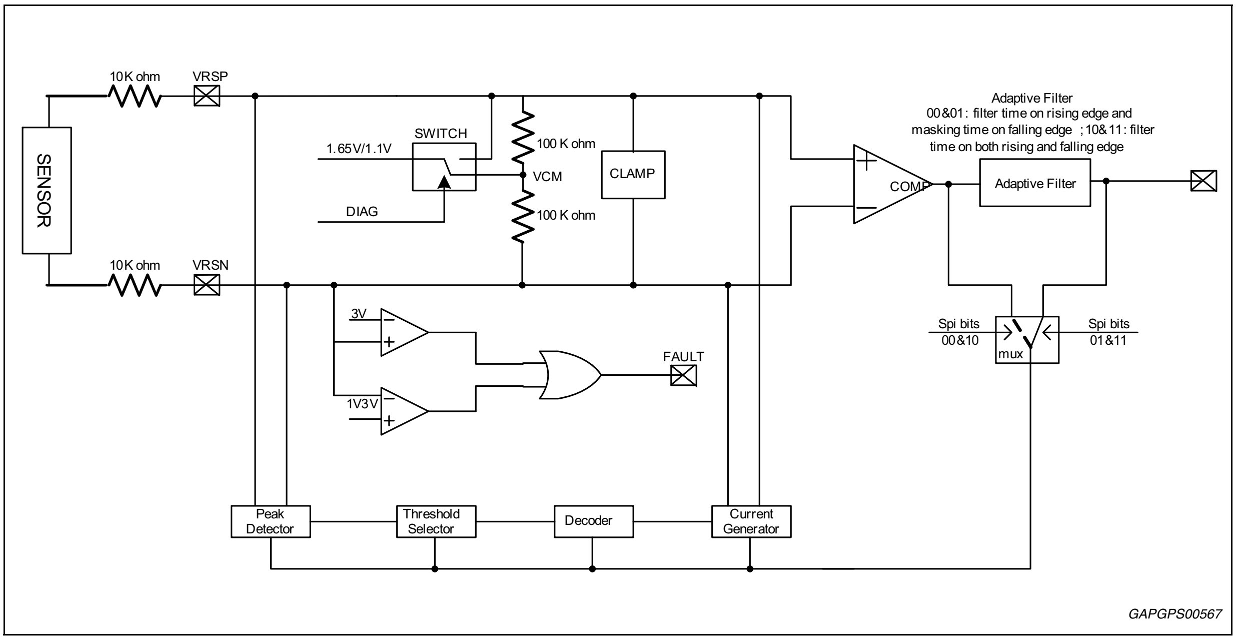


Table 44. Pick voltage detector precision

Pick voltage [PV]	Min	Typ	Max	Unit
PV1	600	930	1300	mV
PV2	1200	1600	1950	mV
PV3	1990	2300	2660	mV
PV4	2600	3000	3380	mV

Table 45. Hysteresis threshold precision

Hysteresis current [H]	Value			Unit	Correspondent value on 20 kΩ ext. resistor	Unit
	Min	Typ	Max		Typ	
HI1	3	5	7	µA	100	mV
HI2	7	10	13.5	µA	200	mV
HI3	12.8	17	23	µA	347	mV
HI4	23	32	41	µA	644	mV
HI5	35	51	65	µA	1020	mV

Note: For a single IC, there is no overlap of parameters PVX (PV1<PV2<PV3<PV4)and HIX(HI1<HI2<HI3<HI4<HI5), which are guaranteed by design

Auto-adaptative time filter (fully adaptive mode)

This characteristic is useful to set the best internal filter time depending on the input signal frequency.

Tfilter time depends on duration of the previous period Tn according to the following formula:

Tfilter(n+1) = 1/32*Tn if Int_vrs > Tfilter(n)

The filtering time purpose is filtering very short spikes.

The digital filtering time is applied to internal squared signal (int_vrs), obtained by Voltage comparators.

The output of time filtering block is out_vrs signal.

The filtering time Tfilter is applied to int_vrs signal in two different ways:

- Rising edge: if int_vrs high level lasts less than Tfilter out_vrs is not set to high level

  In absence of any spikes during input signal rising edge out_vrs signal is expected with a delay of Tfilter time
- Falling edge: the falling edge of int_vrs is not delayed through time filtering block: after falling edge for a time Tfilter any other transition on int_vrs signal is ignored.

Tmaxfilter = 200 µs typ.
Tmin filter = 4 µs typ.

The default value after reset is Tmaxfilter.
The Tfilter function is reset by the enable of FLYING WHEEL function.

Figure 65. Auto-adaptive time filter (rising edge)

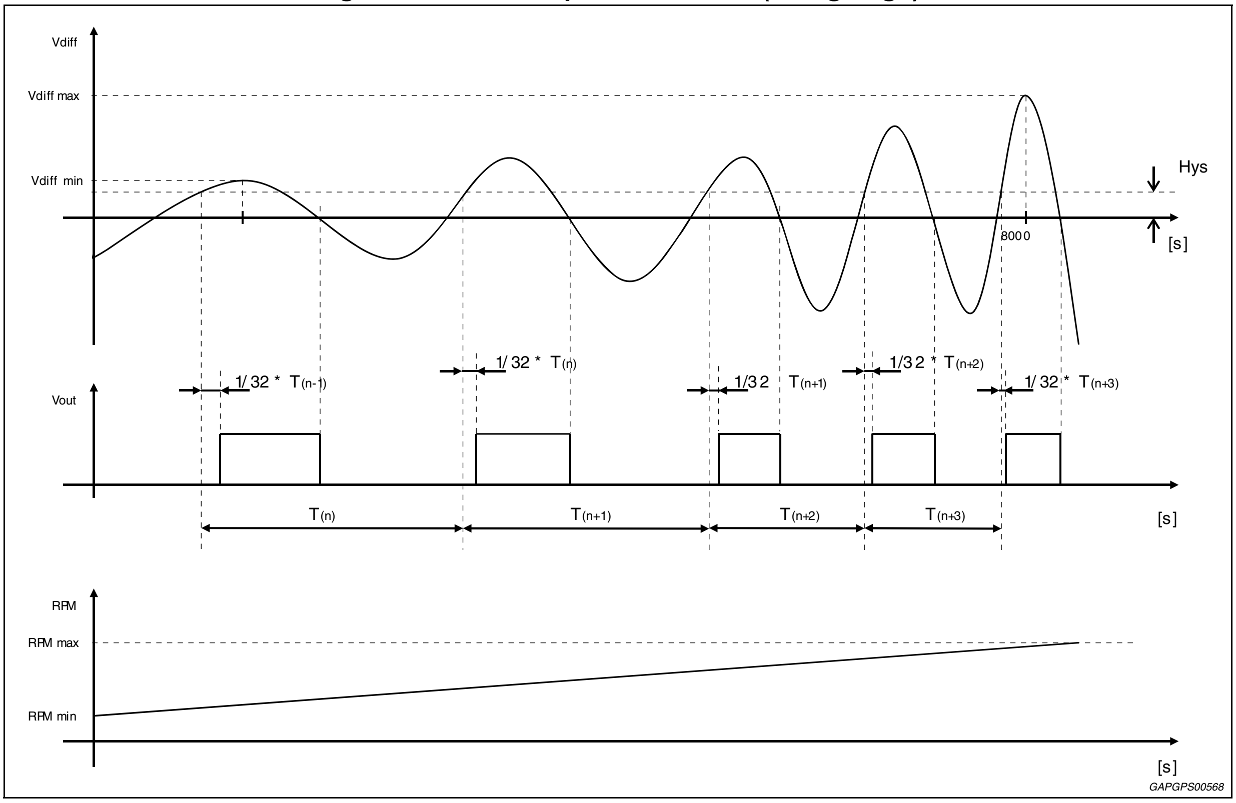
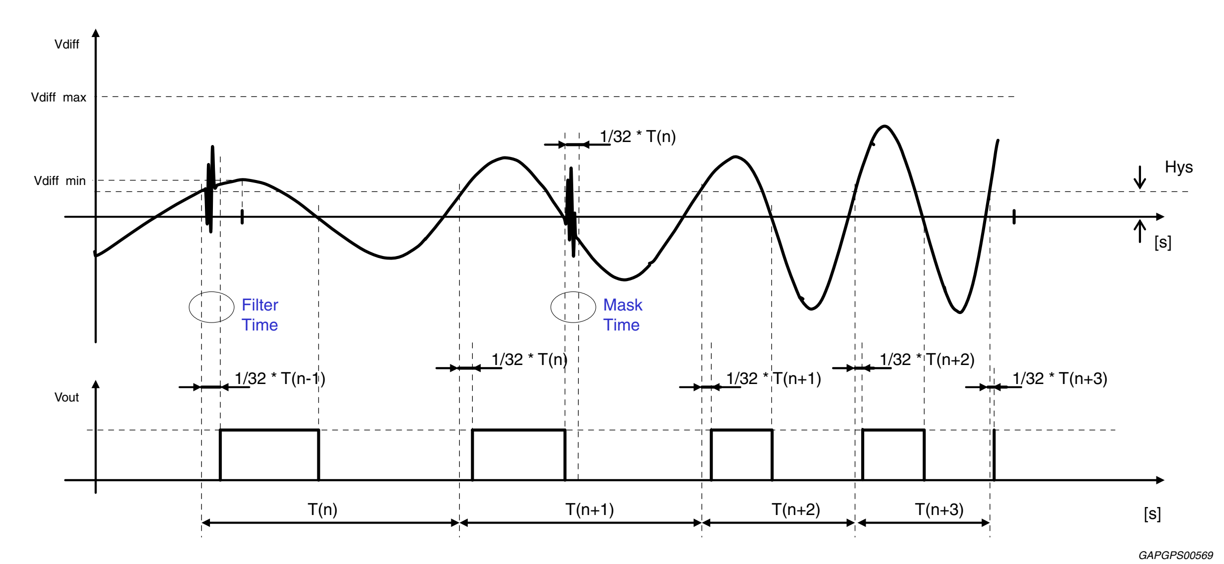


Figure 66. Adaptive filter function when the MSC bit are 00 or 01



Software option configuration requirement for VRS function:

By MSC command it is possible to configure different options of the VRS function:

– The hysteresis changing is driven by a feedback signal coming from COMP output OR from adaptive filter

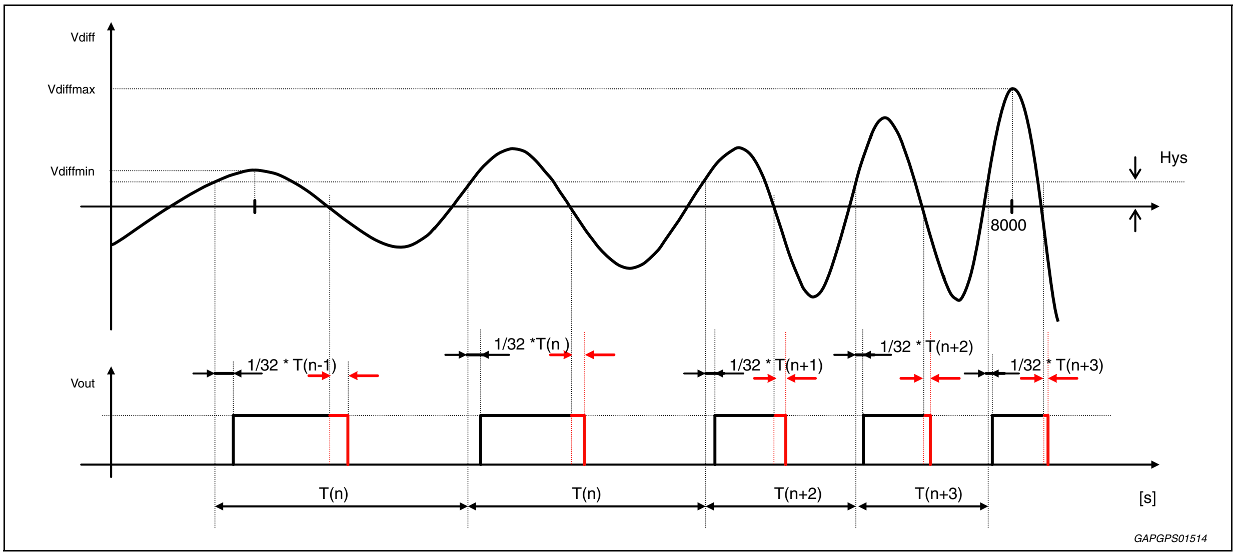
– The adaptive filter can be either on the rising edge or on both edges of the VRS output.

Table 46. MSC command possible configuration of different option of VRS function

MSC Bit	00	01	10	11(1)
Function	Feed back from COMP output. VRS input signal from low to high, add 1/ 32* Tn filter time. VRS output from high to low with 1/32 * Tn masking time.	Feed back from after adaptive filter block instead of from COMP output (specifically as shown in *Figure 67*) VRS output signal from low to high, add 1/32 * Tn filter tune. VRS output from high to low with 1/32 * Tn masking time.	VRS input signal from high to low, add 1/ 32* Tn filter time. VRS output from high to low with 1/32 * Tn filter time.	Realize 01 and 10 functions Feed back from after adaptive filter block instead of from COMP output. VRS output signal from low to high, add 1/ 32* Tn filter time. VRS output from high to low with 1/32 * Tn filter time. Feed back from after adaptive filter block instead of from COM output. VRS output signal from low to high, add 1/32 * Tn filter time. VRS output from high to low with 1/32 * Tn filter time.

1. If MSC CONFIG_REG7-bit4 is set (High) VRS filter time is fixed to 4 µs ±1.25 µs.

Figure 67. Adaptive Filter Function when the MSC bit is 10 or 11



Limited adaptive mode

Auto time adaptive filter is fixed to 4 µs (typical).

Auto amplitude adaptive filter is limited to a minimum hysteresis as set by related VRS register. Note that in case the VRS input amplitude is persistently lower than the minimum hysteresis setting, VRS output deadlock can be removed by setting CONFIG_REG5 bit5 to 1, which forces the hysteresis to 5 µA. This procedure is not glitch free. Once a new minimum hysteresis value has been set, CONFIG_REG5 bit5 must return to 0

VRS diagnostic is not available when limited adaptive mode is selected.

6.16.3 Application circuits

Figure 68. Variable reluctance sensor

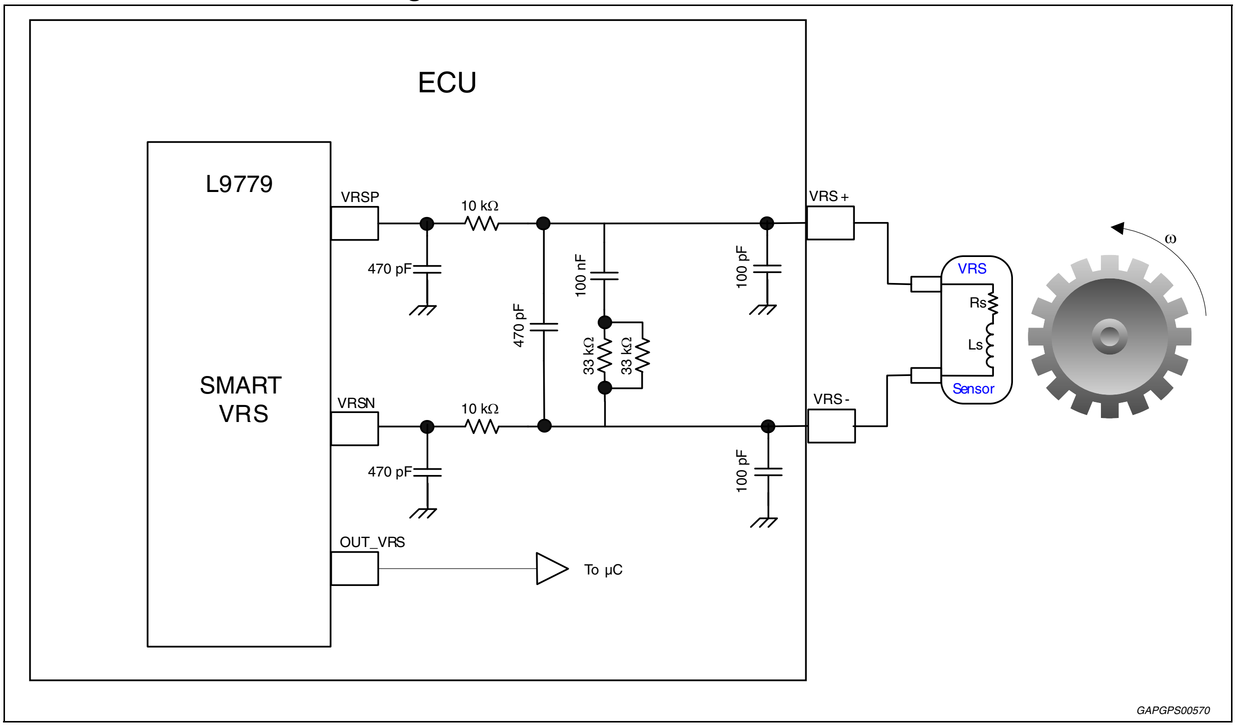


Figure 69. VRs typical characteristics

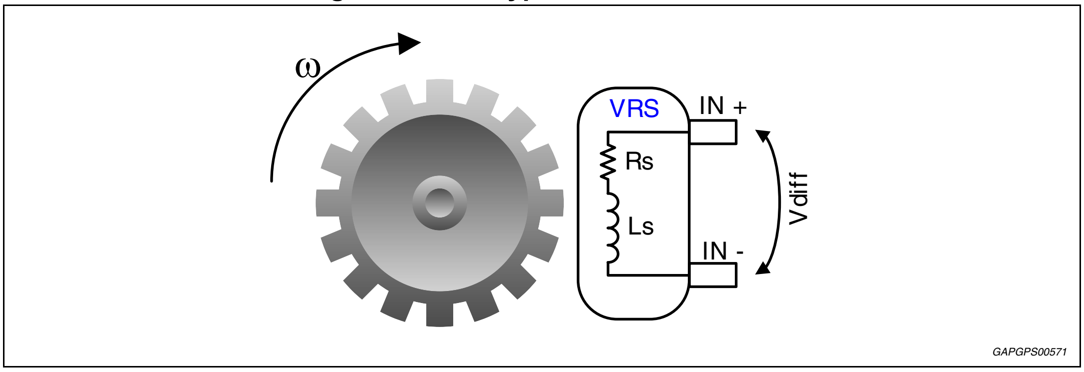


Table 47. VRs typical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Rs	Sensor resistance	300	600	1000	Ω
Ls	Sensor inductor	-	250	-	mH
Vdiff	Sensor output voltage	-200	-	+200	V
Tout	Output period	5000	-	100	µs

Figure 70. Hall effect sensor configuration 1

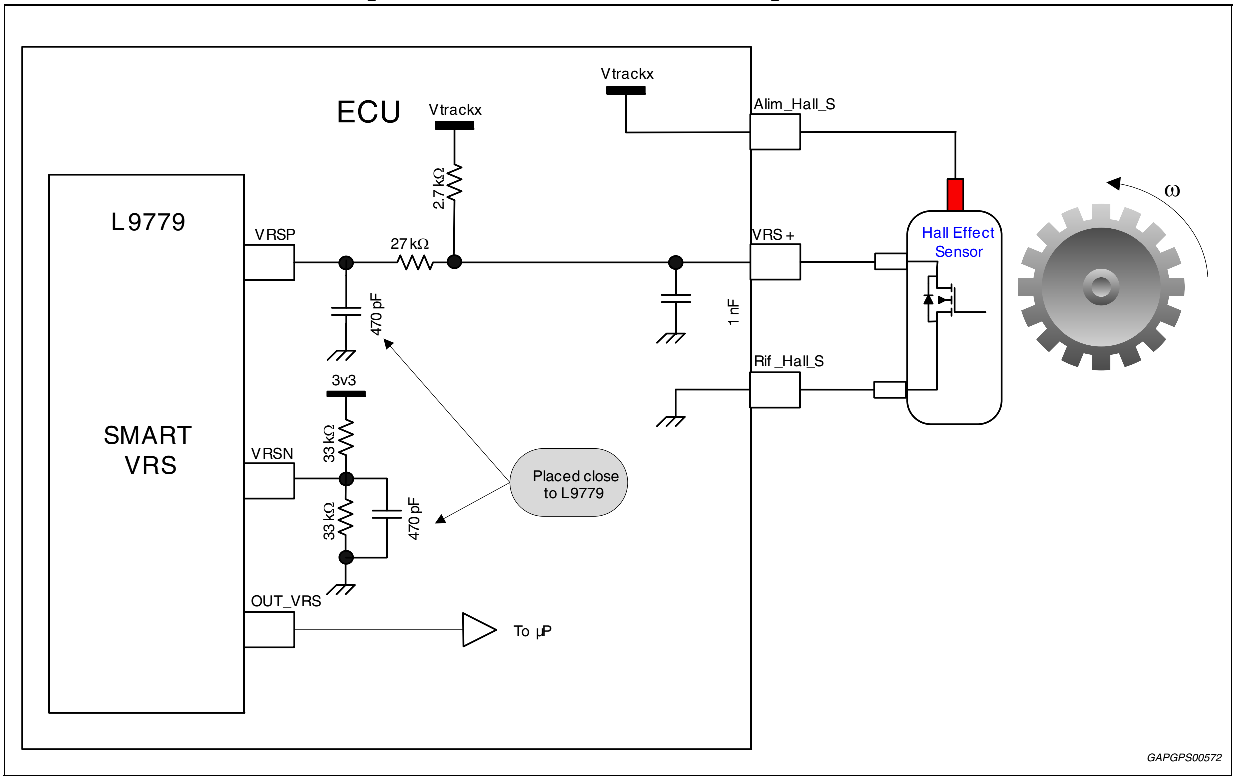
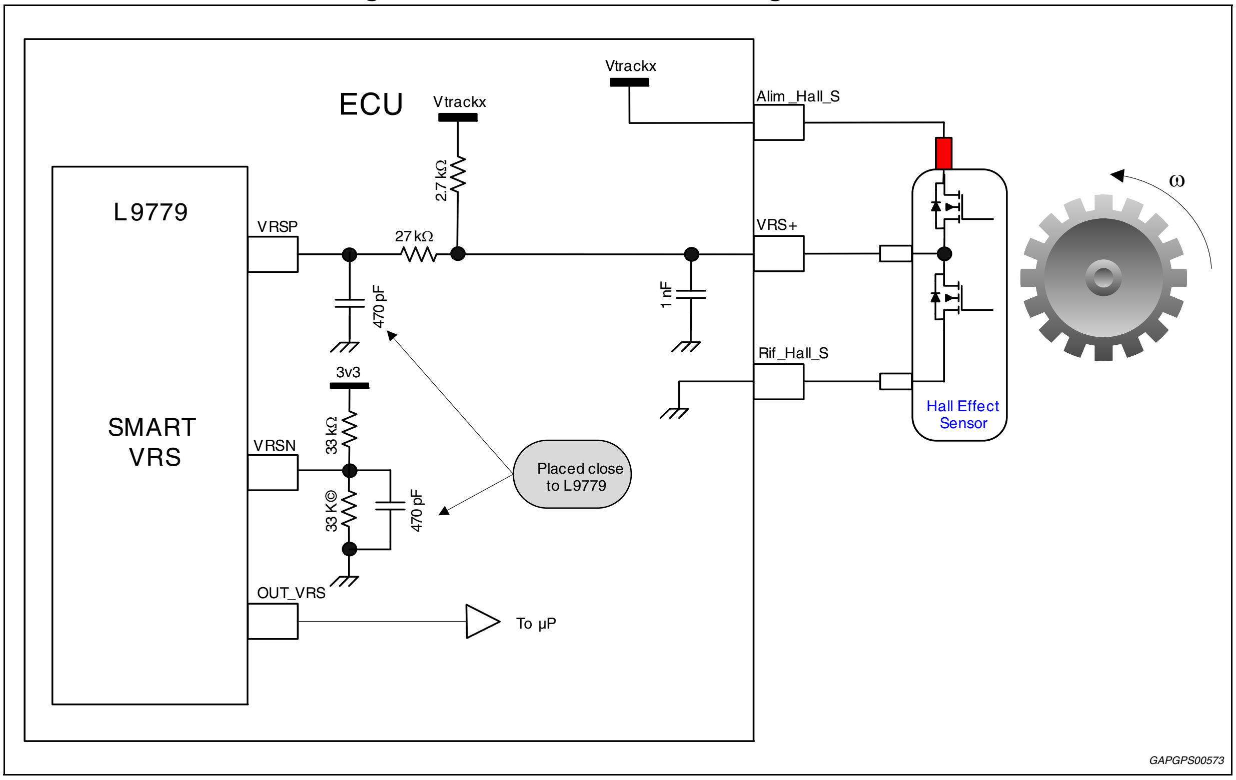


Figure 71. Hall effect sensor configuration 2



6.16.4 Diagnosis test

After the request of diagnosis by MSC, the diagnosis routine tests the sensor presence or vacancy and the short circuit to GND or Vbat. When the system is in diagnosis status the flying wheel interface function doesn't operate. The diagnosis procedure has an operation time of about min 5 ms due to the external transient.

The result of diagnosis routine is valid only if the engine is switched off and if the sensor is a variable reluctance sensor.

In the last operation of the diagnosis protocol writes the diagnosis result in VRSdiag bit and writes the operative status in VRSstatus bit. If a new request is sent the new value is overwritten.

Figure 72. Diagnosis test diagram

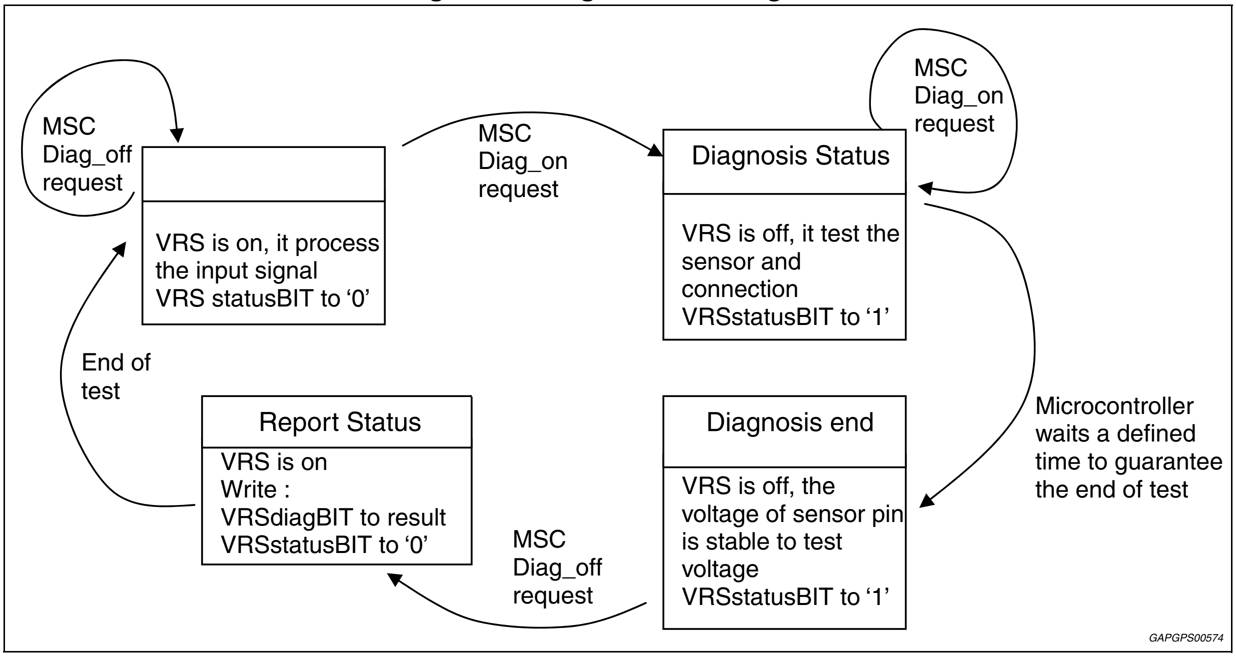


Table 48. Diagnosis test electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
VrsP VrsM	V_{iThL}	Input high-to-low differential threshold voltage	-	-50	0	50	mV
	V_{CM}	Common mode operating range	Not to be tested. It is an application note.	0	1.65	3	V
	V_{clpH}	Input high clamping voltage	|VRS_INP| = |VRS_INM| = 20 mA	3.3 -0.3	-	3.3 +0.3	V
	V_{clpL}	Input low clamping voltage	|VRS_INP| = |VRS_INM| = 20 mA	-1.5	-	-0.3	V
	$V_{openload}$	Output open load voltage	VRS_INP = VRS_INM $V_{openload}$ Mode R enabled	1.5	(3.3) /2	1.8	V

Table 48. Diagnosis test electrical characteristics (continued)

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
VrsP VrsM	I_{bvrsp}	Input bias current Vrsp	VRS_INP = Vopenload Mode R enabled	-	-	2	µA
	I_{bvrsm}	Input bias current V_{rsm}	VRS_INM = Vopenload Mode R enabled	-	-	2	µA
Out_ Vrs	V_{OL}	Output low voltage	VDD_IO = 5 V or 3.3 V Isink current = 2 mA	-	-	0.5	V
	V_{OH}	Output high voltage	VDD_IO = 5 V or 3.3 V Isource current = 2 mA	VDD_IO -0.5	-	-	V
	I_{lk_outvrs}	Input leakage current to GND	-	-	-	1	µA
		Input leakage current to VDD_IO	-	-	-	1	µA
	Td_on_outvrs	Delay on falling edge	Test Ext cap = 300pF	-	-	1	µs
	Td_off_outvrs	Delay on rising edge	Input signal Tperiod = 4 ms	-	-	150	µs
	T_r_Out_vrs	MRX rise time	Test Ext cap = 300 pF	-	-	150	ns
	T_f_Out_vrs	MRX fall time	Test Ext cap = 300 pF	-	-	150	ns
VrsP VrsM	$V_{outdiag}$	Output diag voltage	Vrs_INP = open; diag mode CONFIG_REG1 bit1 = 0	0,9	(3.3)/3	1.5	V
	$I_{outdiag}$	Output diag Current	Vrs_INP = open; Vrs_INM = GND; diag mode	50	65	80	µA
	V_{outsh} $V_{bdiag\ th}$	Output Short-circuit range to VBAT Open Load threshold	Vrs_INP = open; Vrs_INM = Vramp; diag mode	2,8	3	3,2	V
	$V_{outsh\ gnd\ diag\ th}$	Output Short-to GND range threshold	Vrs_INP = open; Vrs_INM = Vramp; diag mode	1.1	1.3	1.5	V

Note: *When VrsP and VrsM are both in input high clamping condition, the clamp voltage of VrsP is 30mV(typical) higher than VrsM.*

6.17 Monitoring module (watchdog)

Table 49. WDA_INT electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
WDA_INT	V_{WDA_low}	Output low voltage	3.5 V < VDD5 I_{WDA} < 4 mA	-	-	0.4	V
			2.2 V < VDD5 < 3.5V I_{WDA} < 1 mA	-	-	0.4	V
	I_{WDA}	Input leakage current	-	-	-	1	µA
	$V_{WDA\_in\_low}$	Input voltage low level	-	-0.3	-	1.1	V
	$V_{WDA\_in\_high}$	Input voltage high level	-	2.3	-	VDD_IO +0.3	V
	$V_{WDA\_in\_hys}$	Input voltage hysteresis	-	300	-	800	mV
	R_{pullup}	Internal pull-up resistor	-	50	-	150	kΩ
	f_{CLK1}	WDA clock CLK1	-	-5%	64	5%	kHz

6.17.1 WDA - Watchdog (algorithmic)

Basic feature

Via MSC bus a WDA "question" must be read from a MSC register. A correct response must be written back via MSC in a well defined timing. If response or timing is not correct, then the WDA error counter EC is increased. If the error counter is increased to values greater than 4, some output functions are shut off. If the error counter reaches values greater than 7 (overflow), then a RST reset may be generated if this is previously configured via MSC.

On the other way round, with a RST event also the WDA output pin goes to low.

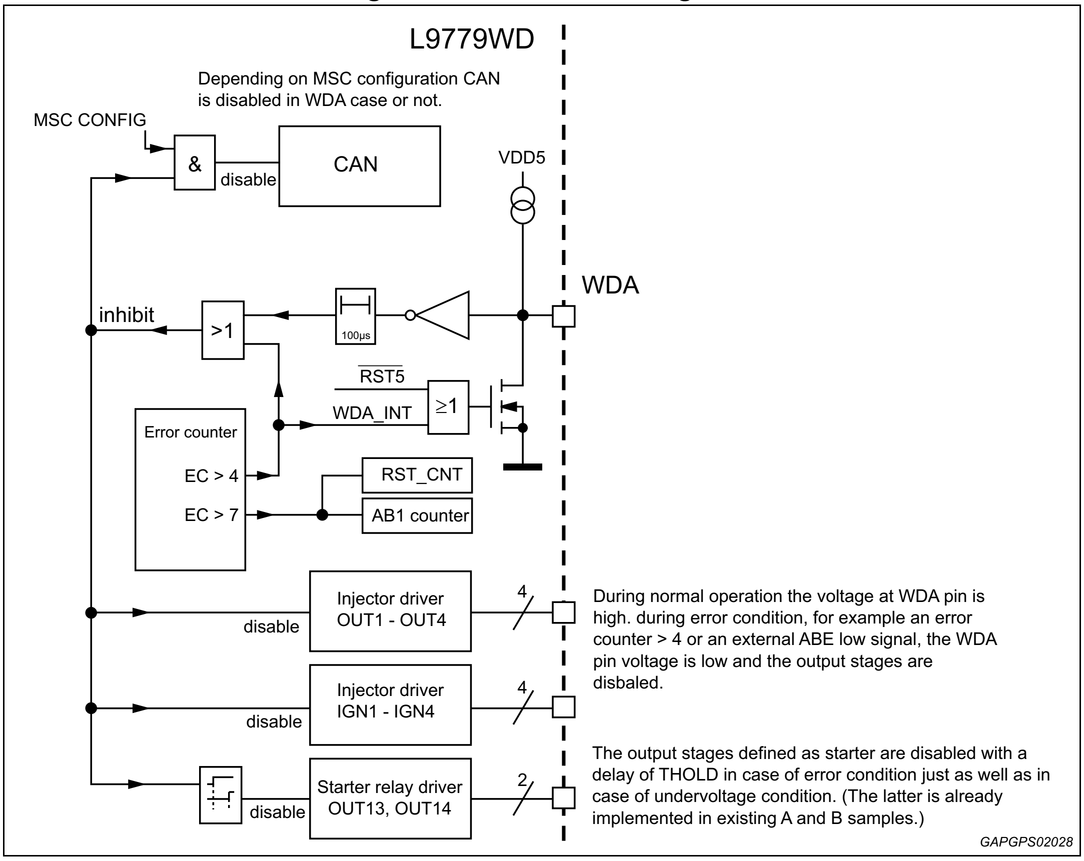
Note that after startup, reset or an overflow the initial value of the error counter is 6.

If WDA resets are enabled via MSC: The number of RST events generated by an error counter overflow is limited by the reset counter RST_CNT. If RST_CNT reaches the value of 7, then RST resets via WDA are no longer generated.

In case many WDA events occur during after-run power latch mode, the power latch mode is terminated by the AB1 counter: With each error counter overflow, the AB1 counter is increased. If it reaches a value greater than 7, then the after-run power latch mode is terminated.

6.17.2 Monitoring module - WDA Functionality

Figure 73. WDA block diagram



Each time the watchdog error counter is EC>7 the AB1-counter AB1_CNT increases. When this counter is AB1_CNT=7 and a further error occurs, the after-run will be terminated. The AB1-counter is not cleared when EC<7. AB1-counter is cleared when EC<5 and <WDA_INT>='0', and is reset by RST_UV.

The monitoring module works independently of the controller functionality. The monitoring module generates various questions, which the controller must fetch and correctly respond to within a defined time window. The monitoring module checks whether the response is returned in a time window and if the response is fully correct.

The question is a 4-bit word. This 4-bit word can be fetched by the controller using a read access to register REQULO. The monitoring module also calculates the expected correct response, which is compared to the actual response from the controller.

The response is a 32-bit word consisting of the 4 bytes RESP_BYTE3, RESP_BYTE2, RESP_BYTE1 and RESP_BYTE0. The 4 bytes are sent to the monitoring module via MSC in the order RESP_BYTE3 - RESP_BYTE2 - RESP_BYTE1 - RESP_BYTE0 using four times the command WR_RESP - once for each answer byte.

Watchdog counters are always counting from power up onwards.

The monitoring cycle phase is initialized by (the end of) writing of RESP_BYTE0 (least significant response byte) or by a write access to the RESPTIME register. The cycle starts with a variable wait time (response time, set by register RESPTIME), followed by a fixed time window. When a monitoring cycle ends (the end of the fixed time window has been reached) a new monitoring cycle is started automatically.

A correct response within the time window (at a response time > 0ms) decreases an ERROR COUNTER by one. An incorrect response, a response outside the time window or response time = 0ms leads to the incrementing of the ERROR COUNTER by one.

"within the time window" means that the end of writing the last answer byte - i.e. RESP_BYTE0 - falls into the fixed time window mentioned above (see picture below). Except the last answer byte, the previous answer bytes may also be written earlier than the beginning of the time window.

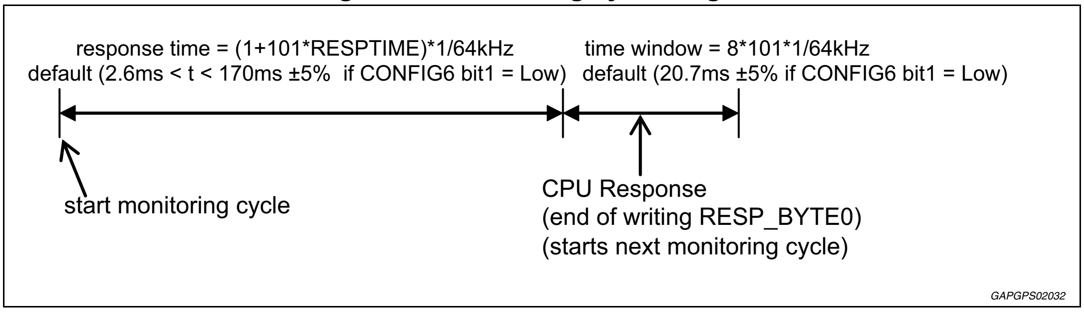
The question sequence is deterministic. A question will be repeated until it is answered correctly both in value and in time. Then the next question is placed in the sequence.

The ERROR COUNTER (EC) is a 3-bit counter. Various actions are activated depending on the value of the counter.

The result of the comparison of the controller response and the calculated correct response, as well as the next question, are available in the registers REQUHI/REQULO after receiving the µC response (LSB of RESP_BYTE0) and can be read by the controller.

Monitoring cycle

Figure 74. Monitoring cycle diagram



Generating questions

The generation of the 4-bit question (REQU [3-0]) is realized with a 4-bit counter and a 4-bit Markov chain. The 4-bit counter only changes into the next state during the sequencer-run when the previous question has been answered correctly in value and in time.

The Markov chain changes into the next state on the 1111b -> 0000b transition of the 4-bit counter if the previous question has been answered correctly in value and in time.

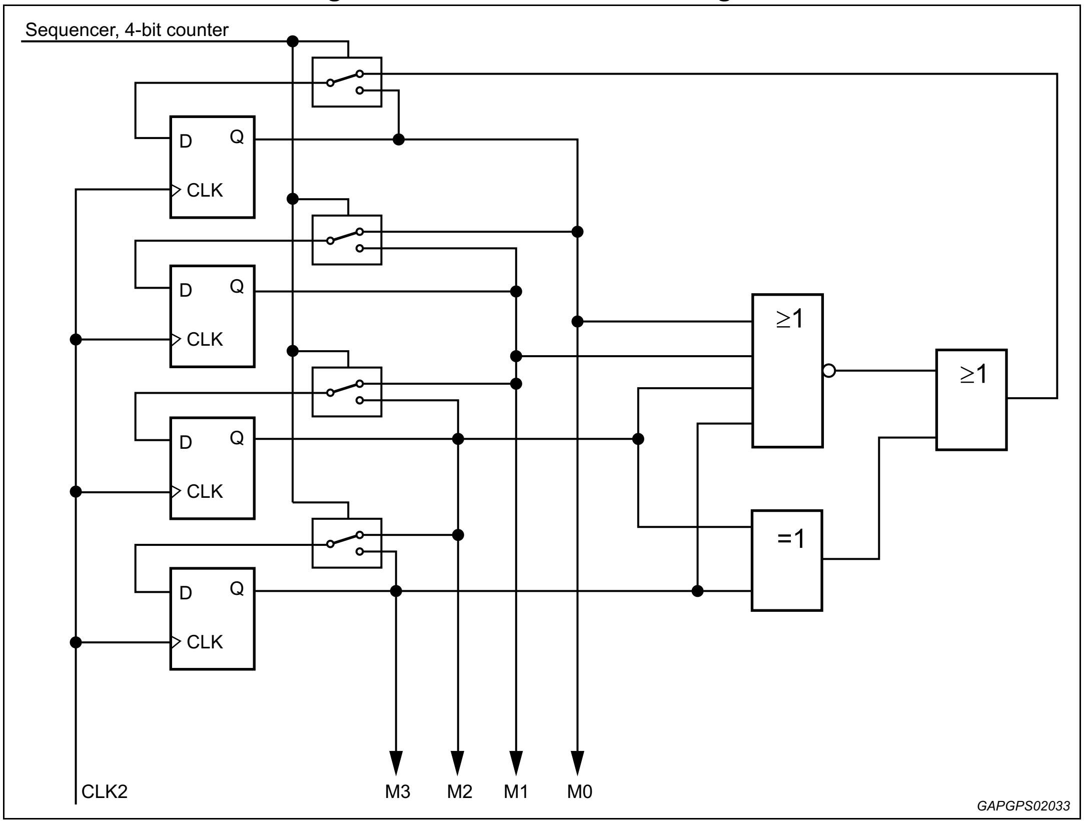
Neither the counter state nor the Markov chain states are changed by a sequencer-run because of a write-access to the RESPTIME register or the expiration of the time window.

The 4-bit counter and Markov chain are set to 0000b when RST_UV is active.

The singularity of the Markov chain is 0000b. To leave the singularity (after power-up, error state), the feedback path (M3 + M2 + M1 + M0) is realized. The "real" feedback logic of the Markov chain is the XOR gate (M3 XOR M2).

The following diagram shows the 4-bit Markov chain.

Figure 75. 4-bit Markov chain diagram



Combining the 4-bit counter and Markov chain to the 4-bit question:

- REQU0 = M1 XOR Z1
- REQU1 = M3 XOR Z3
- REQU2 = M0 XOR Z0
- REQU3 = M2 XOR Z2.

ERROR COUNTER (EC) and reactions, AB1 COUNTER (AB1_CNT) and generation of the monitoring module reset

Various actions are initiated for specific counter states of the ERROR COUNTER EC. The counter reset state is 6.

For ERROR COUNTER (EC) > 4, <WDA_INT> is set to '1', thus activating the open-drain output [WDA] that is low-active.

Table 50. Error counter

ERROR COUNTER	0 ... 4	5	6 ... 7	Over flow EC > 7
WDA_INT	low – i.e. ‘0’	high – i.e. ‘1’	high – i.e. ‘1’	high – i.e. ‘1’
[WDA]	inactive – i.e. ‘1’	active – i.e. ‘0’	active – i.e. ‘0’	active – i.e. ‘0’
AB1-COUNTER	0	unchanged	unchanged	incremented by 1
AB1	low – i.e. ‘0’	unchanged	unchanged	AB1_CNT < 7: low AB1_CNT 6 → 7: low AB1_CNT 7 → 7: high

Shutdown in an error state in "power-latch"

If the ERROR COUNTER reaches the value ‘7’ and a further error occurs the AB1 COUNTER AB1_CNT is incremented by one during a sequencer-run.

The state "EC = 7 and a further error occurs" is also called ERROR COUNTER overflow ("EC" > 7).

If ERROR COUNTER > 4 AND a soft-reset is detected then the COUNTER AB1_CNT is also incremented by one. The counter AB1_CNT is a 3 bit counter.

Behaviour of AB1_CNT:

asynchronous reset to "000" with RST_UV

synchronous reset to "000" IF <WDA_INT> = LOW (EC < 5)

IF (AB1_CNT < 7) AND ((sequencer-run AND ‘EC’ > 7) OR soft-reset) THEN
AB1_CNT = AB1_CNT + 1
ELSE unchanged.

The counter cannot be decremented and can be only reset to "000" by an active RST_UV signal (asynchronous) or <WDA_INT> = '0' (synchronous).

The signal AB1 becomes active '1' when AB1_CNT = ‘111’ and a further error is detected when the sequencer runs or when AB1_CNT = ‘111’ and a soft-reset is detected.

In "power-latch", the active AB1 signal causes a shut-down of the main relay and the voltage regulators. This function ensures a secure shutdown of the system in an error state of the µC in "power-latch".

Signal AB1 is set to '0' again only when <WDA_INT> = '0'.

Behaviour of AB1:

- asynchronous reset to "0" with RST_UV
- synchronous reset to "0" IF <WDA_INT> = '0' (EC < 5)
- IF (AB1_CNT = 7) AND ((sequencer-run AND further error) OR soft-reset) THEN AB1 = 1
  ELSE unchanged.

Generation of a monitoring module reset

The monitoring module may cause a reset at the pin [RST] named "monitoring module reset" in conjunction with the internal signal WD_RST. The generation of a monitoring module reset depends on the state of the bit <INIT_WDR>.

<INIT_WDR> = '0' (reset state):

If <INIT_WDR> = '0', the signal <WD_RST> remains always inactive '0' and the monitoring module can never generate a reset. The error counter can only be decremented via correct responses. If <INIT_WDR> = '0' the state of the reset counter <RST_CNT> remains unchanged when an ERROR COUNTER overflow occurs (description of the reset counter <RST_CNT> see below).

<INIT_WDR> = '1':

If <INIT_WDR> = '1', an ERROR COUNTER overflow activates a reset [RST] (signal <WD_RST> becomes active). The signal <WD_RST> becomes active (i.e. '1') due to an ERROR COUNTER overflow when the value of the 3 bit reset counter <RST_CNT(2-0)> is 0..6. If the value of <RST_CNT> = "111" and an ERROR COUNTER overflow occurs <WD_RST> remains inactive (i.e. '0') and no reset is generated.

The "reset counter" <RST_CNT> is incremented by one during a sequencer-run due to an ERROR COUNTER overflow when <INIT_WDR> = '1' and <RST_CNT> is between 0 and 6. If <RST_CNT> = 7 and an ERROR COUNTER overflow occurs, the counter state remains 7. The counter can not be decremented and can only reset to zero by an active RST_UV signal.

The occurrence of a monitoring module reset is indicated via the flag <WDG_RST> = '1'. Reading the flag via MSC clears it automatically.

In effect maximum 7 monitoring module resets can be generated between 2 active RST_UV signal. (see also state table for <INIT_WDR> = '1' below).

The state of the "reset counter" <RST_CNT> can be read via MSC but cannot be changed.

Table 51. State for <INIT_WDR> = 1

RST_CNT old	"EC" > 7 and sequencer-run	RST_CNT new	WD_RST
000 .. 111	no	= RST_CNT old	'0', no monitoring module reset
000 .. 110	yes	= RST_CNT old + 1	'1', thus monitoring module reset
111	yes	= RST_CNT old =111	'0', no monitoring module reset

In a factory test-mode the pin [WDA] is always active '0'; the internal signal <WDA_INT> is not changed by the factory test-modes.

Note: There is no impact on internal power stages from active pin [WDA] in factory test-mode.

Table 52. Reset-behaviour of <WDA_INT>, AB1 and <WD_RST>

Signal	Reset source	Reset state
WDA_INT	RST_UV	‘1‘, i.e. pin WDA is active
AB1	RST_UV	‘0‘, i.e. inactive
WD_RST	RST_UV	‘0‘, i.e. inactive

Response comparison

The 2-bit counter <RESP_CNT (1-0)> counts the received bytes of the 32-bit response and controls the generation of the expected response. Its default value is "11" (corresponds to "waiting for RESP_BYTE3").

The <RESP_ERR> flag is set '1' when a response byte is incorrect. The flag remains '0' if the 32-bit response is correct. The ERROR COUNTER is updated with the flag. The default state of the flag is '0'.

The 2-bit counter <RESP_CNT(1-0)> and the <RESP_ERR> flag are reset to their corresponding default values at a sequencer-run. The reset condition of the counter <RESP_CNT (1-0)> and the <RESP_ERR> flag are the corresponding default states.

Procedure of the sequential response comparison:

<RESP_CNT(1-0)> = "11": switch the expected response for RESP_BYTE3 to the comparator

Write access: RESP_BYTE3

Set <RESP_CNT> to "10", update <RESP_ERR> flag

<RESP_CNT(1-0)> = "10": switch the expected response for RESP_BYTE2 to the comparator

Write access: RESP_BYTE2

set <RESP_CNT> to "01", update <RESP_ERR> flag

<RESP_CNT(1-0)> = "01": switch the expected response for RESP_BYTE1 to the comparator

Write access: RESP_BYTE1

set <RESP_CNT> to "00", update <RESP_ERR> flag

<RESP_CNT(1-0)> = "00": switch the expected response for RESP_BYTE0 to the comparator

Write access: RESP_BYTE0

Start sequencer (SEQU_START signal), set <RESP_CNT> to "11", update <RESP_ERR> flag (update ERROR COUNTER)

Sequencer clears <RESP_ERR> flag to '0

SEQU_START = ¬(RESP_CNT1) AND ¬(RESP_CNT0) AND “response byte write”

Expected Responses:

RESP_SOLL7 = REQU2 XOR RESP_CNT0
RESP_SOLL6 = REQU0 XOR RESP_CNT0
RESP_SOLL5 = REQU3 XOR RESP_CNT0
RESP_SOLL4 = REQU1 XOR RESP_CNT0

RESP_SOLL3 = ((REQU2 XOR REQU0) XOR REQU3) XOR RESP_CNT1
RESP_SOLL2 = ((REQU0 XOR REQU3) XOR REQU1) XOR RESP_CNT1
RESP_SOLL1 = ((REQU2 XOR REQU0) XOR REQU1) XOR RESP_CNT1

RESP_SOLL0 = (RESP_CNT1 XOR REQU3) XOR REQU0

Table 53. Expected responses

question REQU (3-0)	RESP_BYTE3	RESP_BYTE2	RESP_BYTE1	RESP_BYTE0
0	FF	0F	F0	00
1	B0	40	BF	4F
2	E9	19	E6	16
3	A6	56	A9	59
4	75	85	7A	8A
5	3A	CA	35	C5
6	63	93	6C	9C
7	2C	DC	23	D3
8	D2	22	DD	2D
9	9D	6D	92	62
A	C4	34	CB	3B
B	8B	7B	84	74
C	58	A8	57	A7
D	17	E7	18	E8
E	4E	BE	41	B1
F	01	F1	0E	FE

Reset behaviour

All monitoring module registers are reset by RST_UV The following monitoring module components are also reset by RST_PRL:

Table 54. Reset behaviour

Component:	Reset Condition:
ERROR COUNTER	110b
Register for “EC>7”	‚0‘

Table 54. Reset behaviour (continued)

Component:	Reset Condition:
Register RESPTIME	Maximum value: 0011 1111b
timer state	“000...00”

Note: The signal RST_PRL (partial reset) is active when RST_UV or SW_RST (Soft reset) is active (straight by RST pin. It could be filtered by THOLD after the falling edge of the RST and filtered by the crank event).

Access during a sequencer-run

A sequencer-run (which means the same as a monitoring cycle) is initiated by the writing of a response (i.e. all answer bytes <RESP_BYTE3..0>) or a write to <RESPTIME> or by reaching "end of time window". It must not be interrupted by a new access, i.e. the monitoring module completes the action already started:

- A sequencer-run was initiated by a "response write": The sequencer completes its task with the data of the previous access and the new data are ignored.
- A sequencer-run was initiated by a "response-time write": The sequencer uses the response-time of the previous access, the error counter is correspondingly incremented by one and the <CHRT> bit (REQUHI register) is set and the new data are ignored. <CHRT> will be reset by reading and by the next start of a sequencer run (not reset by the sequencer run that is started by a "response-time write"!)
- A sequencer-run was initiated by "end of time window": The sequencer finishes the started run, the error counter is incremented by one and the new data are ignored.

The writing of a response-time during a sequencer-run must not set the <CHRT> bit (REQUHI register). The new response-time value is also not accepted. The writing of a response during a sequencer-run must not set the <W_RESP> bit, the new response is also not accepted.

Clock and time references

The monitoring module must work independently of the micro-controller clock so that it can monitor the timing of the micro-controller. Therefore, a separate oscillator is necessary. This oscillator is integrated in the L9779 and provides a clock CLK1 for the monitoring module. Clocked with CLK1, a divider generates the base time of 101*1/f_clk = 101 * 1/64 kHz = 1.58 ms for the response-time and 8 * 101*1/64kHz =8* 1.58 ms = 12.6 ms for the fixed time window. Accuracy of CLK1 is ±5% (or better).

The response-time is adjustable by the controller in the range 0ms to about 100ms (register RESPTIME). The response-time can be calculated with the equation response-time = (1+101*RESPTIME)*1/f_clk (where f_CLK depends on CONFIG6 bit1 value: if High - default- f_clk = 64 kHz, if Low f_clk = 39 kHz).

The RESPTIME register is set to '0011 1111'b after a reset. The ERROR COUNTER is incremented by one if the controller changes the response-time. If the response-time is set to 0ms, then the ERROR COUNTER is incremented by one even if a correct response is received within the time window. The maximum error reaction time is given by: maximum response-time, response at the end of a time-window and ERROR COUNTER 0 ' 5 * (100 ms + 12.6 ms) = 563 ms.

Note that clock-tolerances have to be taken into account additionally.

Watchdog influence on power up/down management unit

The watchdog AB1 counter is increased every time the watchdog error counter is EC > 7, which means it has an overflow. If the AB1 counter reaches the value of 7 and a further error occurs, the system will be switched off same as it would happen in case of the already existing PWL_EN_TIMEOUTN signal.

Watchdog influence on smart power reset

WDA has influence on the RST pin only if the WDA error counter is EC > 7 and the resulting reset signal "WD_RST" is enabled by MSC configuration bit "INIT_WDR" in WR_RESPTIME command.

Watchdog influence on Lsa functions (*Section 6.9.1*)

For LSa functions OUT1, OUT2, OUT3, OUT4 (not OUT5).

In case of an internal WDA event (e.g. the WDA error counter is EC > 4 which results in the signal WDA_INT being set) or in case of the WDA pin being pulled low externally, the output stages OUT1, OUT2, OUT3, OUT4 go to inactive state.

Watchdog influence on LSd functions OUT13, OUT14 (starter relay drivers) *Section 6.9.4*

In case of an internal WDA event (e.g. the WDA error counter is EC > 4 which results in the signal WDA_INT being set) or in case of the WDA pin being pulled low externally, the OUT13 and OUT14 stages go to inactive state after the time delay THOLD if the WDA event is still active.

In the case WDA event has switched off OUT13/OUT14 once, Thold becomes 0ms on the next WDA event, unless OUT13/OUT14 are switched off/on or device has been reset.

Moreover, if WDA pin is Low and kept Low at power up, OUT13/OUT14 can be switched on by the external micro, even though WDA EC ≥ 4. That is to allow external micro to control the system especially in the case of WDA pin stuck-low. WDA status pin can be checked by bit 3 of DIA3_REG. See also *Section 6.2.2*.

Watchdog influence on Ignition drivers IGN1, IGN2, IGN3, IGN4

In case of an internal WDA event (e.g. the WDA error counter is EC > 4 which results in the signal WDA_INT being set) or in case of the WDA pin is pulled low externally, the output stages go to inactive state.

Watchdog influence on CAN transceiver

The WDA has influence on the CAN if the MSC configuration bit CAN_TDI is set.

Once the CAN_TDI bit is set, in case of an internal WDA event (e.g. the WDA error counter is EC > 4 which results in the signal WDA_INT being set) or in case of the WDA pin is pulled low externally, the CAN goes to receive-only mode (Rx Only).

6.17.3 Watchdog related MSC commands

RD_DATA8 (read WDA registers)

Table 55. RD_DATA8

Data frame	CSB	C(5..0)	CD(7..0)
RD_DATA8	1	101110	X X X X X X X X

CSB: command selection bit - always '1'

C(5...0): command bits

CD(7...0): command data bits

Reads data block 8 consists of the registers WDA_RESPTIME, REQULO, REQUHI, RST_AB1_CNT. The command has no relevant data as command data bits - they may be set to '1' or '0'.

WR_RESP

Table 56. WR_RESP

Data frame	CSB	C(5..0)	CD(7..0)
WR_RESP	1	100100	RESP(7...0)

CSB: command selection bit - always '1'

C(5...0): command bits

CD(7...0): command data bits

Writes RESP(7...0) - the answer of the µC to the monitoring module question of the U-Chip - to the U-Chip-internal logic of the monitoring module.

WR_RESPTIME

Table 57. WR_RESPTIME

Data frame	CSB	C(5..0)	CD(7..0)
WR_RESPTIME	1	110000	INIT_WDR, CAN_TDI, RESPTIME(5...0),

CSB: command selection bit - always '1'

C(5...0): command bits

CD(7...0): command data bits

Writes RESPTIME(5...0) to the register RESPTIME of the monitoring module. The command has CD(5...0) = RESPTIME(5...0) as command data bits; the command data bits CD7 and CD6 configure INIT_WDR (enable WDA reset) and CAN_TDI (disable CAN in case of WDA event).

6.17.4 Watchdog related MSC registers

MSC registers REQULO, REQUHI, RST_AB1_CNT, RESPTIME are defined as here below:

WDA is configured via MSC by writing MSC_RESPTIME register (WR_RESPTIME command), which is read by RD_DATA7 in upstream.

WDA_RESPTIME is a read_only register, which is written by MSC_RESPTIME, that is to allow proper internal re-synchronization. MSC_RESPTIME bits 5 down through to 0 are automatically replicated into WDA_RESPTIME bit 5 down through to 0 respectively with less than 200 ns latency. This register is read by RD_DATA8 in upstream.

MSC_RESPTIME (upstream data block 7, read command: RD_DATA7)

MSC_RESPTIME **MSC RESPONSE TIME**

7	6	5	4	3	2	1	0
INIT_WDR	CAN_TDI	RESPTIME5	RESPTIME4	RESPTIME3	RESPTIME2	RESPTIME1	RESPTIME0
RW							

Address: -

Type: RW

Reset: 0000 0000b (reset source: Bit 7-0: RST, RST_PRL)

[7] INIT_WDR:
,1': monitoring module reset enabled
,0': monitoring module reset disabled
locked by command LOCK

[6] CAN_TDI: '1': disable transmission if WDA_INT active
locked by command LOCK

[5-0] RESPTIME (5-0): Response-time = (1+ 101*RESPTIME(5-0)) * 1/f_clk with f_clk = 64 kHz if CONFIG6 bit 1 is High, else f_clk=39kHz
The error counter is incremented by one on a controller write access to this register!
not locked by command LOCK

<RESPTIME(5..0)> may be written by the command WR_RESPTIME

WDA_RESPTIME (upstream data block 8, read command: RD_DATA8)

WDA_RESPTIME WDA RESPONSE TIME

7	6	5	4	3	2	1	0
0	0	RESPTIME5	RESPTIME4	RESPTIME3	RESPTIME2	RESPTIME1	RESPTIME0
R							

Address: -

Type: R

Reset: 0011 1111 (reset source RST_PRL)

Reset:

[7] 0

[6] 0

[5-0] effective WDA RESPTIME (after first WR_RESPTIME command till reset WDA_RESPTIME[5:0]==MSC_RESPTIME[5:0])

REQULO (upstream data block 8, read command: RD_DATA8)

REQULO REQUEST LO

7	6	5	4	3	2	1	0
WDA_INT	ERR_CNT2	ERR_CNT1	ERR_CNT0	REQU3	REQU2	REQU1	REQU0
R							

Address: -

Type: R

Reset: 1110 0000b (reset source: Bit 6-4: RST_UV, RST_PRL; Bit 7, 3-0: RST_UV)

[7] WDA_INT: '1': ERROR COUNTER > 4

[6-4] ERR_CNT (2-0): value of the ERROR COUNTER

[3-0] REQU (3-0): 4-bit question

REQUHI (upstream data block8, read command: RD_DATA8)

REQUHI REQUEST HI

7	6	5	4	3	2	1	0
RESP_CNT1	RESP_CNT0	RESP_ERR	RESP_Z0	CHRT	W_RESP	NO_RESP	RESP_TO_EARLY
R							

Address: -

Type: R

Reset: 1100 0000b (reset source: RST_UV, Bit 4 additionally RST_PRL)

[7-6] RESP_CNT(1-0):
Counter for receiving the 4 response bytes

[5] RESP_ERR:
'1': 1 byte of the 32-bit response is incorrect (1)

[4] RESP_Z0:
'1': Controller set response-time to 0ms; a correct response within the time window nevertheless increments the error counter by one '0': Response-time is greater than 0ms

[3] CHRT:
'1': Controller has changed response-time; reset to zero after a read access and after the next sequencer run

[2] W_RESP:
'1': in case of incorrect response in value; reset to zero at sequencer-run (1)

[1] NO_RESP:
'1': in case of no response at all; timer is restarted automatically; reset to zero after a read access

[0] RESP_TO_EARLY:
'1': Response before time window was opened; reset to zero at sequencer-run (1)

1. Sequencer-run: A sequencer-run is initiated by the writing of a complete response (RESP_BYTE3…RESP_BYTE0) or by writing of a response-time <RESPTIME> or by reaching the end of a time window. In case WDA reference time base (1/f_clk) has to be changed to f_clk = 39 kHz, CONFIG6 bit1 has to be written to 0 before sequencer-run is started.

RESP_TO_EARLY = '1':

monitoring module has received a response before beginning of the time window and therefore this was rejected. Reception of a response means "end of reception of RESP_BYTE0" after the other response bytes (i.e. RESP_BYTE3, RESP_BYTE2, RESP_BYTE1 - in this order!) have been received.

NO_RESP = '1':

monitoring module has received no response at all or a response too late after the time window already closed. However, a response too late might be read as RESP_TO_EARLY, as too late a response is at the same time too early a response concerning the next WDG cycle. This results in the NO_RESP monitoring being overwritten by a RESP_TO_EARLY monitoring.

This means that no "end of reception of RESP_BYTE0" was detected before the end of the time window - neither during the time window nor before beginning of the time window. (Remember: RESP_BYTE0 is the last of four response bytes!)

W_RESP = '1':

an error occurred during the sequencer run before.

RESP_ERR = '1':

an error occurred during the actual sequencer run. The bit will be set to '1' after receiving any incorrect answer byte and will remain '1' until the end of the actual sequencer run (no matter if the other answer bytes in this sequencer run are correct or not).

At the end of a sequencer run the error bit W_RESP will be set to the actual value of RESP_ERR, and thereafter the error bit RESP_ERR will be cleared to '0'.
RESP_CNT = '11': waiting for RESP_BYTE3
RESP_CNT = '10': waiting for RESP_BYTE2 (after RESP_BYTE3 was received)
RESP_CNT = '01': waiting for RESP_BYTE1 (after RESP_BYTE2 was received)
RESP_CNT = '00': waiting for RESP_BYTE0 (after RESP_BYTE1 was received)

RST_AB1_CNT (upstream data block 8, read command: RD_DATA8)

RST_AB1_CNT AB1 COUNTER

7	6	5	4	3	2	1	0
0	0	AB1_CNT2	AB1_CNT1	AB1_CNT0	RST_CNT2	RST_CNT1	RST_CNT0
R							

Address: -

Type: R

Reset: xx00 0000b (reset source: Bit 6…0: only RST_UV; RST_PRL has no effect)

[7] 0

[6] 0

[5-3] REQU (3-0): AB1_CNT (2-0)

[2-0] RST_CNT (2-0) reset counter RST_CNT

6.17.5 MicroSecond Channel activity watchdog

MSC data frames are monitored to be sent in intervals shorter than tMSC_mon. If L9779WD receives no valid data frame for longer than tMSC_mon, it will switch off all the drivers and the error flag (TRANS_F) and OUT_DIS will be set.

The MRD and OUT13, 14, 21 and 25 (if low battery function is enabled) are not disabled by missing activity on MSC.

No reset request is sent to the smart reset function module.

To enable the outputs again, the µC has to read the TRANS_F and then send the command START, and then outputs are reactivated with the first correct data frame. If the fault flag is not cleared the START command is ignored.

By default the MicroSecond Channel activity watch dog is enabled and the monitoring time will start after writing of the OUT_DIS bit by START command. Each time the L9779WD receives a valid data frame the tMSC_on timer is reset. This means that micro controller can drive the outputs only when the monitoring module is active.

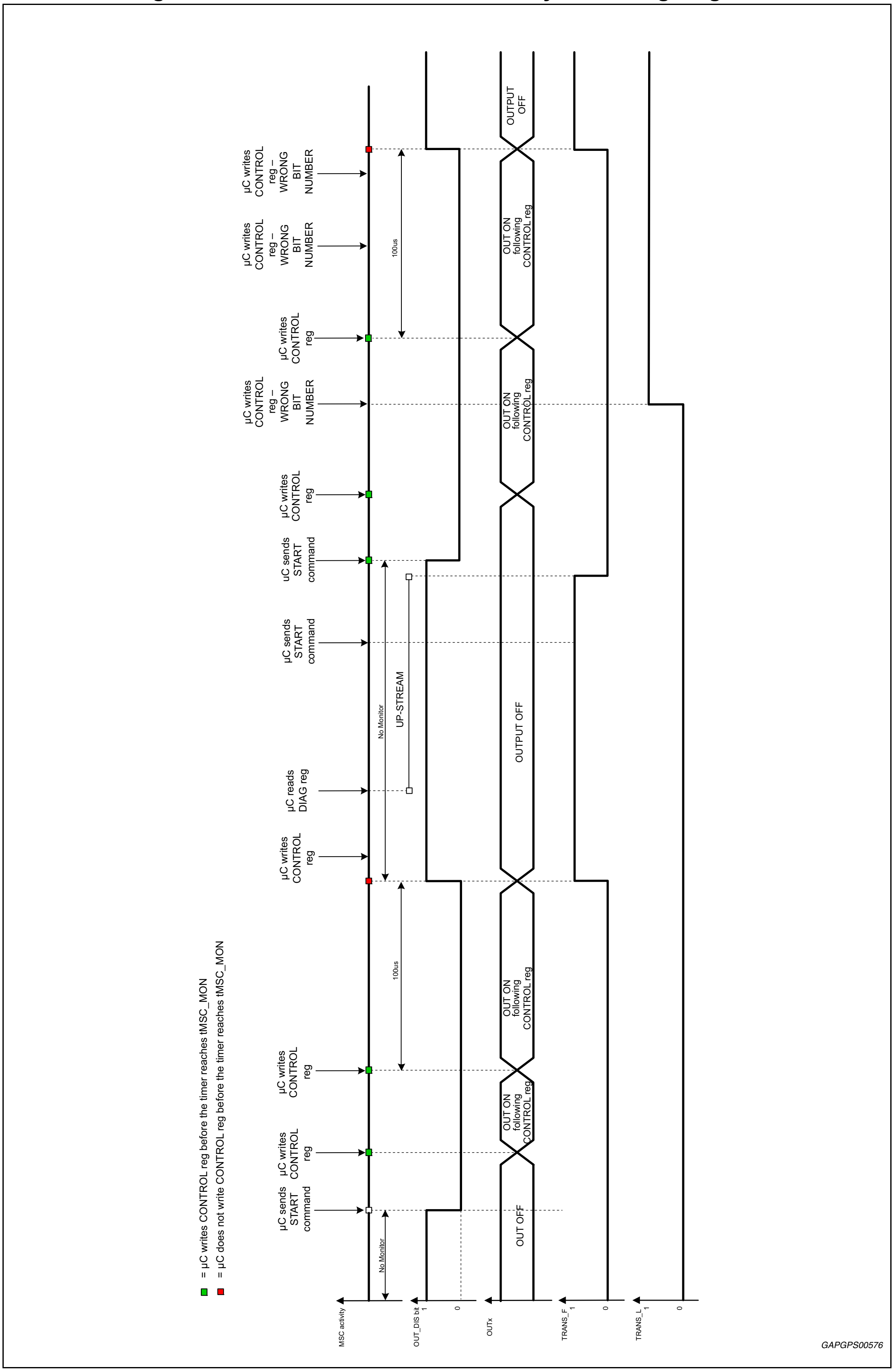
To disable the MicroSecond Channel activity watch dog the µC have to set to 0 the bit MSC_ACT_EN.

If the MSC frame has a wrong number of bit the flag TRANS_L is set but no action on outputs is taken. The frame with wrong length is ignored.

Table 58. MicroSecond Channel activity watchdog

<table>
<tr><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>tMSC_mon</td><td>100</td><td>142</td><td>185</td><td>µs</td></tr>
<tr><td rowspan="4">$t1_{WD}$</td><td>-30%</td><td>0.9*t2WD</td><td>+30%</td><td>ms</td></tr>
<tr><td>-30%</td><td>0.8*t2WD</td><td>+30%</td><td rowspan="3">-</td></tr>
<tr><td>-30%</td><td>0.7*t2WD</td><td>+30%</td></tr>
<tr><td>-</td><td>0</td><td>-</td></tr>
<tr><td rowspan="4">$t2_{WD}$</td><td>14</td><td>20</td><td>26</td><td rowspan="4">ms</td></tr>
<tr><td>35</td><td>50</td><td>65</td></tr>
<tr><td>59</td><td>70</td><td>91</td></tr>
<tr><td>70</td><td>100</td><td>130</td></tr>
</table>

Figure 76. MicroSecond Channel activity watch dog diagram



6.18 Serial interface

The L9779WD offers the possibility to communicate with a µC using the MicroSecond Channel (MSC).

The serial communication is used:

- to set the parameter
- to read diagnosis
- to activate, to deactivate and to use the low side drivers
- to activate test mode (ST reserved).

6.18.1 MSC interface

Communication with the microcontroller is done via MSC i.e.MicroSecond Channel; equivalent to µsec-bus 2^{nd} generation.

Downstream communication is data or command sent by µC and received by L9779WD.

Upstream communication is data sent by the L9779WD and received by µC.

The MicroSecond Channel (MSC) interface provides a serial communication link typically used to connect peripheral devices with a micro controller. The serial communication link is built up by a fast synchronous downstream channel (with differential inputs and differential clock) and a slow synchronous upstream channel.

Differential inputs for downstream data are pins [DIP] and [DIN]; the differential input signal [DIP]-[DIN] is referred to as DI. The clock pins are [CLP] and [CLN], the differential clock [CLP]-[CLN] is referred to as CL. There is an internal resistor between pins [DIP] and [DIN] - and between [CLP] and [CLN].

There is one input for chip select at pin [EN], and one output for upstream data at pin [DO]. L9779WD always is the slave in this communication link. These pins are single-ended.

Multiple power devices with MSC on downstream are possible. Downstream device is selected by EN.

MSC uses normal polarity for DI, CLK, and DO: a logic '1' is a 'high level' and a logic '0' is a 'low level'.

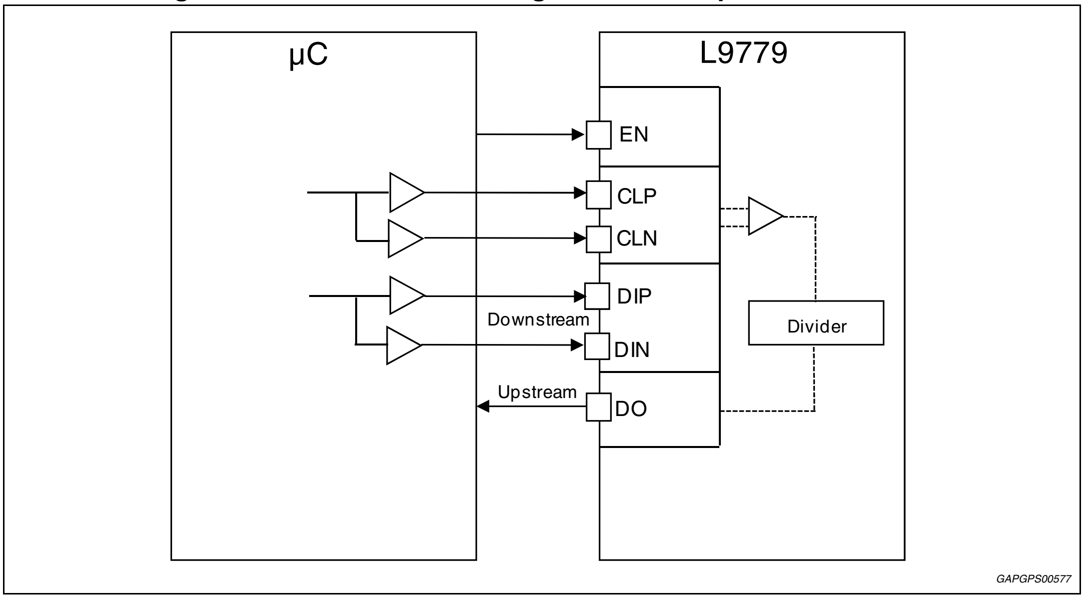
MSC uses inverted polarity for EN: a logic '1' is a 'low level' and a logic '0' is a 'high level'.

By this way it is possible to drive multiple power devices with shared CL and DI lines and individual EN signal.

The maximum downstream clock rate is CL = 40MHz. Upstream is done with a lower clock rate f_{SDO}, selectable by the microcontroller; after a reset the upstream clock rate is f_{SDO} = CL/64.

The upstream clock is synchronous with CL since it is derived from a clock divider. Therefore the CL signal must always be running independently whether a downstream transmission is running or not.

Figure 77. Communication diagram between µC and L9779WD



Downstream communication

Signals

The enable input is active with inverted polarity - i.e., low level during the active phases of command or data frames. An active enable signal validates the DI input signal. Outside the active phase (enable line is at high level) invalid data may occur at DI.

The active phase of a downstream frame starts with the falling edge of the enable signal and ends with the rising edge of the enable signal. The enable signal changes its state with the rising edge of the clock CL (because CL has normal polarity).

DI changes its state on rising edge and it is latched by L9779WD on the falling edge of CL.

Downstream frames are synchronous serial frames. They support enable signal and command/data selection bit as part of the frame. Command/data selection bit allows distinguishing frames as command and data frames in the receiver circuit.

Command frames and data frames may be sent in any sequence with a passive phase of at least 2 CL-cycles after each frame.

Command frame

A command frame always starts with a high level bit (command selection bit). The number of the command bit of the active phase of a command frame NCB is fixed to 14. If the number of the command bit is not equal to NCB = 14 the frame will be ignored, the command will not be executed and the error flag (TRANS_L) will be set.

The length of the command frame's passive phase tCPP must be a minimum of 2 * tCL.

Execution of the command is finished not later than 16*tCL after the end of active phase.

Figure 78. Command frame diagram

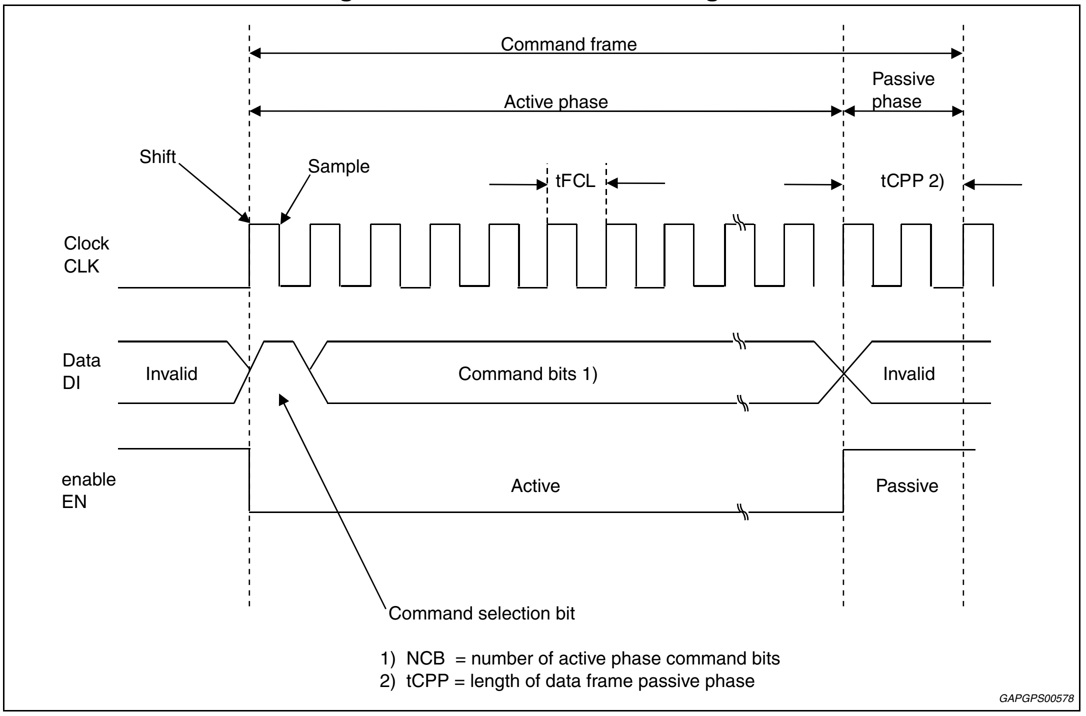


Table 59. Content of a command frame (transmitted LSB first)

Bit	Description
0	='1': command selection bit
1-6	Command LSB first!
7-14	Data for the command LSB first!

Data frame

A data frame always starts with a low level bit (data selection bit). The number of the data bit of the active phase of a data frame NDB is fixed to 30. If the number of the data bit is not equal to NDB = 30 the frame will be ignored and the error flag (TRANS_L) will be set.

The length of the data frame's passive phase tDPP must be a minimum of 2 * tCL.

Execution of the data frame is finished not later than 16*tCL after the end of active phase.

Figure 79. Data frame diagram

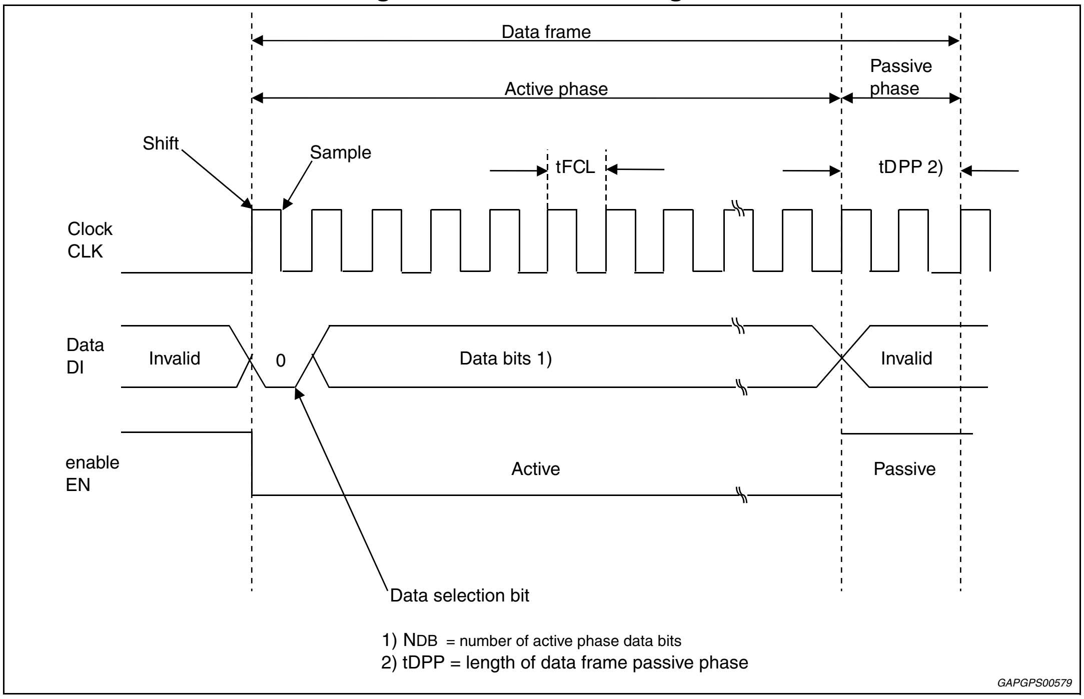


Table 60. Content of a data frame (transmitted LSB first)

Bit	Description
Data selection bit	0
0-7	CONTR_REG1(LSB…MSB)
8-15	CONTR_REG2(LSB…MSB)
16-23	CONTR_REG3(LSB…MSB)
24-29	CONTR_REG4(LSB…MSB)

Upstream communication

The serial data output [DO] is the synchronous serial data signal of the upstream channel.

The polarity for [DO] is ‚normal polarity'- i.e. a low level bit at [DO] is stored in the µC as a logic ‚0', and a high level bit at [DO] is stored in the µC as a logic ‚1'.

The serial data output is single-ended.

The frequency is derived from CL by an internal divider to typ. fSDO = CL/64. It can be adjusted via MSC to fSDO = CL/16... CL/128. The time for a bit is TSDO = fSDO.

Each upstream frame consists of 16 bit:

- 1 start bit, always '0'
- 4-bit-upstream address field (A[0..3] with LSB first)
- 8 bit data upstream data field (D[0..7] with LSB first)
- 1 upstream parity bit (with odd parity for the complete data frame)
- 2 fSDO stop bit, always '1'.

Note: External pull-up resistor on SDO pin is required. Its value depends on MSC SDO bit rate.

The commands that perform a read access to the L9779WD-data always initiate 4 registers to be sent by the L9779 to the µC.

Within the execution of these read commands an upstream data frame is sent after the 2 stop bits of the prior upstream data frame and one additional inter-frame bit waiting time.

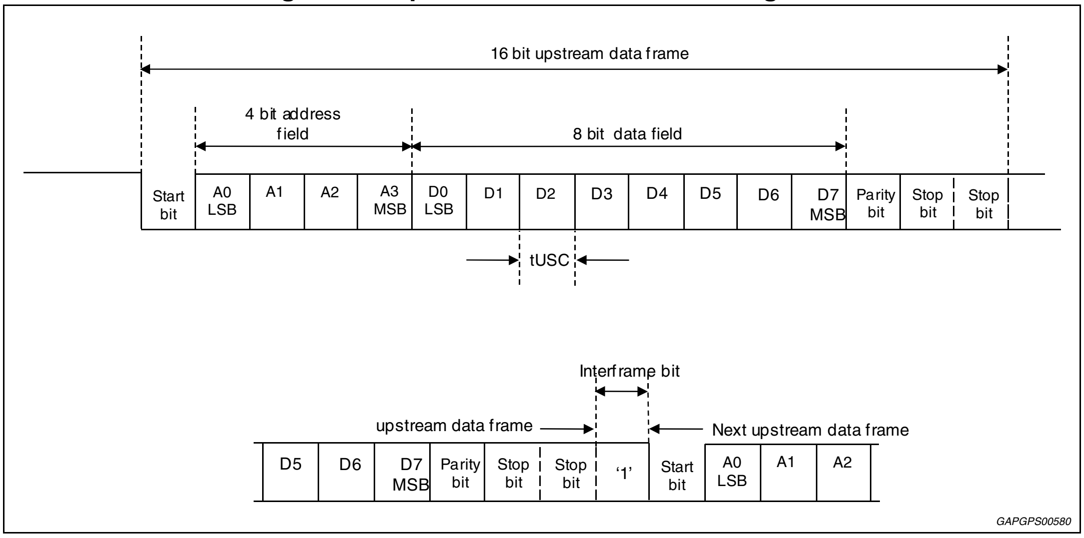
If a new read command is received while the 4 registers up-stream communication is active, the 16 bit up-stream on-going is completed and after the inter-frame bit it is sent the new 4 register up-stream sequence requested.

With the beginning of the upstream frame the latched flags contained in the register are cleared automatically.

The time from the read command to the first upstream frame of the answer is less than 100µs.

The end of the upstream frame is after 17 x 4 tUSC. Outside the upstream frame the DO output is high impedance.

Figure 80. Upstream communication diagram



Timing characteristics

Figure 81. Timing diagram

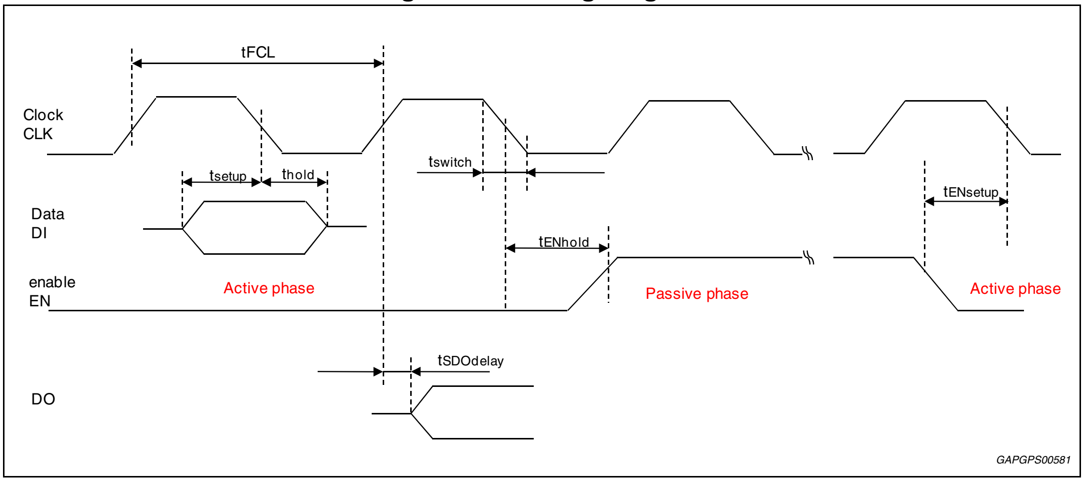


Table 61. Timing characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CL}	Cycle time	25	-	-	ns
t_{setup}	Data setup time	5	-	-	ns
t_{hold}	Data hold time	5	-	-	ns
t_{switch}	Switching time Switching time for CL, EN and SI measured between 0.1*VVDD3 and 0.9*VVDD3	-	-	3	ns
t_{CLlow}	CL low time	10	-	-	ns
t_{CLhigh}	CL high time	10	-	-	ns
$t_{ENsetup}$ (1)	EN setup time (i.e. time between falling edge of EN and next falling edge of CL)	5	-	-	ns
t_{ENhold} (1)	EN hold time (i.e. time between falling edge of CL and next rising edge of EN)	5	-	-	ns
t_{SDO} /t_{CL}	data out cycle time CL_CONF1='1',CL_CONF0='1' CL_CONF1='1',CL_CONF0='0' CL_CONF1='0',CL_CONF0='1' CL_CONF1='0',CL_CONF0='0'	-25%	128 64 32 16	+25%	-
f_{CL}	Clock range at CL L9779WD is fully functional incl. all timings as long as there is a clock at pins CLP, CLN: CL	-	-	40	MHz
-	tSDOdelay	-	-	160	ns

1. Enable setup time and enable hold time are validated with characterization.

Figure 82. Time circuit

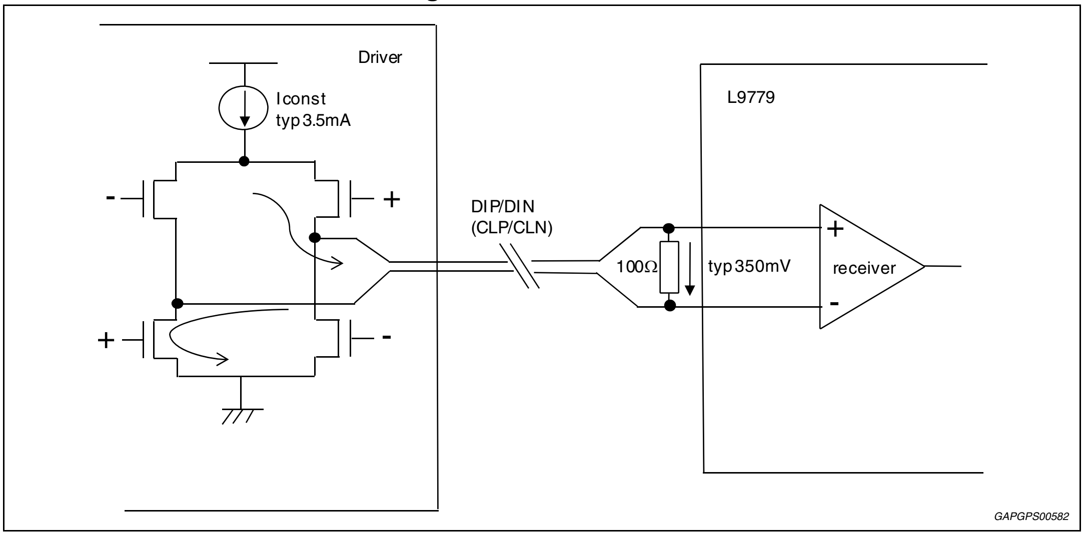


Figure 83. Cycle time diagram

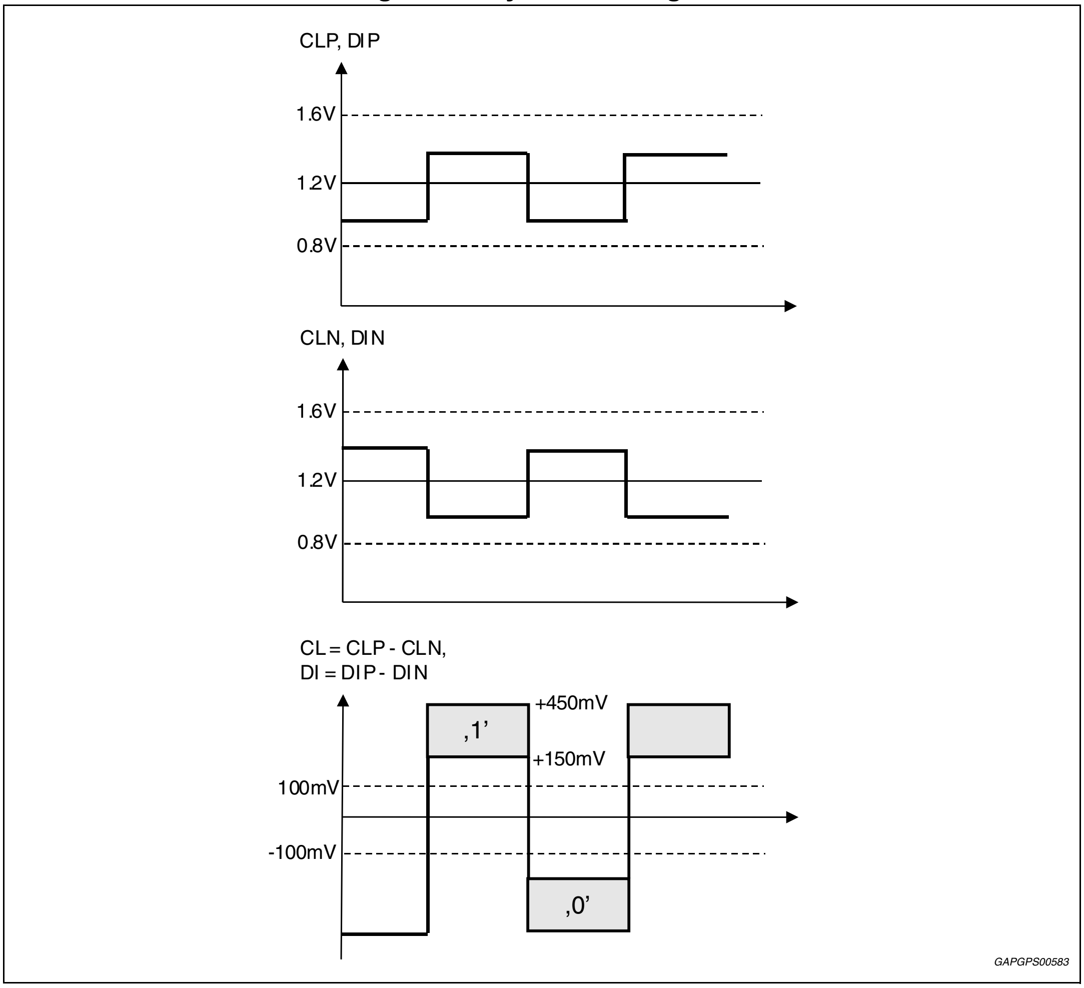


Table 62. Time electrical characteristics

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
CLP, CLN	VCLP, VCLN	Input voltage range	Not to be tested. It is an application note.	0.8	-	1.6	V
	VCLdiff	Differential input voltage VCLdiff =|VCLP-VCLN|		150	-	450	mV
	VCLdiff	Input voltage offset VCLdiff =0.5*(VCLP+VCLN)		1	-	1.4	V
	Rcl	EXTERNAL Resistor between CLP and CLN		-	100	-	Ω
	Rpu_N	Internal pull-up resistor	-	100	200	400	kΩ
	Rpd_P	Internal pull-down resistor	-	100	200	400	kΩ
	VCL_high	Differential input high detection level VCL_high= VCLP_high - VCLN_high	-			100	mV

Table 62. Time electrical characteristics (continued)

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
CLP, CLN	VCL_low	Differential input low detection level VCL_low= VCLP_low- VCLN_low	-	-100	-	-	mV
DIP, DIN	VDIP, VDIN	Input voltage range	Not to be tested. It is an application note.	0.8	-	1.6	V
	VDIdiff	Differential input voltage VDIdiff =|VDIP-VDIN|		150	-	450	mV
	VDIdiff	Input voltage offset VDIdiff =0.5*(VCLP+VCLN)		1	-	1.4	V
	R_{cl}	Resistor between DIP and DIN		-	100	-	Ω
	R_{pu_N}	Internal pull-up resistor	-	100	200	400	kΩ
	R_{pd_P}	Internal pull-down resistor	-	100	200	400	kΩ
	VDI_high	Differential input high detection level VDI_high= VDIP_high- VDIN_high	-	-	-	100	mV
	VDI_low	Differential input low detection level VDI_low= VDIP_low- VDIN_low	-	-100	-	-	mV
DO	VDO_L	DO output low level	VDD_IO = 5 V or 3.3 V Isink current = 2 mA	-	-	0.5	V
	VDO_H	DO output high level	VSUP = 5 V or 3.3 V Isource current=2mA	VDD_IO -0.5	-	-	V
	f_{DO}	Maximum frequency	Tested by SCAN	fCL/ 128	fCL/ 64	fCL/ 16	MHz
EN	EN_L	Low input level	-	-0.3	-	1.1	V
	EN_H	High input level	-	2.3	-	VDD 5+0.3	V
	V_{HYST}	Hysteresis	-	0.1	-	-	V
	I_{IN}	Input current	-	-	-	5	µA
	R_{PU}	Pull-up resistor	-	50	-	250	kΩ

6.18.2 Commands

MSC-commands are encoded with 6 bits with a Hamming distance at least of 2.

Table 63. Commands

#	Command	Command bit MSB ... LSB	Description
1	RD_DATA1	000011	Read CONFIG_REG1…4 (Upstream Block 1)
2	RD_DATA2	000101	Read CONFIG_REG5, 6, 7 (Upstream Block 2)
3	RD_DATA3	000110	Read DIA_REG1...4 (Upstream Block 3)
4	RD_DATA4	001001	Read DIA_REG5...8 (Upstream Block 4)
5	RD_DATA5	001010	Read DIA_REG9…11, IDENT_REG (Upstream Block 5)
6	RD_DATA6	001100	Read WDA_QUERY, 00h, STEP_CNT (Upstream Block 6)
7	WR_CONFIG1	001111	Write CONFIG_REG1
8	WR_CONFIG2	010001	Write CONFIG_REG2
9	WR_CONFIG3	010010	Write CONFIG_REG3
10	WR_CONFIG4	010100	Write CONFIG_REG4
11	WR_CONFIG5	010111	Write CONFIG_REG5
12	WR_CONFIG6	011000	Write CONFIG_REG6
13	WR_CONFIG7	011011	Write CONFIG_REG7
14	LOCK	011101	Disable writing of all configuration bit
15	UNLOCK	011110	Enable writing of all configuration bit
16	SW_RST	100001	Software reset
17	START	100010	Enable power stages
18	RD_SINGLE	101000	Read one byte at a time on each access (see addresses table)
19	STOP	101011	Disable power stage
20	RD_DATA7	101101	Read DIA_REG12, DIA_REG12, RESP, MSC_RESPTIME (Upstream block 7)
21	RD_DATA8	101110	Read WDA_RESPTIME, REQULO, REQUHI, RST_AB1_CNT
22	WR_RESP	100100	Write RESP register
23	WR_RESPTIME	110000	Write RESPTIME register
24	WR_CPS	110011	Write CPS parallel configuration (if CPS mode enabled)
25	MRD_REACT	100111	Main relay reactivation after OVC switch off

Note: Pay attention to the fact that the LSB is always transmitted first.

RD_DATA1, 2, 3, 4, 5, 6, 7 and 8

Table 64. RD_DATA1, 2, 3, 4, 5, 6, 7 and 8

Command	CSB	C(5..0)	CD(7..0)
RD_DATA1	1	0 0 0 0 1 1	X X X X X X X X
RD_DATA2	1	0 0 0 1 0 1	X X X X X X X X
RD_DATA3	1	0 0 0 1 1 0	X X X X X X X X
RD_DATA4	1	0 0 1 0 0 1	X X X X X X X X
RD_DATA5	1	0 0 1 0 1 0	X X X X X X X X
RD_DATA6	1	0 0 1 1 0 0	X X X X X X X X
RD_DATA7	1	1 0 1 1 0 1	X X X X X X X X
RD_DATA8	1	1 0 1 1 1 0	X X X X X X X X

CSB : command selection bit - always '1'

C(5...0) : command bit

CD(7...0): command data bit

READ_DATA1 initiates 4 upstream communications that transfer data block 1 that consists of the registers CONFIG_REG1, CONFIG_REG2, CONFIG_REG3 and CONFIG_REG4, transmitted exactly in this order.

READ_DATA2 initiates 4 upstream communications that transfer data block 2 that consists of the registers CONFIG_REG5, CONFIG_REG6, CONFIG_REG7, not used, transmitted exactly in this order.

READ_DATA3 initiates 4 upstream communications that transfer data block 3 that consists of the registers DIA_REG1, DIA_REG2, DIA_REG3 and DIA_REG4, transmitted exactly in this order.

READ_DATA4 initiates 4 upstream communications that transfer data block 4 that consists of the registers DIA_REG5, DIA_REG6, DIA_REG7 and DIA_REG8, transmitted exactly in this order.

READ_DATA5 initiates 4 upstream communications that transfer data block 5 that consists of the registers DIA_REG9, DIA_REG10, DIA_REG11 and IDENT_REG, transmitted exactly in this order.

READ_DATA6 initiates 4 upstream communications that transfer data block 6 that consists of the registers WDA_QUERY, not used, STEP_CTN_H and STEP_CTN_L.

READ_DATA7 initiates 4 upstream communications that transfer data block 7 that consists of the registers DIA_REG12, DIA_REG12, RESP, and WDA_RESPTIME.

READ_DAT8 initiates 4 upstream communications that transfer data block 7 that consists of the registers WDA_RESPTIME, REQULO, REQUHI, RST_AB1_CNT.

The command has no relevant data as command data bit - they may be set to '1' or '0'.

If a new read command is received while the current 4 up-stream communication is active, the 16 bit up-stream on-going is completed and after the inter-frame bit it is sent the new 4 register up-stream sequence requested.

WR_CONFIG1, 2, 3, 4, 5, 6, 7, WR_RESP, WR_RESPTIME

Table 65. WR_CONFIG1, 2, 3, 4, 5, 6, 7, WR_RESP, WR_RESPTIME

Command	CSB	C(5..0)	CD(7..0)
WR_CONFIG1	1	0 0 1 1 1 1	CONFIG1(7:0)
WR_CONFIG2	1	0 1 0 0 0 1	CONFIG2(7:0)
WR_CONFIG3	1	0 1 0 0 1 0	CONFIG3(7:0)
WR_CONFIG4	1	0 1 0 1 0 0	CONFIG4(7:0)
WR_CONFIG5	1	0 1 0 1 1 1	CONFIG5(7:0)
WR_CONFIG6	1	0 1 1 0 0 0	CONFIG6(7:0)
WR_CONFIG7	1	0 1 1 0 1 1	CONFIG7(7:0)
WR_RESP	1	1 0 0 1 0 0	RESP
WR_RESPTIME	1	1 1 0 0 0 0	WDA_RESPTIME
WR_CPS	1	1 1 0 0 1 1	CPS

CSB : command selection bit - always '1'

C(5...0) : command bit

CD(7...0): command data bit

Writes the register CONFIG_REG1, 2, 3, 4, 5, 6, 7

Lock, unlock

Table 66. Lock, unlock

Command	CSB	C(5..0)	CD(7..0)
Lock	1	0 1 1 1 0 1	X X X X X X X X
Unlock	1	0 1 1 1 1 0	X X X X X X X X

CSB : command selection bit - always '1'

C(5...0) : command bit

CD(7...0): command data bit

This command disables ("lock") writing of all configuration registers. The commands have no relevant data as command data bit - they may be set to '1' or '0'.

The registers RESP and RESPTIME are not affected by LOCK command (i.e. they cannot be locked)

Default state is configuration registers not locked.

The content of a lockable bit is valid both if the bit is locked or if it is unlocked. Writing data to the bit is possible if the bit is unlocked; the new values become valid during execution of the write command.

SW_RST

Table 67. SW_RST

Command	CSB	C(5..0)	CD(7..0)
SW_RST	1	1 0 0 0 0 1	X X X X X X X X

CSB : command selection bit - always '1'

C(5...0) : command bit

CD(7...0): command data bit

With CD(7..0) = X X X X X X X X

This command generates a L9779WD internal reset initiated by the µC's software ("software reset") that clears all the configuration and diagnostic registers and switches-off all the drivers.

The command has no relevant data as command data bit - they may be set to '1' or '0'.

Start, Stop

Table 68. Start, Stop

Command	CSB	C(5..0)	CD(7..0)
Start	1	1 0 0 0 1 0	X X X X X X X X
Stop	1	1 0 1 0 1 1	X X X X X X X X

CSB : command selection bit - always '1'

C(5...0) : command bit

CD(7...0): command data bit

The command START sets the bit <OUT_DIS> to '0'. With <OUT_DIS> = '0' the outputs [OUT1...OUT9] [OUT13…OUT28] and [IGN1...IGN4] can be activated using control registers. After a reset (default state) the bit is <OUT_DIS>='1' and the outputs are disabled (so any MSC data frame writing control registers is ignored and the power stages are all switched off).

The command STOP sets the bit <OUT_DIS> to '1' disabling the outputs.

These commands have no relevant data as command data bit - they may be set to '1' or '0'.

MRD_REACT

Table 69. MRD_REACT

Command	CSB	C(5..0)	CD(7..0)
MRD_REACT	1	1 0 0 1 1 1	X X X X X X X X

CSB : command selection bit - always '1'

C(5...0) : command bit

CD(7...0): command data bit

This command allows to the uC to turn on the MRD if it was switched off due to over current.

RD_SINGLE

Table 70. RD_SINGLE

Command	CSB	C(5..0)	CD(7..0)
RD_SINGLE	1	1 0 1 0 0 0	0 0 CD(5..0)

CSB : command selection bit - always '1'

C(5...0) : command bit

CD(7...0): command data bit to select the register to be read. NB: CD(7..6) must be 0.

This command allows to read one register at a time. The register to be read is specified through the command data field and is encoded with a Hamming distance at least of 2 according to the following table:

Table 71. Register through the command data field

#	CD(5:0)	Register	Description
1	000011	R CONFIG_REG1	MRD_OT_DIS, OUT8 short to VB filter time and threshold
2	000101	R CONFIG_REG2	LS_IGN_OFF, OUT9 short to VB filter time and threshold
3	000110	R CONFIG_REG3	VRS edge and feedback position selection
4	001001	R CONFIG_REG4	lock status/slew-rate/upstream clock ratio/off state diagnosis/power latch mode config
5	001010	R CONFIG_REG5	VRS config/MSC monitoring status/OUT21-28 config
6	001100	R CONFIG_REG6	PSOFF/power latch mode enable flag/reset generation flag/can error enable flag
7	001111	R CONFIG_REG7	low battery setting status to OUT 13,14,24,25/TD mask type/IGN diagnosis type
8	111001	R CONFIG_REG8	WDA RESP
9	111010	R CONFIG_REG9	RESPTIME
10	111100	R CONFIG_REG10	CPS CONF
11	010001	R DIA_REG1	diagnosis bit of OUT 1,2,3,4

Table 71. Register through the command data field (continued)

#	CD(5:0)	Register	Description
12	010010	R DIA_REG2	diagnosis bit of OUT 5,6,7,8
13	010100	R DIA_REG3	diagnosis bit of OUT 9,10,13,14
14	010111	R DIA_REG4	diagnosis bit of OUT 15,16,17,18
15	011000	R DIA_REG5	diagnosis bit of OUT 19,20
16	011011	R DIA_REG6	diagnosis bit of OUT 21,22,23,24
17	011101	R DIA_REG7	diagnosis bit of OUT 25,26,27,28
18	011110	R DIA_REG8	diagnosis bit of IGN 1,2,3,4
19	100001	R DIA_REG9	VTRK diag bit/VRS diag bit/MRD status /KEY_ON_STATUS (not filtered)
20	100010	R DIA_REG10	OV_RST/OUT_DIS/V3V3_UV/general diag in OUT 21-28/CRK_RST/ general diag in OUT 1-10,13-20,IGN 1-4/TNL_RST
21	100100	R DIA_REG11	MSC error flag/CAN error flag/VDD reset flag/ over temperature flag
22	100111	ZERO_REG	Returns all zeros
23	101000	R STP_CNT_H	stepper counts high
24	101011	R STP_CNT_L	stepper counts low
25	101110	R IDENT_REG	chip id, revision information
26	101101	R DIA_REG12	Key on status filtered
27	110000	RESPTIME	WDA Response Time
28	110011	REQULO	WDA request low byte
29	110101	REQUHI	WDA request high byte
30	110110	RST_AB1_CNT	WDA AB1 counter

In case of RD_SINGLE command the upstream consists of 16 bits as described in *Figure 80*.

The association between the registers and the "4 bit address field" is the following:

Table 72. Association between the registers and the "4 bit address field

#	Register	Content of "4 bit address field" in the upstream
1	CONFIG_REG1	0000
2	CONFIG_REG2	0100
3	CONFIG_REG3	1000
4	CONFIG_REG4	1100
5	CONFIG_REG5	0000
6	CONFIG_REG6	0100
7	CONFIG_REG7	1000

Table 72. Association between the registers and the "4 bit address field (continued)

#	Register	Content of “4 bit address field” in the upstream
8	RESP (CONFIG_REG8)	1100
9	RESPTIME (CONFIG_REG9)	0000
10	CPS (CONFIG_REG10)	0100
11	DIA_REG1	0001
12	DIA_REG 2	0101
13	DIA_REG 3	1001
14	DIA_REG 4	1101
15	DIA_REG 5	0010
16	DIA_REG 6	0110
17	DIA_REG 7	1010
18	DIA_REG 8	1110
19	DIA_REG 9	0011
20	DIA_REG 10	0111
21	DIA_REG 11	1011
22	ZERO_REG	0100
23	STEP_H	1000
24	STEP_L	1100
25	R IDENT_REG	0000
26	DIA_REG 12	0000
27	RESPTIME	0001
28	REQULO	0101
29	REQUHI	1001
30	RST_AB1_CNT	1101

6.18.3 Registers (Upstream blocks)

Table 73. Registers

Register	Address	Description	Written by	Read by
Upstream read block 1				
CONFIG_REG1	0000b	Configuration register 1	WR_CONFIG1	RD_DATA1
CONFIG_REG2	0100b	Configuration register 2	WR_CONFIG2	RD_DATA1
CONFIG_REG3	1000b	Configuration register 3	WR_CONFIG3	RD_DATA1
CONFIG_REG4	1100b	Configuration register 4	WR_CONFIG4	RD_DATA1
Upstream read block 2				
CONFIG_REG5	0000b	Configuration register 5	WR_CONFIG5	RD_DATA2
CONFIG_REG6	0100b	Configuration register 6	WR_CONFIG6	RD_DATA2
CONFIG_REG7	1000b	Configuration register 7	WR_CONFIG7	RD_DATA2
0x0000	1100b	-	-	RD_DATA2
Upstream read block 3				
DIA_REG1	0001b	Diagnostic register1	-	RD_DATA3
DIA_REG2	0101b	Diagnostic register2	-	RD_DATA3
DIA_REG3	1001b	Diagnostic register3	-	RD_DATA3
DIA_REG4	1101b	Diagnostic register4	-	RD_DATA3
Upstream read block 4				
DIA_REG5	0010b	Diagnostic register5	-	RD_DATA4
DIA_REG6	0110b	Diagnostic register6	-	RD_DATA4
DIA_REG7	1010b	Diagnostic register7	-	RD_DATA4
DIA_REG8	1110b	Diagnostic register8	-	RD_DATA4
Upstream read block 5				
DIA_REG9	0011b	Diagnostic register9	-	RD_DATA5
DIA_REG10	0111b	Diagnostic register10	-	RD_DATA5
DIA_REG11	1011b	Diagnostic register11	-	RD_DATA5
IDENT_REG	1111b	Identifier	-	RD_DATA5
Upstream read block 6				
WD_QUERY	0000b	WDA Query	-	RD_DATA6
0x0000	0100b	Not used	-	RD_DATA6
STEP_CNT_H	1000b	-	-	RD_DATA6
STEP_CNT_L	1100b	-	-	RD_DATA6

Table 73. Registers (continued)

Register	Address	Description	Written by	Read by
Upstream read block 7				
DIA_REG12	0000b	Diagnostic register 12	-	RD_DATA7
DIA_REG12	0100b	Diagnostic register 12	-	RD_DATA7
RESP	1000b	Response to WDA register	-	RD_DATA7
RESPTIME	1100b	MSC RESPTIME register	-	RD_DATA7
Upstream read block 8				
RESPTIME	0001b	-	-	RD_DATA8
REQULO	0101b	-	-	RD_DATA8
REQUHI	1001b	-	-	RD_DATA8
AB1_COUNTER	1101b	-	-	RD_DATA8
CONTR_REG1	-	Command for OUTn, IGNn See Control Registers CONTR_REG1 to 4	Data frame	---
CONTR_REG2	-		Data frame	---
CONTR_REG3	-		Data frame	---
CONTR_REG4	-		Data frame	---

STEP_CNT_H STEPPER COUNTER HIGH

7	6	5	4	3	2	1	0
LINEUP2	LINEUP1	RESERVED	CNT[9:5]				
R							

Address: 1000b

Type: R

Reset: 0000 0000

[7] LINEUP2: used to assure the alignment of high and low part of the counter

[6] LINEUP1: used to assure the alignment of high and low part of the counter

[5] RESERVED: not used

[4:0] CNT[9:5]: high part of steps count

STEP_CNT_L STEPPER COUNTER LOW

7	6	5	4	3	2	1	0
LINEUP2	LINEUP1	RESERVED	CNT[4:0]				
R							

Address: 1100b

Type: R

Reset: 0000 0000

[7] LINEUP2: used to assure the alignment of high and low part of the counter

[6] LINEUP1: used to assure the alignment of high and low part of the counter

[5] RESERVED: not used

[4:0] CNT[4:0]: low part of steps count

IDENT_REG Identity register

7	6	5	4	3	2	1	0
IDENT[2:0]			MCR[2:0]			MSR[1:0]	
R							

Address: 1111b

Type: R

Reset: 0000_0000

[7:5] IDENT[2:0]: chip identifier
000: L9779WD
001
010
011

[4:2] MCR[2:0]: chip revision corresponding to: metal change
000: AA version
001: AB version
010: AC version
110: AD version

[1:0] MSR[1:0]: chip revision corresponding to: full mask set

Configuration register 1, 2, 3

CONFIG_REG1 Configuration register 1

7	6	5	4	3	2	1	0
F_TH_SEL_8[2:0]			F_TM_SEL_8[2:0]			VRS mode	MRD_OT_DID
R/W						R/W	R/W

Address: 0000b

Type: R/W (write access: WRITE_CONFIG1)

Reset: 0000 1000

[7:5] F_TH_SEL_8: OUT8 short fault to VB threshold voltage selection.
000: 0.55 V (default)
001: 1 V
010: 1.5 V
011: 2 V
100: 2.5 V
101: 0.172 V
110: 0.3 V
111: 0.45 V

[4:2] F_TM_SEL_8: OUT8 short fault to VB filter time selection.
000: 1.3 µs
001: 2.6 µs
010: 5.2 µs (default)
011: 10 µs
100: 21 µs
101: 42 µs
110: 84 µs
111: 170 µs

[1] VRS mode:
0 = limited adaptive (default)
1 = full adaptive

[0] MRD_OT_DIS: disables OT switch_off for MRD:
0 = MRD OT switches off the driver
1 = MRD OT does NOT switch off the driver

CONFIG_REG2 Configuration register 2

7	6	5	4	3	2	1	0
F_TH_SEL_9[2:0]			F_TM_SEL_9[2:0]			Charge pump OFF	LS_IGN_OFF
R/W						R	R/W

Address: 0100b

Type: R/W (write access: WRITE_CONFIG2)

Reset: 0000 1000

[7:5] F_TH_SEL_9[2:0]: OUT9 short fault to VB threshold voltage selection.
000: 0.55 V (default)
001: 1 V
010: 1.5 V
011: 2 V
100: 2.5 V
101: 0.150 V
110: 0.3 V
111: 0.45 V

[4:2] F_TM_SEL_9[2:0]: OUT9 short fault to VB filter time selection.
000: 1.3 µs
001: 2.6 µs
010: 5.2 µs (default)
011: 10 µs
100: 21 µs
101: 42 µs
110: 84 µs
111: 170 µs

[1] Charge pump OFF
0= ON (default)
1= OFF

[0] LS_IGN_OFF Control LS stage of IGN driver
0 = normal behaviour
1 = LS of IGN driver always OFF

CONFIG_REG3 Configuration register 3

7	6	5	4	3	2	1	0
RESERVED						EN_FALLING_FILT	HYS_FB_SEL
R/W							

Address: 1000b

Type: R/W (write access: WRITE_CONFIG3)

Reset: 0000 1000

[7:2] RESERVED: not used

[1] EN_FALLING_FILT:
0 = Falling edge filter disabled
1 = Falling edge filter enabled

[0] HYS_FB_SEL:
0 = VRS hyst. Feedback connected before adaptative filter
1 = VRS hyst. Feedback connected after adaptative filter

CONFIG_REG4 Configuration register 4

7	6	5	4	3	2	1	0
PWL_TIMEOUT_CONF[2:0]			OFF_LCDR	FDO_SEL[1:0]		ISO_SRC	LOCK
R/W							

Address: 1100b

Type: R/W (write access: WRITE_CONFIG4)

Reset: 0000_0010

[7:5] PWL_TIMEOUT_CONF[2:0]: Power latch mode time-out configuration.
000: Disabled (default)
001: 4.7 minutes ±5%
010: 9 minutes ±5%
011: 19 minutes ±5%
100: 28 minutes ±5%
101: 37 minutes ±5%
110: 75 minutes ±5%
111: 470 ms ±5%

[4] OFF_LCDR: Off state diagnosis for Low-current drive
1 = Off state diagnosis and the bias current of OUT19, OUT20 is active
0 = Off state diagnosis and the bias current of OUT19, OUT20 is disabled

[3:2] F_DO_SEL[1:0]: Upstream clock ratio selection.
00: fDO= fCL/ 64(default)
01: fDO= fCL/ 16
10: fDO= fCL/ 32
11: fDO= fCL/ 128

[1] ISO_SRC: Slew-rate control for the ISO9141 serial interface (K-Line)
0 = No slew rate limitation
1 = Slew-rate limitation active

[0] LOCK: Lock bit status. Set by LOCK command and cleared with UNLOCK command
1 = ALL configuration registers are locked and cannot be changed
0 = all configuration registers can be changed

CONFIG_REG5 Configuration register 5

7	6	5	4	3	2	1	0
RESERVED	MSC_ACT_EN	VRS_DIAG/ MIN_HYST	VRS_MODE1	VRS_MODE0	VRS_HYST2	VRS_HYST1	VRS_HYST0
R/W							

Address: 0000b

Type: R/W (write access: WRITE_CONFIG5)

Reset: -

Note: 1101_1000

[7] RESERVED: not used

[6] MSC_ACT_EN: MSC activity monitoring enable
1: MSC activity monitoring function is enabled
0: MSC activity monitoring function is disabled

[5] If fully adaptive mode selected:
VRS diag: VRS diagnosis enable
1: diagnosis function is enabled
0: diagnosis function is disabled

If limited adaptive mode selected:
Forces VRS minimum hysteresis (5 µA)
1: minimum hysteresis forced
0: normal operation as per VRS_HYST configuration

[4:3] VRS_MODE
00: internal auto-adaptive filter time OFF, Internal auto-adaptive hysteresis OFF
01: internal auto-adaptive filter time OFF, Internal auto-adaptive hysteresis ON
10: Iinternal auto-adaptive filter time ON, Internal auto-adaptive hysteresis OFF
11: internal auto-adaptive filter time ON, Internal auto-adaptive hysteresis ON

[2:0] VRS_HYST
000: Hys current = 17 µA (Hys VRS = 347 mV with 10 kΩ ext resistors) [default]
001: Hys current = 5 µA (Hys VRS=100mV with 10 kΩ ext resistors)
010: Hys current = 10 µA (Hys VRS=200mV with 10 kΩ ext resistors)
011: Hys current = 17 µA (Hys VRS=347mV with 10 kΩ ext resistors)
100: Hys current = 32 µA (Hys VRS=644mV with 10 kΩ ext resistors)
101: Hys current = 51 µA (Hys VRS=967mV with 10 kΩ ext resistors)
110: Hys current = 17 µA (Hys VRS=347mV with 10 kΩ ext resistors)
111: Hys current = 0 µA (used only for test purpose)

Note: When VRS limited amplitude adaptive mode is set, VRS_HYST limits the minimum hysteresis to the set value.

When VRS limited mode is set, filter time must be enabled at operation start, and shall never be disabled afterwards.

When VRS limited mode is set, VRS diagnostic function is not available.

CONFIG_REG6 Configuration register 6

7	6	5	4	3	2	1	0
CAN_ERR_EN	NL_RST	PWL_EN_N/ SEO_EN_N	PSOFF	VDD5_UV mask	VDD5 under voltage on SDO	WDA time base setting (RESPTIME)	PWL/SEO timeout
R/W							

Address: 0100b

Type: R/W (write access: WRITE_CONFIG6)

Reset: 0010 0010

[7] CAN_ERR_EN: CAN error handling
1: CAN error handling enabled
0: CAN error handling disabled

[6] NL_RST: Reset generation during Power latch mode when KEY_ON 0 --> 1
1: reset generated
0: reset not generated

[5] PWL_EN_N: Power latch mode enable
PWL_EN_N/SEO_EN_N: Power latch/secure engine off mode enable
1: power latch mode function is disabled (default)
0: power latch mode function is enabled

[4] PSOFF: Power supply off (VDD5, VTRK1, VTRK2, Charge-pump, internal supply) when KEY_ON = 0 and PWL_EN_N = 1
0: switch off power supply and switch off MRD
1: do not switch off power supply and switch off MRD

[3] VDD5_UV mask
1: mask VDD5_UV
0: mask removed (default)
Note: if VDD5_UV is masked, OUTx are not automatically switched off.

[2] VDD5 under voltage on SDO
1: VDD5 under voltage event forces SDO to constantly send Low logic values whenever SDO output is enabled, till VDD5 under voltage monitor remains active
0: this function disabled (default)
Note: as SDO gets stuck to Low upon VDD5_UV event, before any further readings, it is recommended that this function is disabled.

[1] WDA time base setting
This bit selects the RESPTIME time base
1: (default) sets time base to 1/64 kHz
0: sets time base to 1/39 kHz

[0] PWL/SEO timeout
0: PWL timeout counter has priority over SEO (default)
1: SEO timeout counter has priority over PW
Note: if this bit is set, bit4 and bit5 of same register have no effects

Table 74. CONFIG_REG6 power off source

Reg6-bit5	Reg6-bit0	Power off source: WATCHDOG	Power off source: KEY OFF	Power off source: TIMEOUT (REG4 bit7..5)	SEO (OUT1…4 OUT13/ OUT14)	Description
1	0		X			Direct switch-off at KEY_ON=0(default)
1	1	X	(X)			Switch-off in case of Watch-dog error
0	0	X	(X)	X	X	Switch-off at expiration of PWL timer SEO enabled for OUT1-4, OUT13,14
0	1	X	(X)		X	Switch-off in case of Watchdog error SEO enabled for OUT1-4, OUT13,14

CONFIG_REG7 Configuration register 7

7	6	5	4	3	2	1	0
IGN_DIA_MODE	IGN_DIA_SGEN	TD_MASK_X2	RESERVED	OUT25_EN_LB	OUT21_EN_LB	OUT14_EN_LB	OUT13_EN_LB
R/W							

Address: 1000b

Type: R/W (write access: WRITE_CONFIG7)

Reset: 0101 0000

[7] IGN_DIA_MODE: IGN diagnosis mode for short to battery:
1: latch mode
0: no latch mode

[6] IGN_DIA_SGEN: IGN diagnosis enable for short to ground:
1: Current diagnosis enabled
0: Voltage diagnosis enabled

[5] TD_MASK_X2:
0: Td_mask as specified in respective tables for OUT13 to OUT28
1: Td_mask doubled for OUT13 to OUT28

[4] RESERVED: not used

[3] OUT25_EN_LB: Low battery function enable
1: LB function is enabled for OUT25
0: LB function is disabled for OUT25

[2] OUT21_EN_LB: Low battery function enable
1: LB function is enabled for OUT21
0: LB function is disabled for OUT21

[1] OUT14_EN_LB: Low battery function enable
1: LB function is enabled for OUT14
0: LB function is disabled for OUT14

[0] OUT13_EN_LB: Low battery function enable
1: LB function is enabled for OUT13
0: LB function is disabled for OUT13

Note: The bit OUT21,25_EN_LB has priority over the CPS_CONFx bit, this means that if one of OUT21,25_EN_LB is set to 1 the OUT21…28 become independent power stages.

CONFIG_REG10 (CPS Configuration register) Configuration register 10

7	6	5	4	3	2	1	0
see *Table 39* and *40*							CPS_CONF
-							

Address: -

Type: WR_CPS

Reset: 0000 0001

[7:1] See *Table 39* and *40*

[0] CPS_CONF
1: OUT21...OUT28 are configured as 2 full-bridge for stepper motor driving (default)
0: OUT21...OUT24 are configured as single power stages

DIA_REG[1:5] Diagnostic register 1, 2, 3, 4, 5

	7	6	5	4	3	2	1	0
DIA_REG1	OUT4_DIAG		OUT3_DIAG		OUT2_DIAG		OUT1_DIAG	
DIA_REG2	OUT8_DIAG		OUT7_DIAG		OUT6_DIAG		OUT5_DIAG	
DIA_REG3	OUT14_DIAG		OUT13_DIAG		WDA_STATUS	RESERVED	OUT9_DIAG	
DIA_REG4	OUT18_DIAG		OUT17_DIAG		OUT16_DIAG		OUT15_DIAG	
DIA_REG5	RESERVED				OUT20_DIAG		OUT19_DIAG	

Address: 0001b, 0101b, 1001b, 1101b, 0010b

Type: R (Read only)

Reset:

DIA_REG1:[7:6] OUT4_DIAG: Diagnosis bit of power stage OUT4
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

DIA_REG1:[5:4] OUT3_DIAG: Diagnosis bit of power stage OUT3
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

DIA_REG1:[3:2] OUT2_DIAG: Diagnosis bit of power stage OUT2
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

DIA_REG1:[1:0] OUT1_DIAG: Diagnosis bit of power stage OUT1
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

DIA_REG2:[7:6] OUT8_DIAG: Diagnosis bit of power stage OUT8
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

DIA_REG2:[5:4] OUT7_DIAG: Diagnosis bit of power stage OUT7
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

DIA_REG2:[3:2] OUT6_DIAG: Diagnosis bit of power stage OUT6
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

DIA_REG2:[1:0] OUT5_DIAG: Diagnosis bit of power stage OUT5
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

DIA_REG3:[7:6] OUT14_DIAG: Diagnosis bit of power stage OUT14
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

DIA_REG3:[5:4] OUT13_DIAG: Diagnosis bit of power stage OUT13
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

DIA_REG3:[3]]WDA STATUS: status of WDA pin, not latched

DIA_REG3:[2] RESERVED: not used

DIA_REG3:[1:0] OUT9_DIAG: Diagnosis bit of power stage OUT9
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

DIA_REG4:[7-6] OUT18_DIAG: Diagnosis bit of power stage OUT18
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

DIA_REG4:[5-4] OUT17_DIAG: Diagnosis bit of power stage OUT17
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

DIA_REG4:[3-2] OUT16_DIAG: Diagnosis bit of power stage OUT16
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

DIA_REG4:[1-0] OUT15_DIAG: Diagnosis bit of power stage OUT15
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

DIA_REG5:[7:4] RESERVED: All bit read 1

DIA_REG5:[3-2] OUT20_DIAG: Diagnosis bit of power stage OUT20
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

DIA_REG5:[1-0] OUT19_DIAG: Diagnosis bit of power stage OUT19
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

Note: All diagnosis bit (including OT1, F1, OT2, F2) will be cleared automatically by reading – i.e. if a diagnosis bits indicates a fault this fault has occurred after the last read access to this register.

Diagnostic register 6 and 7

DIA_REG6 Diagnostic register 6

	7	6	5	4	3	2	1	0
Configured as single power stages	OUT24_DIAG		OUT23_DIAG		OUT22_DIAG		OUT21_DIAG	
Configured as H bridge	H1_DIAG							

Address: 0110b

Type: R (Read only)

Reset:

Configured as single power stages

[7-6] OUT24_diag[1:0]: Diagnosis bit of OUT24
00: Short-circuit to ground
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

[5-4] OUT23_diag[1:0]: Diagnosis bit of OUT23
00: Short-circuit to VB
01: Open load (OL)
10: Short-circuit to GND
11: Power stage OK NO FAIL

[3-2] OUT22_diag[1:0]: Diagnosis bit of OUT22
00: Short-circuit to ground
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

[1-0] OUT21_diag[1:0]: Diagnosis bit of OUT21
00: Short-circuit to VB
01: Open load (OL)
10: Short-circuit to GND
11: Power stage OK NO FAIL

Configured as H bridge

[7-0] H1_diag[7:0]: Diagnosis bit of H1 bridge
00000001: Short to Ground (OFF)
00000101: Short to VBAT (OFF)
00000100: Open Load (OFF)
00000010: Open Load (ON)
00000011: Over current (ON)
00000111: Fault detection running (ON)
11111111: Power stages OK NO FAULT
All other combinations: NOT USED

DIA_REG7 Diagnostic register 7

	7	6	5	4	3	2	1	0
Configured as single power stages	OUT28_DIAG		OUT27_DIAG		OUT26_DIAG		OUT25_DIAG	
Configured as H bridge	H2_DIAG							

Address: 1010b

Type: R (Read only)

Reset:

Configured as single power stages

[7-6] OUT28_DIAG[1:0]: Diagnosis bit of OUT28
00: Short-circuit to ground
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

[5-4] OUT27_DIAG[1:0]: Diagnosis bit of OUT27
00: Short-circuit to ground
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage OK NO FAIL

[3-2] OUT26_DIAG[1:0]: Diagnosis bit of OUT26
00: Short-circuit to VB
01: Open load (OL)
10: Short-circuit to GND
11: Power stage OK NO FAIL

[1-0] OUT25_DIAG[1:0]: Diagnosis bit of OUT25
00: Short-circuit to VB
01: Open load (OL)
10: Short-circuit to GND
11: Power stage OK NO FAIL

Configured as H bridge

[7-0] H2_diag[7:0]: Diagnosis bit of H2 bridge
00000001: Short to Ground (OFF)
00000101: Short to VBAT (OFF)
00000100: Open Load (OFF)
00000010: Open Load (ON)
00000011: Over current (ON)
00000111: Fault detection running (ON)
11111111: Power stages OK NO FAULT
All other combinations: NOT USED

DIA_REG8 Diagnostic register 8

7	6	5	4	3	2	1	0
IGN4_DIAG[1:0]		IGN3_DIAG[1:0]		IGN2_DIAG[1:0]		IGN1_DIAG[1:0]	

Address: 1110b

Type:

Reset:

[7:6] IGN4_DIAG[1:0]: Diagnosis bit of IGN4
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage ok NO FAIL

[5:4] IGN3_DIAG[1:0]: Diagnosis bit of IGN3
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage ok NO FAIL

[3:2] IGN2_DIAG[1:0]: Diagnosis bit of IGN2
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage ok NO FAIL

[1:0] IGN1_DIAG[1:0]: Diagnosis bit of IGN1
00: Short-circuit to ground (SCG)
01: Open load (OL)
10: Short-circuit to BAT (SCB)
11: Power stage ok NO FAIL

DIA_REG9 Diagnostic register 9

7	6	5	4	3	2	1	0
KEY_ON_STATUS	MRD_OVC	VRS_STAT	VRS_DIAG	VTRK2_DIAG[1:0]		VTRK1_DIAG[1:0]	
R/W							

Address: 0011b

Type:

Reset:

[7] KEY_ON_STATUS
1: KEY_ON voltage above KEY_ON_H
0: KEY_ON voltage below KEY_ON_L

[6] MRD_OVC
1: Current MRD status is OFF due to previous Over current
0: Current MRD status is ON (no OVC detected)

[5] VRS_STAT
1: Diag ON
0: Diag OFF

[4] VRS_DIAG
0: No Fault
1: Generic fault detected

This function is only available if VRS is set to fully adaptive mode. When limited adaptive mode is set, VRS_DIAG always returns 0.

[3-2] VTRK2_DIAG[1:0]: Diagnosis bit of VTRK2
00: Not used
01: Overload condition/out of regulation
10: Overvoltage (OV) or over temperature (OT) (Lower priority respect to Overload condition)
11: Sensor supply VTRK ok NO FAIL

[1-0] VTRK1_DIAG[1:0]: Diagnosis bit of VTRK1
00: Not used
01: Overload condition/out of regulation
10: Overvoltage (OV) or over temperature (OT) (Lower priority respect to overload condition)
11: Sensor supply VTRK OK NO FAIL

DIA_REG10 Diagnostic register 10

7	6	5	4	3	2	1	0
TNL_RST	F1	CRK_RST	F2	VDD5_OV	V3V3_UV	OUT_DIS	OV_RST

Address: 0111b

Type:

Reset:

[7] TNL_RST
0: No reset generated
1: Reset generated by TNL

[6] F1
0: No fault
1: any fault occurred in OUT1...10, OUT13...20, IGN1…4

[5] CRK_RST
0: No reset generated
1: Reset generated by VDD_UV (t<THOLD)

[4] F2
0: No fault
1: any fault occurred in OUT21...28

[3] VDD5_OV
0: No fault
1: Overvoltage on VDD5 regulator

[2] V3V3_UV
0: No fault
1: Undervoltage on V3V3 regulator

[1] OUT_DIS
0: All OUT can be switched ON
1: All OUT disabled (except MRD and supplies)

[0] OV_RST
0: No fault
1: Power stages were switched off due to battery overvoltage

Note: <OUT_DIS>: this bit has to be set to 0 with the command START before power stages OUTx and IGNx can be activated. As long as <OUT_DIS>=1 any data for these power stages is ignored. It is not affected by reading, and it is reset by POR, software reset SW_RST command and when the RST pin is asserted.

DIA_REG11 Diagnostic register 11

7	6	5	4	3	2	1	0
OT1	OT2	OT3	OT4	VDD5UV_RST	CAN_ERROR	TRANS_L	TRANS_F

Address: 1011b

Type:

Reset:

[7] OT1
0: No fault
1: Over temperature occurred in VTRK1,2

[6] OT2
0: No fault
1: Over temperature occurred in the OUTx and IGNx

[5] OT3
0: No fault
1: Over temperature occurred in MRD

[4] OT4
0: No fault
1: Over temperature occurred in V3V3

[3] VDD5UV_RST
0: No reset generated
1: Reset generated by VDD_UV (t >THOLD)
Note: if VDD5_UV is masked, the VDD5_UV event is anyhow latched.

[2] CAN_ERROR
0: No fault
1: fault present (one of the 4 possible error on CAN)

[1] TRANS_L
0: No fault
1: data frame length incorrect

[0] TRANS_F
0: No fault
1= no data stream within time-out

DIA_REG12 Diagnostic register 12

7	6	5	4	3	2	1	0
VDDIO_UNDERVOLTAGE	WDG_RST (latched)	SEO OUT1-4	SEO OUT13-14	WDG_RST (latched)	RESERVED		KEY_ON_FLT

Address: 0000b

Type:

Reset:

[7] VDDIO_UNDERVOLTAGE:
It goes to 1, if VDDIO undervoltage longer than 225 ms

[6] WDG_RST latched:
1: WDA has generated a RST event
0: no event

[5] SEO event when the OUT1-4 are switched off after 225 ms

[4] SEO event when the OUT13-14 after 600ms when KEY is OFF

[3] WDG_RST not latched:
1: WDA has generated a RST event
0: no event

[2:1] RESERVED: not used

[0] KEY_ON_FLT: Key on after filter

Note: the DIA_REG12 is read by READ_DATA 7 but reset by READ_DATA5.

Bit4 and bit5 are usable when power-latch enable bit in CONF6 Bit 5 is set to 0. SEO Flags are set to 1 after delay if KEY_ON is low or if a WDA event occurs with CONF6 Bit 5 already set to 0. In the latter case the KEY_ON may be high but SEO bits are nevertheless set.

Control registers CONTR1 to 4

Control registers are written with the data frame. (Remember: D1 is the second least bit of the data frame - the LSB D0 is the "data selection bit" with D0='0'. The bit D0 is the first bit received by the L9779WD on the downstream channel in a data frame!).

They control the output stages OUT1…10, OUT13…20, OUT21…28 and IGNn.

CMD = 1 OUTPUT ONCMD = 0 OUTPUT OFF

CONTR_REG1 Control register 1

7	6	5	4	3	2	1	0
CMD_OUT1	CMD_OUT2	CMD_OUT3	CMD_OUT4	CMD_OUT5	CMD_OUT20	CMD_OUT8	CMD_OUT19
R/W							

Address:

Type: Via DATA frame

Reset: 0000 0000 (ALL outputs switched OFF)

[7] CMD_OUT1
1: OUT1 - Power stage switched ON
0: OUT1 - Power stage switched OFF

[6] CMD_OUT2
1: OUT2 - Power stage switched ON
0: OUT2 - Power stage switched OFF

[5] CMD_OUT3
1: OUT3 - Power stage switched ON
0: OUT3 - Power stage switched OFF

[4] CMD_OUT4
1: OUT4 - Power stage switched ON
0: OUT4 - Power stage switched OFF

[3] CMD_OUT5
1: OUT5 - Power stage switched ON
0: OUT5 - Power stage switched OFF

[2] CMD_OUT20
1: OUT20 - Power stage switched ON
0: OUT20 - Power stage switched OFF

[1] CMD_OUT8
1: OUT8 - Power stage switched ON
0: OUT8 - Power stage switched OFF

[0] CMD_OUT19
1: OUT19 - Power stage switched ON
0: OUT19 - Power stage switched OFF

CONTR_REG2 Control register 2

7	6	5	4	3	2	1	0
CMD_OUT15	CMD_OUT14	DON'T CARE	CMD_OUT9	CMD_IGN1	CMD_IGN2	CMD_IGN3	CMD_IGN4

Address:

Type: Via DATA frame

Reset: 0000 0000 (ALL outputs switched OFF)

[7] CMD_OUT15
1: OUT15 - Power stage switched ON
0: OUT15 - Power stage switched OFF

[6] CMD_OUT14
1: OUT14 - Power stage switched ON
0: OUT14 - Power stage switched OFF

[5] DON'T CARE

[3] CMD_OUT9
1: OUT9 - Power stage switched ON
0: OUT9 - Power stage switched OFF

[4] CMD_IGN1
1: IGN1 - Power stage switched ON
0: IGN1 - Power stage switched OFF

[2] CMD_IGN2
1: IGN2 - Power stage switched ON
0: IGN2 - Power stage switched OFF

[1] CMD_IGN3
1: IGN3 - Power stage switched ON
0: IGN3 - Power stage switched OFF

[0] CMD_IGN4
1: IGN4 - Power stage switched ON
0: IGN4 - Power stage switched OFF

CONTR_REG3 Control register 3

	7	6	5	4	3	2	1	0
CPS_CONF = 0	CMD_OUT22	CMD_OUT21	CMD_OUT16	CMD_OUT13	CMD_OUT17	CMD_OUT18	CMD_OUT7	CMD_OUT6
CPS_CONF = 1	DIR	ENABLE						

Address:

Type: Via DATA frame

Reset: 0000 0000 (ALL outputs switched OFF)

0 CMD_OUT6
1: OUT6 - Power stage switched ON
0: OUT6 - Power stage switched OFF

1 CMD_OUT7
1: OUT7 - Power stage switched ON
0: OUT7 - Power stage switched OFF

2 CMD_OUT18
1: OUT18 - Power stage switched ON
0: OUT18 - Power stage switched OFF

3 CMD_OUT17
1: OUT17 - Power stage switched ON
0: OUT17 - Power stage switched OFF

4 CMD_OUT13
1: OUT13 - Power stage switched ON
0: OUT13 - Power stage switched OFF

5 CMD_OUT16
1: OUT16 - Power stage switched ON
0: OUT16 - Power stage switched OFF

6 CMD_OUT21
1: OUT21 - Power stage switched ON (High side driver)
0: OUT21 - Power stage switched OFF
Note: If CPS_CONF=0 (single power stages configuration)
ENABLE
0: stepper motor driver disabled
1: stepper motor driver enabled
Note: If CPS_CONF=1(stepper motor driving configuration)

7 CMD_OUT22
1: OUT22 - Power stage switched ON
Note: If CPS_CONF=0 (single power stages configuration)
0: OUT22 - Power stage switched OFF
DIR
0: forward direction
1: backward direction
Note: if CPS_CONF=1(stepper motor driving configuration)

Note: The meaning of some CONTR_REG3 bit depends on the configuration of bit CPS_CONF of CONF_REG1.

CONTR_REG4 Control register 4

	7	6	5	4	3	2	1	0
CPS_CONF = 0	RESERVED		CMD_OUT28	CMD_OUT27	CMD_OUT26	CMD_OUT25	CMD_OUT24	CMD_OUT23
CPS_CONF = 1								PWM

Address:

Type:

Reset: 0000 0000 (ALL outputs switched OFF)

[6-7] RESERVED: NOT used

[5] CMD_OUT28
1: OUT28 Power stage switched ON
0: OUT28 Power stage switched OFF

[4] CMD_OUT27
1: OUT27 Power stage switched ON
0: OUT27 Power stage switched OFF

[3] CMD_OUT26
1: OUT26 - Power stage switched ON (High side driver)
0: OUT26 - Power stage switched OFF

[2] CMD_OUT25
1: OUT25 - Power stage switched ON (High side driver)
0: OUT25 - Power stage switched OFF

[1] CMD_OUT24
1: OUT24 - Power stage switched ON
0: OUT24 - Power stage switched OFF

[0] If CPS_CONF=0 (single power stages configuration)
CMD_OUT23
1: OUT23 Power stage switched ON
0: OUT23 Power stage switched OFF

if CPS_CONF=1(stepper motor driving configuration)
PWM
1 →0: no step change in the driving sequence
0 →1: step change in the driving sequence (next step applied)

Note: The meaning of some CONTR_REG4 bit depends on the configuration of bit CPS_CONF of CONF_REG1.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK® is an ST trademark.

7.1 HiQUAD-64 package information

Figure 84. HiQUAD-64 package outline

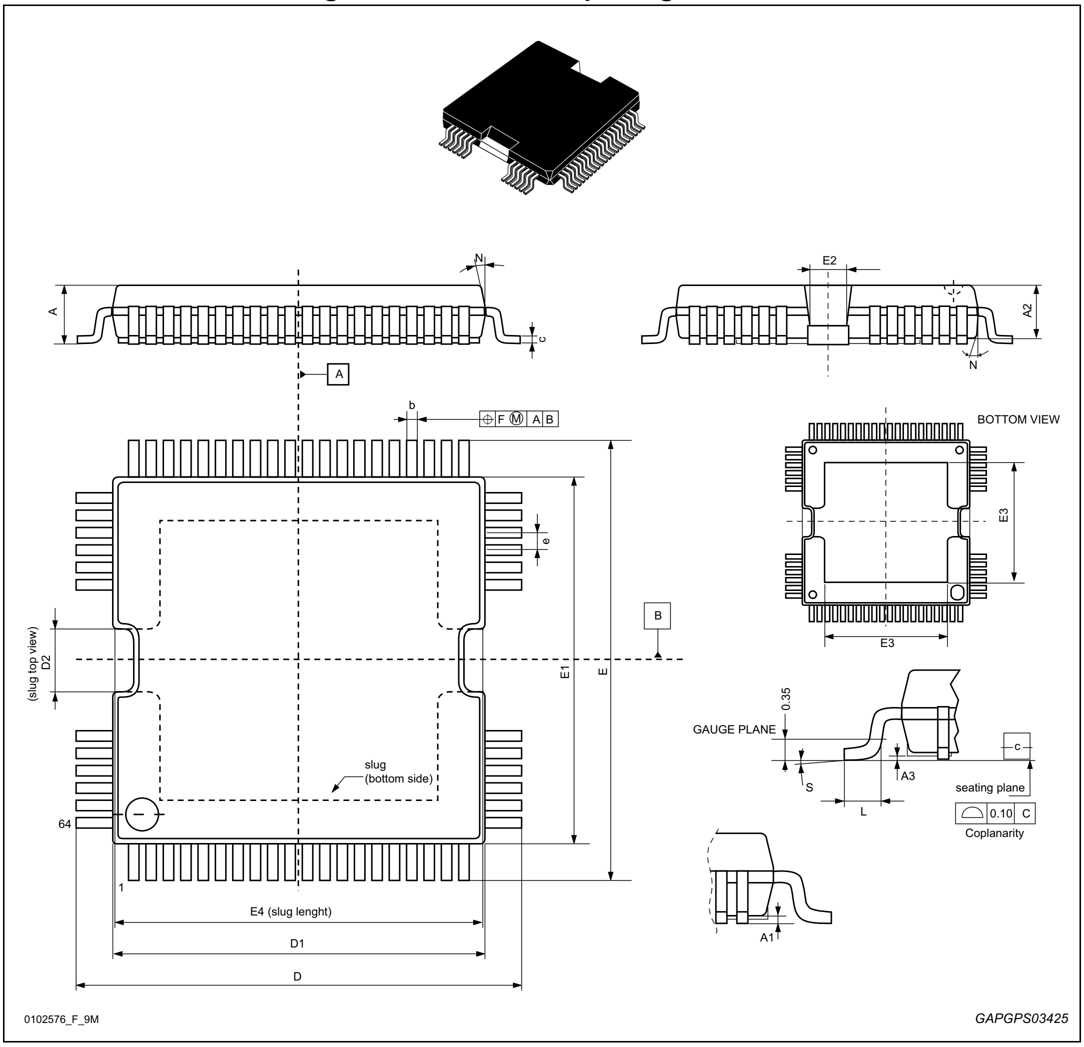


Table 75. HiQUAD-64 package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	3.15	-	-	0.1240
A1	0	-	0.25	0	-	0.0098
A2	2.50	-	2.90	0.0984	-	0.1142
A3	0	-	0.10	0	-	0.0039
b	0.22	-	0.38	0.0087	-	0.0150
c	0.23	-	0.32	0.0091	-	0.0126
D[2]	17.00	-	17.40	0.6693	-	0.6850
D1	13.90	14.00	14.10	0.5472	0.5512	0.5551
D2	2.65	2.80	2.95	0.1043	0.1102	0.1161
E	17.00	-	17.40	0.6693	-	0.6850
E1[1]	13.90	14.00	14.10	0.5472	0.5512	0.5551
E2	2.35	-	2.65	0.0925	-	0.1043
E3	9.30	9.50	9.70	0.3661	0.3740	0.3819
E4	13.30	13.50	13.70	0.5236	0.5315	0.5394
e	-	0.65	-	-	0.0256	-
F	-	0.12	-	-	0.0047	-
G	-	0.10	-	-	0.0039	-
L	0.80	-	1.10	0.0315	-	0.0433
N	-	-	10°	-	-	10°
s	0°	-	7°	0°	-	7°

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006inc.).

8 Revision history

Table 76. Document revision history

Date	Revision	Changes
3-Feb-2015	1	Initial release.
19-Mar-2015	2	Removed reference to L9779WDM from document. Updated: *Table 4: ESD protection on page 19*; In *Table 42: CAN transceiver electrical characteristics* the values of the $V_{CANHL,CM}$ parameter.
08-Apr-2015	3	Modified on *Table 34* page 84 for “Diagnostic high threshold” parameter the max. value in 3 V.
20-May-2015	4	Updated *Table 63 on page 135* and *Table 71 on page 139*.
14-Sep-2015	5	Updated: *Table 35 on page 87* and *Table 36 on page 88*.