ZL2106

6A Digital-DC Synchronous Step-Down DC/DC Converter

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The ZL2106 is a digital power conversion and management IC that combines an integrated synchronous step-down DC/DC converter with key power management functions in a small package, resulting in a flexible and integrated solution.

The ZL2106 can provide an output voltage from 0.54V to 5.5V (with margin) from an input voltage between 4.5V and 14V. Internal low $r_{DS(ON)}$ synchronous power MOSFETs enable the ZL2106 to deliver continuous loads up to 6A with high efficiency. An internal Schottky bootstrap diode reduces discrete component count. The ZL2106 also supports phase spreading to reduce system input capacitance.

Power management features such as digital soft-start delay and ramp, sequencing, tracking, and margining can be configured by simple pin-strapping or through an on-chip serial port. The ZL2106 uses the PMBus™ protocol for communication with a host controller and the Digital-DC bus for interoperability between other Zilker Labs devices.

Features

- Integrated MOSFET switches
- 6A continuous output current
- ±1% output voltage accuracy
- *Snapshot™* parametric capture
- I^2C/SMBus interface, PMBus compatible
- Internal non-volatile memory (NVM)

Applications

- Telecom, Networking, Storage equipment
- Test and Measurement equipment
- Industrial control equipment
- 5V and 12V distributed power systems

Related Literature

- AN1468 “ZL2106EVAL1Z Evaluation Board”, USB Adapter Board, GUI Software
- AN2010 “Thermal and Layout Guidelines for Digital-DC™ Products”
- AN2033 “Zilker Labs PMBus Command Set-DDC ProductsPMBus Command Set”
- AN2035 “Compensation Using CompZL™”

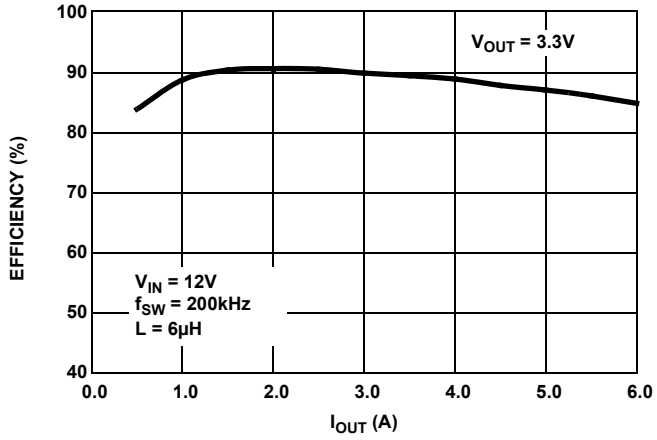

FIGURE 1. ZL2106 EFFICIENCY

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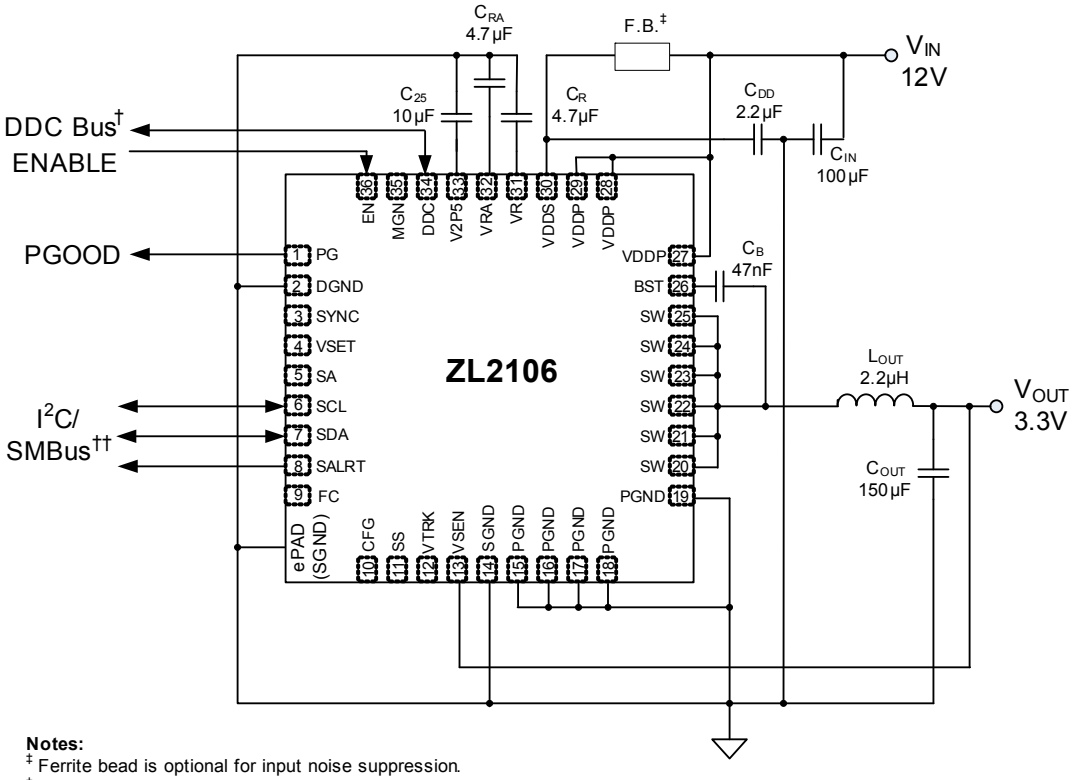
Typical Application Circuit

The following application circuit represents a typical implementation of the ZL2106. For PMBus operation, it is recommended to tie the enable pin (EN) to SGND.



Notes:

‡ Ferrite bead is optional for input noise suppression.

† The DDC bus pull-up resistance will vary based on the capacitive loading of the bus, including the number of devices connected. The 10 kΩ default value, assuming a maximum of 100 pF per device, provides the necessary 1 µs pull-up rise time. Please refer to the Digital-DC Bus section for more details.

†† The I²C/SMBus pull-up resistance will vary based on the capacitive loading of the bus, including the number of devices connected. Please refer to the I²C/SMBus specifications for more details.

FIGURE 2. 12V TO 3.3V/6A APPLICATION CIRCUIT (5ms SS DELAY, 5ms SS RAMP)

Block Diagram

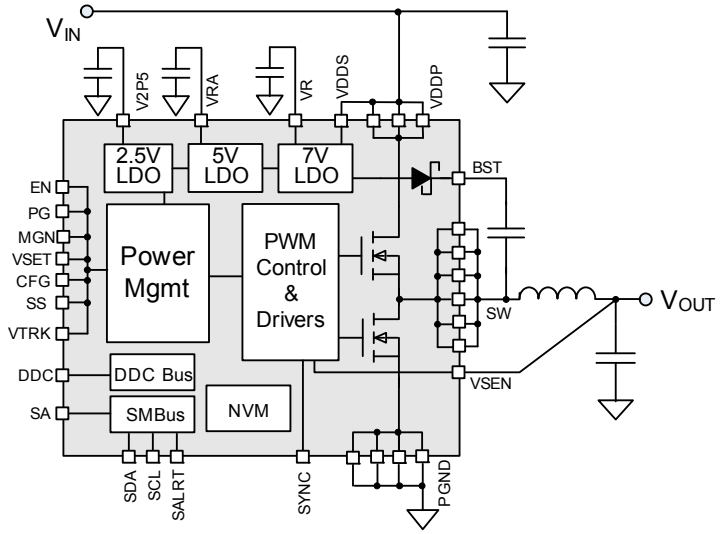


FIGURE 3. BLOCK DIAGRAM

Pin Configuration

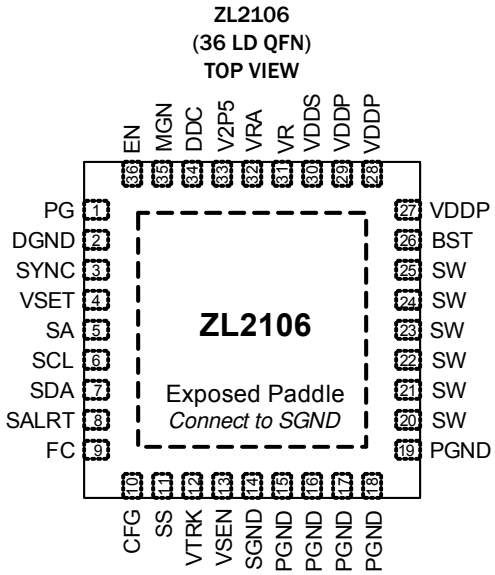


FIGURE 4.

Pin Descriptions

PIN	LABEL	TYPE (Note 1)	DESCRIPTION
1	PG	O	Power-good. This pin transitions high 100ms after output voltage stabilizes within regulation band. Selectable open drain or push-pull output. Factory default is open drain.
2	DGND	PWR	Digital ground. Common return for digital signals. Connect to low impedance ground plane.
3	SYNC	I/O, M (Note 2)	Clock synchronization pin. Used to set switching frequency of internal clock or for synchronization to external frequency reference.
4	VSET	I, M	Output voltage select pin. Used to set V_{OUT} set-point and V_{OUT} max.
5	SA	I, M	Serial address select pin. Used to assign unique SMBus address to each IC.
6	SCL	I/O	Serial clock. Connect to external host interface.
7	SDA	I/O	Serial data. Connect to external host interface.
8	SALRT	O	Serial alert. Connect to external host interface if desired.
9	FC	I, M	Loop compensation select pin. Used to set loop compensation.
10	CFG	I, M	Configuration pin. Used to control the SYNC pin, sequencing and enable tracking.
11	SS	I, M	Soft-start pin. Used to set the ramp delay and ramp time, sets UVLO and configure tracking.
12	VTRK	I	Track sense pin. Used to track an external voltage source.
13	VSEN	I	Output voltage positive feedback sensing pin.
14	SGND	PWR	Common return for analog signals. Connect to low impedance ground plane.
15, 16, 17, 18, 19	PGND	PWR	Power ground. Common return for internal switching MOSFETs. Connect to low impedance ground plane.
20, 21, 22, 23, 24, 25	SW	I/O	Switching node (level-shift common).
26	BST	PWR	Bootstrap voltage for level-shift driver (referenced to SW).
27, 28, 29	VDDP	PWR	Bias supply voltage for internal switching MOSFETs (return is PGND).
30	VDDS	PWR	IC supply voltage (return is SGND).

Pin Descriptions (Continued)

PIN	LABEL	TYPE (Note 1)	DESCRIPTION
31	VR	PWR	Regulated bias from internal 7V low-dropout regulator (return is PGND). Decouple with a 4.7µF capacitor to PGND.
32	VRA	PWR	Regulated bias from internal 5V low-dropout regulator for internal analog circuitry (return is SGND). Decouple with a 4.7µF capacitor to SGND.
33	V2P5	PWR	Regulated bias from internal 2.5V low-dropout regulator for internal digital circuitry (return is DGND). Decouple with a 10µF capacitor.
34	DDC	I/O	Digital-DC Bus (open drain). Interoperability between Zilker Labs devices.
35	MGN	I	Margin pin. Used to enable margining of the output voltage.
36	EN	I	Enable pin. Used to enable the device (active high).
ePad	SGND	PWR	Exposed thermal pad. Common return for analog signals. Connect to low impedance ground plane.

NOTES:

1. I = Input, O = Output, PWR = Power or Ground, M = Multi-mode pins. Please refer to Section “Multi-mode Pins” on page 11.
2. The SYNC pin can be used as a logic pin, a clock input or a clock output.

Ordering Information

PART NUMBER (Note 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
ZL2106ALCF (Note 2)	2106	-40 to +85	36 Ld 6mmx6mm QFN	L36.6x6C
ZL2106ALCFT (Notes 1, 2)	2106	-40 to +85	36 Ld 6mmx6mm QFN	L36.6x6C
ZL2106ALCFTK (Notes 1, 2)	2106	-40 to +85	36 Ld 6mmx6mm QFN	L36.6x6C

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ZL2106. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

DC Supply Voltage for VDDP, VDDS Pins . . . . . -0.3V to 17V
High-Side Supply Voltage for BST Pin. . . . . -0.3V to 25V
High-Side Boost Voltage for BST - SW Pins . . . . . -0.3V to 8V
Internal MOSFET Reference for VR Pin . . . . . -0.3V to 8.5V
Internal Analog Reference for VRA Pin . . . . . -0.3V to 6.5V
Internal 2.5 V Reference for V2P5 Pin. . . . . -0.3V to 3V
Logic I/O Voltage for EN, CFG, DDC, FC, MGN, PG, SDA, SCL, SA, SALRT, SS, SYNC, VTRK, VSET, VSEN Pins . . . . . -0.3V to 6.5V
Ground Differential for DGND - SGND, PGND - SGND Pins . . . . . ±0.3V
MOSFET Drive Reference Current for VR Pin
Internal Bias Usage 20mA
Switch Node Current for SW Pin
Peak (Sink Or Source) 10A
ESD Rating
Human Body Model 2kV
Machine Model 500V
Latch-Up. . . . . per JESD78 (JEDEC Standard)

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
36 Ld QFN (Notes 4, 5)	28	1.7

Junction Temperature Range . . . . . -55°C to +150°C
Storage Temperature Range. . . . . -55°C to +150°C
Dissipation Limits (Note 6)
T_A = +25°C 3.5W
T_A = +55°C 2.5W
T_A = +85°C 1.4W
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Input Supply Voltage Range, VDDP, VDDS (See Figure 14)
VDDS tied to VR, VRA. . . . . 4.5V to 5.5V
VDDS tied to VR, VRA Floating . . . . . 5.5V to 7.5V
VR, VRA Floating. . . . . 7.5V to 14V
Output Voltage Range, V_{OUT} (Note 7) . . . . . 0.54V to 5.5V
Operating Junction Temperature Range, T_J . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. Thermal impedance depends on layout.
7. Includes margin limits.

Electrical Specifications

V_{DDP} = V_{DDS} = 12V, T_A = -40°C to +85°C unless otherwise noted. (Note 8) Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	CONDITIONS	MIN (Note 18)	TYP	MAX (Note 18)	UNIT
Input and Supply Characteristics					
I_{DD} Supply Current	f_{SW} = 200kHz, no load		11	**20**	mA
	f_{SW} = 1MHz, no load		15	**30**	mA
I_{DDS} Shutdown Current	EN = 0V, No I^2C/SMBus activity		0.6	**1**	mA
VR Reference Output Voltage	V_{DD} > 8V, I_{VR} < 10mA	**6.5**	7.0	**7.5**	V
VRA Reference Output Voltage	V_{DD} > 5.5V, I_{VRA} < 20mA	**4.5**	5.1	**5.5**	V
V2P5 Reference Output Voltage	I_{V2P5} < 20mA	**2.25**	2.5	**2.75**	V
Output Characteristics					
Output Current	I_{RMS}, Continuous			**6**	A
Output Voltage Adjustment Range (Note 9)	V_{IN} > V_{OUT}	**0.6**		**5.0**	V
Output Voltage Setpoint Resolution	Set using resistors		10		mV
	Set using I^2C/SMBus		±0.025		% FS (Note 10)
V_{SEN} Output Voltage Accuracy	Includes line, load, temp	**-1**		**1**	%
V_{SEN} Input Bias Current	V_{SEN} = 5.5V		110	**200**	µA
Soft-start Delay Duration Range (Note 11)	Set using SS pin or resistor	**2**		**20**	ms
	Set using I^2C/SMBus	**0.002**		**500**	s

Electrical Specifications $V_{DDP} = V_{DDS} = 12V$, $T_A = -40°C$ to $+85°C$ unless otherwise noted. (Note 8) Typical values are at $T_A = +25°C$.
Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)

PARAMETER	CONDITIONS	MIN (Note 18)	TYP	MAX (Note 18)	UNIT
Soft-start Delay Duration Accuracy	Turn-on delay (precise mode) (Notes 11, 12)		±0.25		ms
	Turn-on delay (normal mode) (Note 13)		-0.25/+4		ms
	Turn-off delay (Note 13)		-0.25/+4		ms
Soft-start Ramp Duration Range	Set using SS pin or resistor	**2**		**20**	ms
	Set using I^2C/SMBus	**0**		**200**	ms
Soft-start Ramp Duration Accuracy			100		µs
Logic Input/Output Characteristics					
Logic Input Leakage Current	Digital pins	**-250**		**250**	nA
Logic input low, V_{IL}				**0.8**	V
Logic input OPEN (N/C)	Multi-mode logic pins		1.4		V
Logic Input High, V_{IH}		**2.0**			V
Logic Output Low, V_{OL}	$I_{OL} \leq 4mA$			**0.4**	V
Logic Output High, V_{OH}	$I_{OH} \geq -2mA$	**2.25**			V
Oscillator and Switching Characteristics					
Switch Node Current, I_{SW}	Peak (source or sink) (Note 14)			**9**	A
Switching Frequency Range		**200**		**1000**	kHz
Switching Frequency Set-point Accuracy	Predefined settings (Table 9)	**-5**		**5**	%
PWM Duty Cycle (Max)	Factory default (Note 15)			**95** (Note 16)	%
SYNC Pulse Width (Min)		**150**			ns
Input Clock Frequency Drift Tolerance	External clock source	**-13**		**13**	%
$r_{DS(ON)}$ of High Side N-channel FETs	$I_{SW} = 6A$, $V_{GS} = 6.5V$		60	**85**	mΩ
$r_{DS(ON)}$ of Low Side N-channel FETs	$I_{SW} = 6A$, $V_{GS} = 12V$		43	**65**	mΩ
Tracking					
VTRK Input Bias Current	VTRK = 5.5V		110	**200**	µA
VTRK Tracking Ramp Accuracy	100% Tracking, V_{OUT} - VTRK	**-100**		**100**	mV
VTRK Regulation Accuracy	100% Tracking, V_{OUT} - VTRK	**-1**		**1**	%
Fault Protection Characteristics					
UVLO Threshold Range	Configurable via I^2C/SMBus	**2.85**		**16**	V
UVLO Set-point Accuracy		**-150**		**150**	mV
UVLO Hysteresis	Factory default		3		%
	Configurable via I^2C/SMBus	**0**		**100**	%
UVLO Delay				**2.5**	µs
Power-good V_{OUT} Threshold	Factory default		90		% V_{OUT}
Power-good V_{OUT} Hysteresis	Factory default		5		%
Power-good Delay	Using pin-strap or resistor	**2**		**20**	ms
	Configurable via I^2C/SMBus	**0**		**500**	s

Electrical Specifications $V_{DDP} = V_{DDS} = 12V$, $T_A = -40°C$ to $+85°C$ unless otherwise noted. (Note 8) Typical values are at $T_A = +25°C$. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	CONDITIONS	MIN (Note 18)	TYP	MAX (Note 18)	UNIT
VSEN Undervoltage Threshold	Factory default		85		% V_{OUT}
	Configurable via I^2C/SMBus	**0**		**110**	% V_{OUT}
VSEN Overvoltage Threshold	Factory default		115		% V_{OUT}
	Configurable via I^2C/SMBus	**0**		**115**	% V_{OUT}
VSEN Undervoltage Hysteresis			5		% V_{OUT}
VSEN Undervoltage/Overvoltage Fault Response Time	Factory default		16		µs
	Configurable via I^2C/SMBus	**5**		**60**	µs
Peak Current Limit Threshold	Factory default			**9.0**	A
	Configurable via I^2C/SMBus	**0.2**		**9.0**	A
Current Limit Set-point Accuracy			±10		% FS (Note 10)
Current Limit Protection Delay	Factory default		5		t_{SW} (Note 17)
	Configurable via I^2C/SMBus	**1**		**32**	t_{SW} (Note 17)
Thermal Protection Threshold (Junction Temperature)	Factory default		125		°C
	Configurable via I^2C/SMBus	**-40**		**125**	°C
Thermal Protection Hysteresis			15		°C

NOTES:

8. Refer to Safe Operating Area in Figure 8 and thermal design guidelines in AN2010.
9. Does not include margin limits.
10. Percentage of Full Scale (FS) with temperature compensation applied.
11. The device requires a delay period following an enable signal and prior to ramping its output. Precise timing mode limits this delay period to approx 2ms, where in normal mode it may vary up to 4ms.
12. Precise ramp timing mode is only valid when using EN pin to enable the device rather than PMBus enable. Precise ramp timing mode is automatically disabled for a self-enabled device (EN pin tied high).
13. The devices may require up to a 4ms delay following the assertion of the enable signal (normal mode) or following the de-assertion of the enable signal. Precise mode requires Re-Enable delay = t_{OFF}+ t_{FALL}+10µs.
14. Switch node current should not exceed I_{RMS} of 6A.
15. Factory default is the initial value in firmware. The value can be changed via PMBus commands.
16. Maximum duty cycle is limited by the equation MAX_DUTY(%) = $[1 - (150\times10^{-9} \times f_{SW})] \times 100$ and not to exceed 95%.
17. $t_{SW} = 1/f_{SW}$, where f_{SW} is the switching frequency.
18. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

For some applications, ZL2106 operating conditions (input voltage, output voltage, switching frequency, temperature) may require de-rating to remain within the Safe Operating Area (SOA). $V_{IN} = V_{DDP} = V_{DDS}$, $T_J = +125°C$

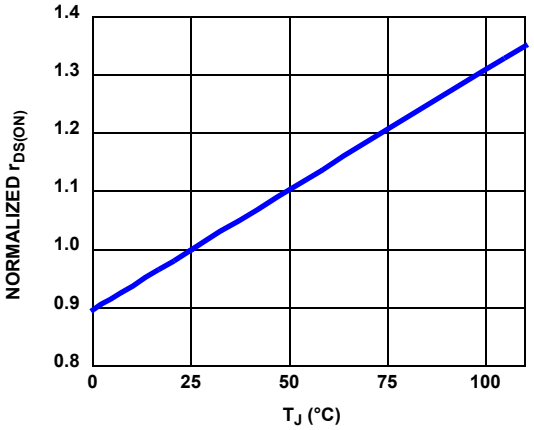


FIGURE 5. LOW-SIDE $r_{DS(ON)}$ vs T_J NORMALIZED FOR $T_J = +25°C$ ($V_{DDS} = 12V$, $I_{DRAIN} = 0.3A$)

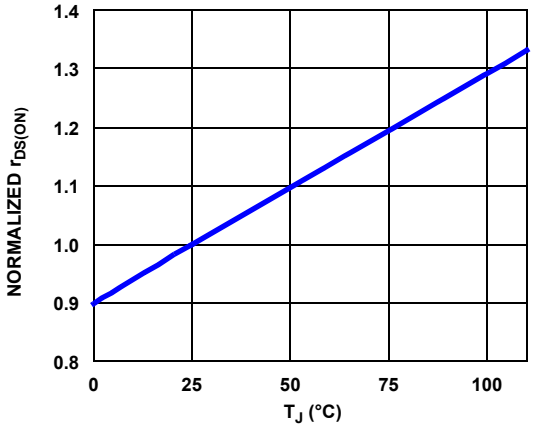


FIGURE 6. HIGH-SIDE $r_{DS(ON)}$ vs T_J NORMALIZED FOR $T_J = +25°C$ ($V_{DDS} = 12V$, BST – SW = 6.5V, $I_{DRAIN} = 0.3A$)

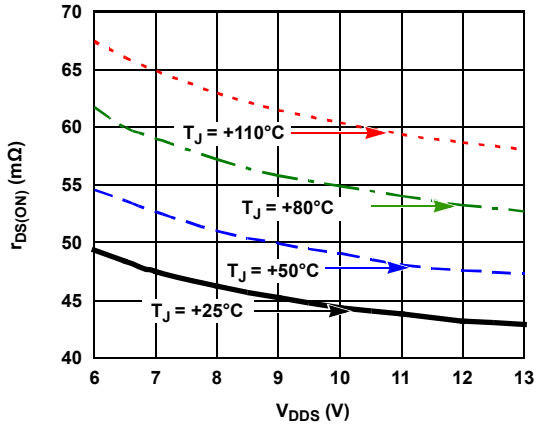


FIGURE 7. LOW-SIDE $r_{DS(ON)}$ vs V_{DDS} WITH T_J

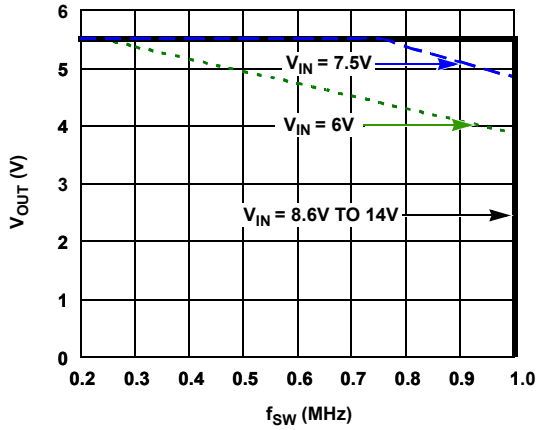


FIGURE 8. SAFE OPERATING AREA, $T_J \leq +125°C$

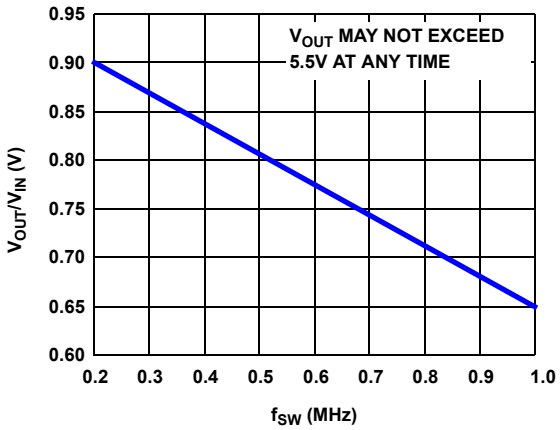


FIGURE 9. MAXIMUM CONVERSION RATIO, $T_J \leq +125°C$

ZL2106 Overview

Digital-DC Architecture

The ZL2106 is an innovative mixed-signal power conversion and power management IC based on Zilker Labs patented Digital-DC technology that provides an integrated, high performance step-down converter for point of load applications. The ZL2106 integrates all necessary PWM control circuitry as well as low $r_{DS(ON)}$ synchronous power MOSFETs to provide an extremely small solution for supplying load currents up to 6A.

Its unique PWM loop utilizes an ideal mix of analog and digital blocks to enable precise control of the entire power conversion process with no software required, resulting in a very flexible device that is also very easy to use. An extensive set of power management functions are fully integrated and can be configured using simple pin connections. The user configuration can be saved in an internal non-volatile memory (NVM). Additionally, all functions can be configured and monitored via the SMBus hardware interface using standard PMBus commands, allowing ultimate flexibility.

Once enabled, the ZL2106 is immediately ready to regulate power and perform power management tasks with no programming required. Advanced configuration options and real-time configuration changes are available via the I^2C/SMBus interface if desired and continuous monitoring of multiple operating parameters is possible with minimal interaction from a host controller. Integrated sub-regulation circuitry enables single supply operation from any external supply between 4.5V and 14V with no secondary bias supplies needed. The ZL2106 can also be configured to operate from a 3.3V or 5V standby supply when the main power rail is not present, allowing the user to configure and/or read diagnostic information from the device when the main power has been interrupted or is disabled.

The ZL2106 can be configured by simply connecting its pins according to the tables provided in the following sections. Additionally, a comprehensive set of application notes are available to help simplify the design process. An evaluation board is also available to help the user become familiar with the device. This board can be evaluated as a standalone platform using pin configuration settings. A Windows™-based GUI is also provided to enable full configuration and monitoring capability via the I^2C/SMBus interface using an available computer and the included USB cable.

Power Conversion Overview

The ZL2106 operates as a voltage-mode, synchronous buck converter with a selectable constant frequency pulse width modulator (PWM) control scheme. The ZL2106 integrates dual low $r_{DS(ON)}$ synchronous MOSFETs to minimize the circuit footprint.

Figure 10 illustrates the basic synchronous buck converter topology showing the primary power train components. This converter is also called a step-down converter, as the output voltage must always be lower than the input voltage.

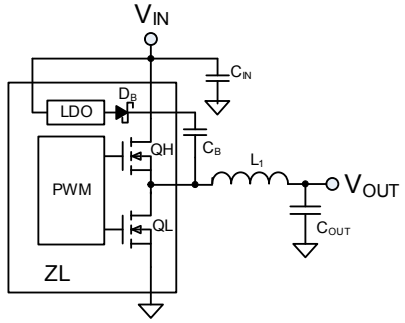


FIGURE 10. SYNCHRONOUS BUCK CONVERTER

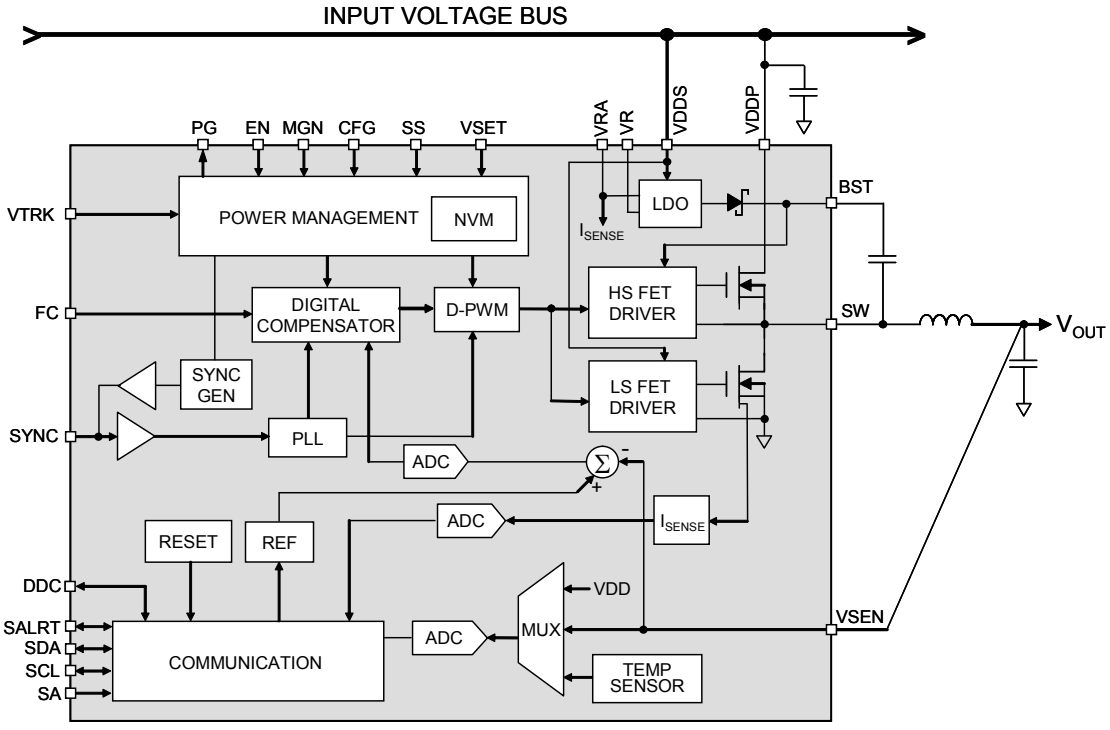


FIGURE 11. ZL2106 BLOCK DIAGRAM

The ZL2106 integrates two N-channel power MOSFETs; QH is the top control MOSFET and QL is the bottom synchronous MOSFET. The amount of time that QH is on as a fraction of the total switching period is known as the duty cycle *D*, which is described by Equation 1:

$$D \approx \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 1)}$$

During time D, QH is on and $V_{IN} - V_{OUT}$ is applied across the inductor. The output current ramps up as shown in Figure 12.

When QH turns off (time 1-D), the current flowing in the inductor must continue to flow from the ground up through QL, during which the current ramps down. Since the output capacitor C_{OUT} exhibits low impedance at the switching frequency, the AC component of the inductor current is filtered from the output voltage so the load sees nearly a DC voltage.

The maximum conversion ratio is shown in Figure 9. Typically, buck converters specify a maximum duty cycle that effectively limits the maximum output voltage that can be realized for a given input voltage and switching frequency. This duty cycle limit ensures that the low-side MOSFET is allowed to turn on for a minimum amount of time during each switching cycle, which enables the bootstrap capacitor to be charged up and provide adequate gate drive voltage for the high-side MOSFET.

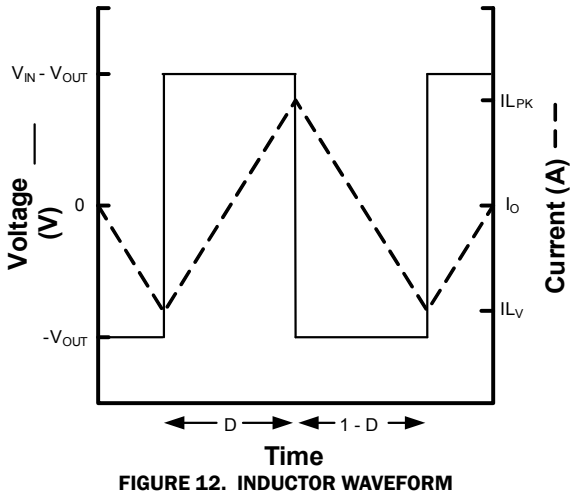


FIGURE 12. INDUCTOR WAVEFORM

In general, the size of components L_1 and C_{OUT} as well as the overall efficiency of the circuit are inversely proportional to the switching frequency, f_{SW}. Therefore, the highest efficiency circuit may be realized by switching the MOSFETs at the lowest possible frequency; however, this will result in the largest component size. Conversely, the smallest possible footprint may be realized by switching at the fastest possible frequency but this gives a somewhat lower efficiency. Each user should determine the optimal combination of size and efficiency when determining the switching frequency for each application.

The block diagram for the ZL2106 is illustrated in Figure 11. In this circuit, the target output voltage is regulated by connecting the VSEN pin directly to the output regulation point. The VSEN signal is then compared to an internal reference voltage that had been set to the desired output voltage level by the user. The error signal derived from this comparison is converted to a digital value with an analog to digital (A/D) converter. The digital signal is also applied to an adjustable digital compensation filter and the compensated signal is used to derive the appropriate PWM duty cycle for driving the internal MOSFETs in a way that produces the desired output.

Power Management Overview

The ZL2106 incorporates a wide range of configurable power management features that are simple to implement without additional components. Also, the ZL2106 includes circuit protection features that continuously safeguard the device and load from damage due to unexpected system faults. The ZL2106 can continuously monitor input voltage, output voltage/current and internal temperature. A Power-good output signal is also included to enable power-on reset functionality for an external processor.

All power management functions can be configured using either pin configuration techniques (see Figure 13) or via the I^2C/SMBus interface. Monitoring parameters can also be pre-configured to provide alerts for specific conditions. See Application Note AN2033 for more details on SMBus monitoring.

Multi-mode Pins

In order to simplify circuit design, the ZL2106 incorporates patented multi-mode pins that allow the user to easily configure many aspects of the device without programming. Most power management features can be configured using these pins. The multi-mode pins can respond to four different connections, as shown in Table 1. These pins are sampled when power is applied or by issuing a PMBus Restore command (See Application Note AN2033).

PIN-STRAP SETTINGS

This is the simplest method, as no additional components are required. Using this method, each pin can take on one of three possible states: LOW, OPEN, or HIGH. These pins can be connected to the V2P5 pin for logic HIGH settings as this pin provides a regulated voltage higher than 2V. Using a single pin one of three settings can be selected.

TABLE 1. MULTI-MODE PIN CONFIGURATION

PIN TIED TO	VALUE
LOW (Logic LOW)	< 0.8VDC
OPEN (N/C)	No connection
HIGH (Logic HIGH)	> 2.0VDC
Resistor to SGND	Set by resistor value

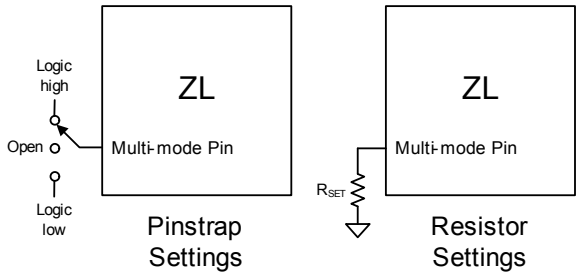


FIGURE 13. PIN-STRAP AND RESISTOR SETTING EXAMPLES

RESISTOR SETTINGS

This method allows a greater range of adjustability when connecting a finite value resistor (in a specified range) between the multi-mode pin and SGND.

Standard 1% resistor values are used, and only every fourth E96 resistor value is used so the device can reliably recognize the value of resistance connected to the pin while eliminating the error associated with the resistor accuracy. Up to 31 unique selections are available using a single resistor.

I²C/SMBUS METHOD

ZL2106 functions can be configured via the I²C/SMBus interface using standard PMBus commands. Additionally, any value that has been configured using the pin-strap or resistor setting methods can also be re-configured and/or verified via the I²C/SMBus. See Application Note AN2033 for more details.

The SMBus device address and VOUT_MAX are the only parameters that must be set by external pins. All other device parameters can be set via the I²C/SMBus. The device address is set using the SA pin. VOUT_MAX is determined as 10% greater than the voltage set by the VSET pin.

Resistor pin-straps are recommended to be used for all available device parameters to allow a safe initial power-up before configuration is stored via the I²C/SMBus. For example, this can be accomplished by pin-strapping the undervoltage lockout threshold (using SS pin) to a value greater than the expected input voltage, thus preventing the device from enabling prior to loading a configuration file.

Power Conversion Functional Description

Internal Bias Regulators and Input Supply Connections

The ZL2106 employs three internal low dropout (LDO) regulators to supply bias voltages for internal circuitry, allowing it to operate from a single input supply. The internal bias regulators are as follows:

- VR: The VR LDO provides a regulated 7V bias supply for the high-side MOSFET driver circuit. It is powered from the VDDS pin and supplies bias current internally. A 4.7µF filter capacitor is required at the VR pin. The VDDS pin directly supplies the low-side MOSFET driver circuit.
- VRA: The VRA LDO provides a regulated 5V bias supply for the current sense circuit and other analog circuitry. It is powered from the VDDS pin and supplies bias current internally. A 4.7µF filter capacitor is required at the VRA pin.

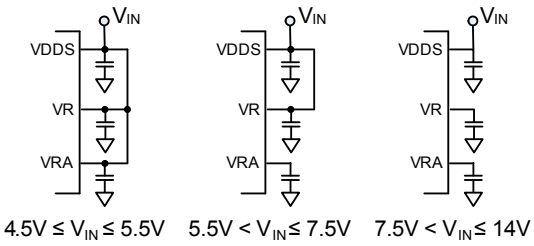


FIGURE 14. INPUT SUPPLY CONNECTIONS

- V2P5: The V2P5 LDO provides a regulated 2.5V bias supply for the main controller circuitry. It is powered from the VRA LDO and supplies bias current internally. A 10µF filter capacitor is required at the V2P5 pin.

When the input supply (VDDS) is higher than 7.5V, the VR and VRA pins should not be connected to any other pins. These pins should only have a filter capacitor attached. Due to the dropout voltage associated with the VR and VRA bias regulators, the VDDS pin must be connected to these pins for designs operating from a supply below 7.5V. Figure 14 illustrates the required connections for all cases.

Note: The internal bias regulators, VR and VRA, are not designed to be outputs for powering other circuitry. Do not attach external loads to any of these pins. Only the multi-mode pins may be connected to the V2P5 pin for logic HIGH settings.

High-side Driver Boost Circuit

The gate drive voltage for the high-side MOSFET driver is generated by a floating bootstrap capacitor, C_B (see Figure 10). When the lower MOSFET (QL) is turned on, the SW node is pulled to ground and the capacitor is charged from the internal VR bias regulator through diode D_B. When QL turns off and the upper MOSFET (QH) turns on, the SW node is pulled up to VDDP and the voltage on the bootstrap capacitor is boosted approximately 6.5V above VDDP to provide the necessary voltage to power the high-side driver. An internal Schottky diode is used with C_B to help maximize the high-side drive supply voltage.

Output Voltage Selection

The output voltage may be set to any voltage between 0.6V and 5.0V provided that the input voltage is higher than the desired output voltage by an amount sufficient to prevent the device from exceeding its maximum duty cycle specification. Using the pin-strap method, V_{OUT} can be set to one of three standard voltages as shown in Table 2.

TABLE 2. PIN-STRAP OUTPUT VOLTAGE SETTINGS

VSET	V_{OUT} (V)
LOW	1.2
OPEN	1.5
HIGH	3.3

TABLE 3. ZL2106 START-UP SEQUENCE

STEP #	STEP NAME	DESCRIPTION	TIME DURATION
1	Power Applied	Input voltage is applied to the ZL2106's VDD pins (VDDP and VDDS).	Depends on input supply ramp time
2	Internal Memory Check	The device will check for values stored in its internal memory. This step is also performed after a Restore command.	Approx 5ms to 10ms (device will ignore an enable signal or PMBus traffic during this period)
3	Multi-mode Pin Check	The device loads values configured by the multi-mode pins.	
4	Device Ready	The device is ready to accept an enable signal.	-
5	Pre-ramp Delay	The device requires approximately 2ms following an enable signal and prior to ramping its output. Additional pre-ramp delay may be configured using the SS pin.	Approximately 2ms

TABLE 4. RESISTORS FOR SETTING OUTPUT VOLTAGE

R_{SET} (kΩ)	V_{OUT} (V)
10	0.6
11	0.7
12.1	0.75
13.3	0.8
14.7	0.9
16.2	1.0
17.8	1.1
19.6	1.2
21.5	1.25
23.7	1.3
26.1	1.4
28.7	1.5
31.6	1.6
34.8	1.7
38.3	1.8
42.2	1.9
46.4	2.0
51.1	2.1
56.2	2.2
61.9	2.3
68.1	2.4
75	2.5
82.5	2.6
90.9	2.7
100	2.8
110	2.9
121	3.0
133	3.1
147	3.2
162	3.3
178	5.0

The resistor setting method can be used to set the output voltage to levels not available in Table 2. To set V_{OUT} using resistors, use Table 4 to select the resistor that corresponds to the desired voltage.

The output voltage may also be set to any value between 0.6V and 5.0V using the I^2C interface. See Application Note AN2033 for details.

Start-up Procedure

The ZL2106 follows a specific internal start-up procedure after power is applied to the VDD pins (VDDP and VDDS). Table 3 describes the start-up sequence.

If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting the EN pin. The device requires approximately 5ms to 10ms to check for specific values stored in its internal memory. If the user has stored values in memory, those values will be loaded. The device will then check the status of all multi-mode pins and load the values associated with the pin settings.

Once this process is completed, the device is ready to accept commands via the I^2C/SMBus interface and the device is ready to be enabled. Once enabled, the device requires approximately 2ms before its output voltage may be allowed to start its ramp-up process. If a soft-start delay period less than 2ms has been configured (using PMBus commands), the device will default to a 2ms delay period. If a delay period greater than 2ms is configured, the device will wait for the configured delay period prior to starting to ramp its output.

After the delay period has expired, the output will begin to ramp towards its target voltage according to the pre-configured soft-start ramp time that has been set using the SS pin. It should be noted that if the EN pin is tied to VDDP or VDDS, the device will still require approximately 5ms to 10ms before the output can begin its ramp-up as described in Table 3.

Soft-start Delay and Ramp Times

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features may be used as part of an overall inrush current management strategy or to control how fast a load IC is turned on. The ZL2106 gives the system designer several options for precisely and independently controlling both the delay and ramp time periods.

The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires. The soft-start delay period is set using the SS pin. Precise ramp delay timing mode reduces the delay time variations and is available when the appropriate bit in the MISC_CONFIG register had been set. Please refer to Application Note AN2033 for details.

The soft-start ramp timer enables a precisely controlled ramp to the nominal V_{OUT} value that begins once the delay period has expired. The ramp-up is guaranteed monotonic and its slope may be precisely set using the SS pin. Using the pin-strap method, the soft-start delay and ramp times can be set to one of three standard values according to Table 5.

TABLE 5. SOFT-START DELAY AND RAMP SETTINGS

SS PIN SETTING	DELAY AND RAMP TIME (ms)	UVLO
LOW	2	7.5V
OPEN	5	
HIGH	10	

If the desired soft-start delay and ramp times are not one of the values listed in Table 5, the times can be set to a custom value by connecting a resistor from the SS pin to SGND using the appropriate resistor value from Table 6. The value of this resistor is measured upon start-up or Restore and will not change if the resistor is varied after power has been applied to the ZL2106 (see Figure 15).

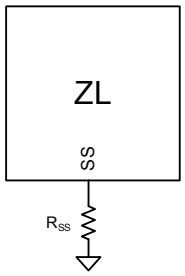


FIGURE 15. SS PIN RESISTOR CONNECTIONS

The soft-start delay and ramp times can also be set to custom values via the I^2C/SMBus interface. When the SS delay time is set to 0ms, the device will begin its ramp-up after the internal circuitry has initialized (~2ms). When the soft-start ramp period is set to 0ms, the output will ramp up as quickly as the output load capacitance and loop settings will allow. It is generally recommended to set the soft-start ramp to a value greater than 500µs to prevent inadvertent fault conditions due to excessive inrush current.

TABLE 6. DELAY AND RAMP CONFIGURATION

R_{SS} (kΩ)	DELAY TIME (ms)	RAMP TIME (ms)	UVLO (V)
10	5	5	4.5
11	10		
12.1	20		
13.3	5	10	
14.7	10		
16.2	20		
17.8	5	2	5.5
19.6	10		
21.5	20		
23.7	5	5	
26.1	10		
28.7	20		
31.6	5	10	
34.8	10		
38.3	20		
42.2	5	20	
46.4	10		
51.1	20		
56.2	5	2	7.5
61.9	10		
68.1	20		
75	5	5	
82.5	10		
90.9	20		
100	5	10	
110	10		
121	20		
133	5	20	
147	10		
162	20		

Power-good (PG)

The ZL2106 provides a Power-good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin will assert if the output is within +15%/-10% of the target voltage. These limits may be changed via the I^2C/SMBus interface. See Application Note AN2033 for details.

A PG delay period is the time from when all conditions for asserting PG are met and when the PG pin is actually asserted. This feature is commonly used instead of an external reset controller to signal the power supply is at its target voltage prior to enabling any powered circuitry. By default, the ZL2106 PG delay is set to 1ms and may be changed using the I^2C/SMBus interface as described in AN2033.

Switching Frequency and PLL

The ZL2106 incorporates an internal phase-locked loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock source for other Zilker Labs devices.

The SYNC pin is a unique pin that can perform multiple functions depending on how it is configured. The CFG pin is used to select the operating mode of the SYNC pin as shown in Table 4. Figure 16 illustrates the typical connections for each mode.

TABLE 7. SYNC PIN FUNCTION SELECTION

CFG PIN	SYNC PIN FUNCTION
LOW	SYNC is configured as an input
OPEN	Auto detect mode
HIGH	SYNC is configured as an output f_{SW} = 400kHz

CONFIGURATION A: SYNC OUTPUT

When the SYNC pin is configured as an output (CFG pin is tied HIGH), the device will run from its internal oscillator and will drive the resulting internal oscillator signal (preset to 400kHz) onto the SYNC pin so other devices can be synchronized to it. The SYNC pin will not be checked for an incoming clock signal while in this mode.

CONFIGURATION B: SYNC INPUT

When the SYNC pin is configured as an input (CFG pin is tied LOW), the device will automatically check for an external clock signal on the SYNC pin each time the EN pin is asserted. The internal oscillator will then synchronize with the rising edge of the external clock. The incoming clock signal must be in the range of 200kHz to 1MHz with a minimum duty cycle and must be stable when the EN pin is asserted. The external clock signal must also exhibit the necessary performance requirements (see the "Electrical Specifications" table beginning on page 6).

In the event of a loss of the external clock signal, the output voltage may show transient over/undershoot. If this happens, the ZL2106 will automatically switch to its internal oscillator and switch at a frequency close to the previous incoming frequency.

CONFIGURATION C: SYNC AUTO DETECT

When the SYNC pin is configured in auto detect mode (CFG pin is left OPEN), the device will automatically check for a clock signal on the SYNC pin after enable is asserted. If a valid clock signal is present, the ZL2106's oscillator will then synchronize with the rising edge of the external clock (refer to SYNC INPUT description).

If no incoming clock signal is present, the ZL2106 will configure the switching frequency according to the state of the SYNC pin as listed in Table 8. In this mode, the ZL2106 will only read the SYNC pin connection during the start-up sequence. Changes to the SYNC pin connection will not affect f_{SW} until the power (VDDS) is cycled off and on again.

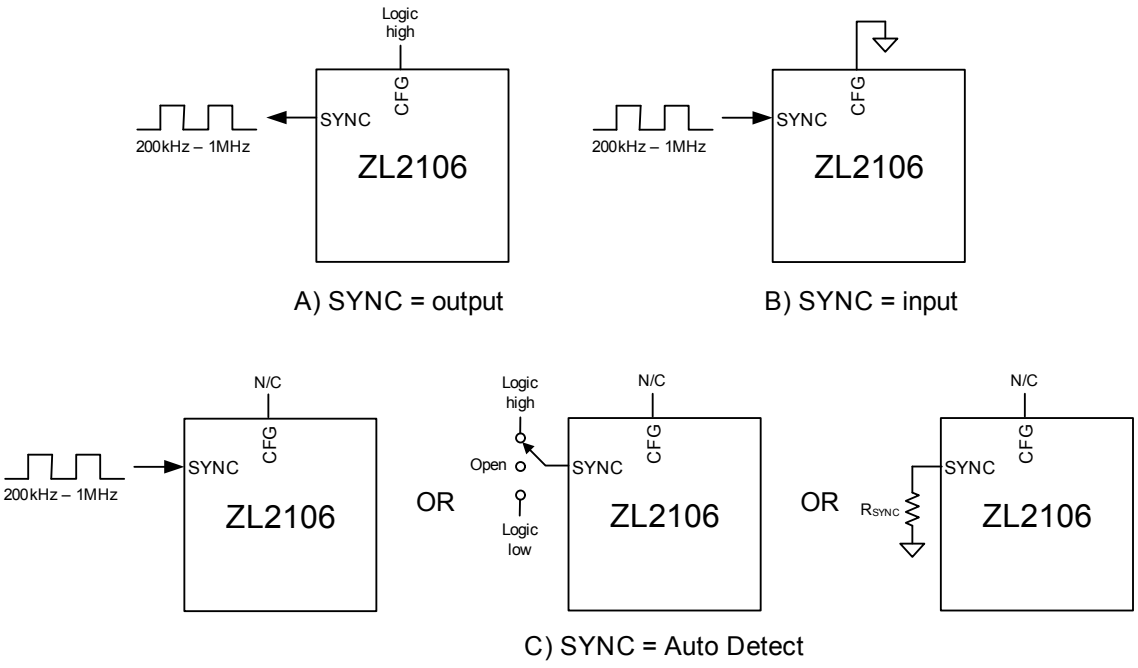


FIGURE 16. SYNC PIN CONFIGURATIONS

TABLE 8. SWITCHING FREQUENCY SELECTION

SYNC PIN	FREQUENCY
LOW	200kHz
OPEN	400kHz
HIGH	1MHz
Resistor	See Table 9

If the user wishes to run the ZL2106 at a frequency not listed in Table 8, the switching frequency can be set using an external resistor, R_{SYNC}, connected between SYNC and SGND using Table 9.

TABLE 9. R_{SYNC} RESISTOR VALUES

R_{SYNC} (kΩ)	F_{SW} (kHz)
10	200
11	222
12.1	242
13.3	267
14.7	296
16.2	320
17.8	364
19.6	400
21.5	421
23.7	471
26.1	533
28.7	571
31.6	615
34.8	667
38.3	727
42.2	889
46.4	1000

The switching frequency can also be set to any value between 200kHz and 1MHz using the I^2C/SMBus interface. The available frequencies are defined by f_{SW} = 8MHz/N, where whole number N is $8 \leq N \leq 40$. See Application Note AN2033 for details.

If a value other than f_{SW} = 8MHz/N is entered using a PMBus command, the internal circuitry will select the valid switching frequency value that is closest to the entered value. For example, if 810kHz is entered, the device will select 800kHz (N=10).

Note: The switching frequency read back using the appropriate PMBus command will differ slightly from the selected value in Table 9. The difference is due to hardware quantization.

When multiple Zilker Labs devices are used together, connecting the SYNC pins together will force all devices to synchronize with each other. The CFG pin of one device must set its SYNC pin as an output and the remaining devices must have their SYNC pins set as an input or as auto detect.

Note: Precise ramp timing mode must be disabled to use SYNC clock auto detect.

Component Selection

The ZL2106 is a synchronous buck converter with integrated MOSFETs that uses an external inductor and capacitors to perform the power conversion process. The proper selection of the external components is critical for optimized performance.

To select the appropriate external components for the desired performance goals, the power supply requirements listed in Table 10 must be defined.

TABLE 10. POWER SUPPLY REQUIREMENTS

PARAMETER	RANGE	EXAMPLE VALUE
Input Voltage (V_{IN})	4.5V to 14.0V	12V
Output Voltage (V_{OUT})	0.6V to 5.0V	3.3V
Output Current (I_{OUT})	0A to 6A	4A
Output Voltage Ripple (V_{orip})	< 3% of V_{OUT}	±1% of V_{OUT}
Output Load Step (I_{ostep})	< I_o	±25% of I_o
Output Load Step Rate	-	2.5A/µs
Output Deviation Due to Load Step	-	±3% of V_{OUT}
Maximum PCB Temp.	+120°C	+85°C
Desired Efficiency	-	85%
Other Considerations	-	Optimize for small size

DESIGN GOAL TRADE-OFFS

The design of the buck power stage requires several compromises among size, efficiency and cost. The inductor core loss increases with frequency, so there is a trade-off between a small output filter made possible by a higher switching frequency and getting better power supply efficiency. Size can be decreased by increasing the switching frequency at the expense of efficiency. Cost can be minimized by using through-hole inductors and capacitors; however these components are physically large.

To start the design, select a frequency based on Table 11. This frequency is a starting point and may be adjusted as the design progresses.

TABLE 11. CIRCUIT DESIGN CONSIDERATIONS

FREQUENCY RANGE	EFFICIENCY	CIRCUIT SIZE
200kHz to 400kHz	Highest	Larger
400kHz to 800kHz	Moderate	Smaller
800kHz to 1MHz	Lower	Smallest

INDUCTOR SELECTION

The output inductor selection process must include several trade-offs. A high inductance value will result in a low ripple current (I_{opp}), which will reduce output capacitance and produce a low output ripple voltage, but may also compromise output transient load performance. Therefore, a balance must be struck

between output ripple and optimal load transient performance. A good starting point is to select the output inductor ripple equal to the expected load transient step magnitude (I_{ostep}):

$$I_{opp} = I_{ostep} \quad \text{(EQ. 2)}$$

Now the output inductance can be calculated using Equation 3, where V_{INM} is the maximum input voltage:

$$L_{OUT} = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{INM}}\right)}{fsw \times I_{opp}} \quad \text{(EQ. 3)}$$

The average inductor current is equal to the maximum output current. The peak inductor current (I_{Lpk}) is calculated using Equation 4 where I_{OUT} is the maximum output current:

$$I_{Lpk} = I_{OUT} + \frac{I_{opp}}{2} \quad \text{(EQ. 4)}$$

Select an inductor rated for the average DC current with a peak current rating above the peak current computed in Equation 4.

In overcurrent or short-circuit conditions, the inductor may have currents greater than 2X the normal maximum rated output current. It is desirable to use an inductor that still provides some inductance to protect the load and the internal MOSFETs from damaging currents in this situation.

Once an inductor is selected, the DCR and core losses in the inductor are calculated. Use the DCR specified in the inductor manufacturer's data sheet.

$$P_{LDCR} = DCR \times I_{Lrms}^{2} \quad \text{(EQ. 5)}$$

I_{Lrms} is given by Equation 6:

$$I_{Lrms} = \sqrt{I_{OUT}^{2} + \frac{(I_{opp})^2}{12}} \quad \text{(EQ. 6)}$$

where I_{OUT} is the maximum output current. Next, calculate the core loss of the selected inductor. Since this calculation is specific to each inductor and manufacturer, refer to the chosen inductor data sheet. Add the core loss and the DCR loss and compare the total loss to the maximum power dissipation recommendation in the inductor data sheet.

OUTPUT CAPACITOR SELECTION

Several trade-offs must also be considered when selecting an output capacitor. Low ESR values are needed to have a small output deviation during transient load steps (V_{osag}) and low output voltage ripple (V_{orip}). However, capacitors with low ESR, such as semi-stable (X5R and X7R) dielectric ceramic capacitors, also have relatively low capacitance values. Many designs can use a combination of high capacitance devices and low ESR devices in parallel.

For high ripple currents, a low capacitance value can cause a significant amount of output voltage ripple. Likewise, in high transient load steps, a relatively large amount of capacitance is needed to minimize the output voltage deviation while the inductor current ramps up or down to the new steady state output current value.

As a starting point, apportion one-half of the output ripple voltage to the capacitor ESR and the other half to capacitance, as shown in Equations 7 and 8:

$$C_{OUT} = \frac{I_{opp}}{8 \times f_{sw} \times \frac{V_{orip}}{2}} \quad \text{(EQ. 7)}$$

$$ESR = \frac{V_{orip}}{2 \times I_{opp}} \quad \text{(EQ. 8)}$$

Use these values to make an initial capacitor selection, using a single capacitor or several capacitors in parallel.

After a capacitor has been selected, the resulting output voltage ripple can be calculated using Equation 9:

$$V_{orip} = I_{opp} \times ESR + \frac{I_{opp}}{8 \times f_{sw} \times C_{OUT}} \quad \text{(EQ. 9)}$$

Because each part of this equation was made to be less than or equal to half of the allowed output ripple voltage, the V_{orip} should be less than the desired maximum output ripple.

INPUT CAPACITOR

It is highly recommended that dedicated input capacitors be used in any point-of-load design, even when the supply is powered from a heavily filtered 5V or 12V "bulk" supply from an off-line power supply. This is because of the high RMS ripple current that is drawn by the buck converter topology. This ripple (I_{CINrms}) can be determined from Equation 10:

$$I_{CINrms} = I_{OUT} \times \sqrt{D \times (1 - D)} \quad \text{(EQ. 10)}$$

Without capacitive filtering near the power supply circuit, this current would flow through the supply bus and return planes, coupling noise into other system circuitry. The input capacitors should be rated at 1.2X the ripple current calculated in Equation 10 to avoid overheating of the capacitors due to the high ripple current, which can cause premature failure. Ceramic capacitors with X7R or X5R dielectric with low ESR and 1.1X the maximum expected input voltage are recommended.

BOOTSTRAP CAPACITOR SELECTION

The high-side driver boost circuit utilizes an internal Schottky diode (D_B) and an external bootstrap capacitor (C_B) to supply sufficient gate drive for the high-side MOSFET driver. C_B should be a 47nF ceramic type rated for at least 10V.

C_{V2P5} SELECTION

This capacitor is used to both stabilize and provide noise filtering for the 2.5V internal power supply. It should be between 4.7µF and 10µF, should use a semi-stable X5R or X7R dielectric ceramic with a low ESR (less than 10mΩ) and should have a rating of 4V or more.

C_{VR} SELECTION

This capacitor is used to both stabilize and provide noise filtering for the 7V reference supply. It should be between 4.7µF and 10µF, should use a semi-stable X5R or X7R dielectric ceramic capacitor with a low ESR (less than 10mΩ) and should have a rating of 10V or more. Because the current for the bootstrap supply is drawn from this capacitor, C_{VR} should be sized at least

10X the value of C_B so that a discharged C_B does not cause the voltage on it to droop excessively during a C_B recharge pulse.

C_{VRA} SELECTION

This capacitor is used to both stabilize and provide noise filtering for the analog 5V reference supply. It should be between 2.2µF and 10µF, should use a semi-stable X5R or X7R dielectric ceramic capacitor with a low ESR (less than 10mΩ) and should have a rating of 6.3V or more.

THERMAL CONSIDERATIONS

In typical applications, the ZL2106's high efficiency will limit the internal power dissipation inside the package. However, in applications that require a high ambient operating temperature the user must perform some thermal analysis to ensure that the ZL2106's maximum junction temperature is not exceeded.

The ZL2106 has a maximum junction temperature limit of +125°C, and the internal over-temperature limiting circuitry will force the device to shut down if its junction temperature exceeds this threshold. In order to calculate the maximum junction temperature, the user must first calculate the power dissipated inside the IC (P_Q) as expressed in Equation 11:

$$P_Q = \left(I_{LOAD}{}^2\right)\left[\left(R_{DS(ON)QH}\right)(D) + \left(R_{DS(ON)QL}\right)(1-D)\right] \quad \text{(EQ. 11)}$$

The maximum operating junction temperature can then be calculated using Equation 12:

$$T_{j\max} = T_{PCB} + \left(P_Q \times \theta_{JC}\right) \quad \text{(EQ. 12)}$$

Where T_{PCB} is the expected maximum printed circuit board temperature and θ_{JC} is the junction-to-case thermal resistance for the ZL2106 package.

Current Sensing and Current Limit Threshold Selection

The ZL2106 incorporates a patented "lossless" current sensing method across the internal low-side MOSFET that is independent of $r_{DS(ON)}$ variations, including temperature. The default value for the gain, which does not represent a $r_{DS(ON)}$ value, and the offset of the internal current sensing circuit can be modified by the IOUT_CAL_GAIN and IOUT_CAL_OFFSET commands.

The design should include a current limiting mechanism to protect the power supply from damage and prevent excessive current from being drawn from the input supply in the event that the output is shorted to ground or an overload condition is imposed on the output. Current limiting is accomplished by sensing the current through the circuit during a portion of the duty cycle. The current limit threshold is set to 9A by default. The current limit threshold can set to a custom value via the I^2C/SMBus interface. Please refer to Application Note AN2033 for further details.

Additionally, the ZL2106 gives the power supply designer several choices for the fault response during over or under current conditions. The user can select the number of violations allowed before declaring a fault, a blanking time and the action taken when a fault is detected. The blanking time represents the time when no current measurement is taken. This is to avoid taking a reading just after a current load step (less accurate due to potential ringing). Please refer to Application note AN2033 for further details.

Loop Compensation

The ZL2106 operates as a voltage-mode synchronous buck controller with a fixed frequency PWM scheme. Although the ZL2106 uses a digital control loop, it operates much like a traditional analog PWM controller. Figure 17 is a simplified block diagram of the ZL2106 control loop, which differs from an analog control loop only by the constants in the PWM and compensation blocks. As in the analog controller case, the compensation block compares the output voltage to the desired voltage reference and compensation zeroes are added to keep the loop stable. The resulting integrated error signal is used to drive the PWM logic, converting the error signal to a duty cycle to drive the internal MOSFETs.

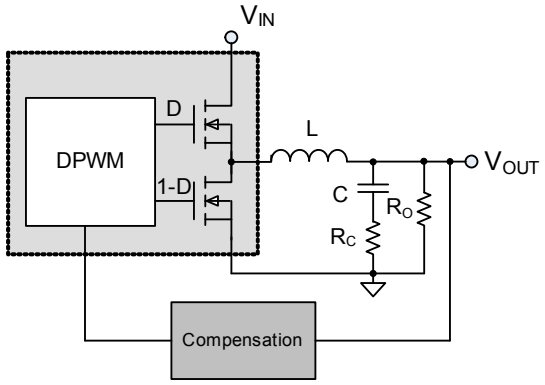


FIGURE 17. CONTROL LOOP BLOCK DIAGRAM

TABLE 12. RESISTOR SETTING FOR LOOP COMPENSATION

$G_{(dB)}$	Q	fsw/fn	FC (k)
24	0.150	115.000	Open or 11
27	0.150	115.000	Low or 10
27	0.150	69.147	13.3
27	0.150	41.577	14.7
27	0.300	115.000	16.2
27	0.300	69.147	17.8
27	0.300	41.577	19.6
27	0.300	25.000	21.5
27	0.600	69.147	23.7
27	0.600	41.577	26.1
27	0.600	25.000	28.7
30	0.150	115.000	High or 12.1
30	0.150	69.147	31.6
30	0.150	41.577	34.8
30	0.300	115.000	38.3
30	0.300	69.147	42.2
30	0.300	41.577	46.4
30	0.300	25.000	51.1
30	0.600	69.147	56.2
30	0.600	41.577	61.9
30	0.600	25.000	68.1
33	0.150	115.000	75.0

TABLE 12. RESISTOR SETTING FOR LOOP COMPENSATION (Continued)

$G_{(dB)}$	Q	fsw/fn	FC (k)
33	0.150	69.147	82.5
33	0.150	41.577	90.9
33	0.300	115.000	100.0
33	0.300	69.147	110.0
33	0.300	41.577	121.0
33	0.300	25.000	133.0
33	0.600	69.147	147.0
33	0.600	41.577	162.0
33	0.600	25.000	178.0

In the ZL2106, the compensation zeros are set by configuring the FC pin or via the I²C/SMBus interface once the user has calculated the required settings. This method eliminates the inaccuracies due to the component tolerances associated with using external resistors and capacitors required with traditional analog controllers.

The loop compensation coefficients can also be set via the I²C/SMBus interface. Please refer to Application Note AN2033 for further details. Also refer to Application Note AN2035 for further technical details on setting loop compensation.

Driver Dead-time Control

The ZL2106 utilizes a predetermined fixed dead-time applied between the gate drive signals for the top and bottom MOSFETs.

In a synchronous buck converter, the MOSFET drive circuitry must be operated such that the top and bottom MOSFETs are never in the conducting state at the same time. This is because potentially damaging currents flow in the circuit if both MOSFETs are on simultaneously for periods of time exceeding a few nanoseconds. Conversely, long periods of time in which both MOSFETs are off reduces overall circuit efficiency by allowing current to flow in their parasitic body diodes.

Therefore, it is advantageous to minimize the dead-time to provide peak optimal efficiency without compromising system reliability. The ZL2106 has optimized the dead-time for the integrated MOSFETs to maximizing efficiency.

Power Management Functional Description

Input Undervoltage Lockout

The input undervoltage lockout (UVLO) prevents the ZL2106 from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V_{UVLO}) can be set to either 4.5V or 10.8V using the SS pin according to Table 6.

The UVLO voltage can also be set to any value between 2.85V and 16V via the I²C/SMBus interface.

Once an input undervoltage fault condition occurs, the device can respond in a number of ways as follows:

1. Continue operating without interruption.
2. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device will remain in shutdown until instructed to restart.
3. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.

The default response from a UVLO fault is an immediate shutdown of the device. Please refer to Application Note AN2033 for details on how to configure the UVLO threshold or to select specific UVLO fault response options via the I²C/SMBus interface.

Output Overvoltage Protection

The ZL2106 offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at the VSEN pin) to a threshold set to 15% higher than the target output voltage (the default setting). If the VSEN voltage exceeds this threshold, the PG pin will de-assert and the device can then respond in a number of ways as follows:

1. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.
2. Turn off the high-side MOSFET and turn on the low-side MOSFET. The low-side MOSFET remains on until the device attempts a restart.

The default response from an overvoltage fault is to immediately shut down. For continuous overvoltage protection when operating from an external clock, the only allowed response is an immediate shutdown. Please refer to Application Note AN2033 for details on how to select specific overvoltage fault response options via I²C/SMBus.

Output Pre-Bias Protection

An output pre-bias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start up if a pre-bias condition exists at the output. The ZL2106 provides pre-bias protection by sampling the output voltage prior to initiating an output ramp.

If a pre-bias voltage lower than the target voltage exists after the pre-configured delay period has expired, the target voltage is set to match the existing pre-bias voltage and both drivers are enabled. The output voltage is then ramped to the final regulation value at the ramp rate set by the SS pin.

The actual time the output will take to ramp from the pre-bias voltage to the target voltage will vary depending on the pre-bias voltage but the total time elapsed from when the delay period expires and when the output reaches its target value will match the pre-configured ramp time (see Figure 18).

If a pre-bias voltage higher than the target voltage exists after the pre-configured delay period has expired, the target voltage is set to match the existing pre-bias voltage and both drivers are enabled with a PWM duty cycle that would ideally create the pre-bias voltage.

Once the pre-configured soft-start ramp period has expired, the PG pin will be asserted (assuming the pre-bias voltage is not higher than the overvoltage limit). The PWM will then adjust its duty cycle to match the original target voltage and the output will ramp down to the pre-configured output voltage.

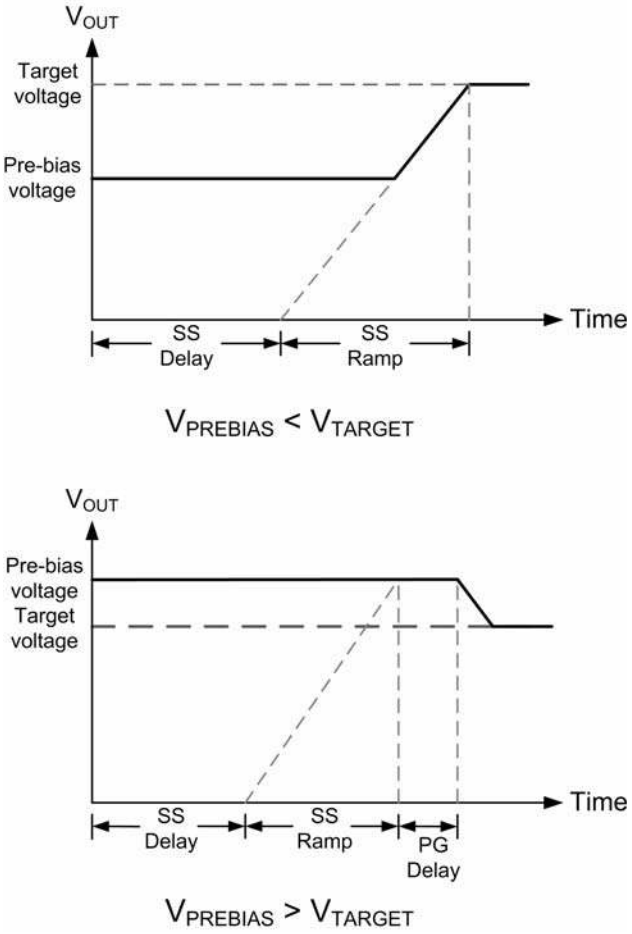


FIGURE 18. OUTPUT RESPONSES TO PRE-BIAS VOLTAGES

If a pre-bias voltage higher than the overvoltage limit exists, the device will not initiate a turn-on sequence and will declare an overvoltage fault condition to exist. In this case, the device will respond based on the output overvoltage fault response method that has been selected. See "Output Overvoltage Protection" on page 19 for response options due to an overvoltage condition.

Output Overcurrent Protection

The ZL2106 can protect the power supply from damage if the output is shorted to ground or if an overload condition is imposed on the output. Once the current limit threshold has been selected (see "Current Sensing and Current Limit Threshold Selection" on page 18), the user may determine the desired course of action in response to the fault condition. The following overcurrent protection response options are available:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.
6. The default response from an overcurrent fault is an immediate shutdown of the device. Please refer to Application Note AN2033 for details on how to select specific overcurrent fault response options via I^2C/SMBus.

Thermal Overload Protection

The ZL2106 includes an on-chip thermal sensor that continuously measures the internal temperature of the die and will shutdown the device when the temperature exceeds the preset limit. The factory default temperature limit is set to +125°C, but the user may set the limit to a different value if desired. See Application Note AN2033 for details. Note that setting a higher thermal limit via the I^2C/SMBus interface may result in permanent damage to the device. Once the device has been disabled due to an internal temperature fault, the user may select one of several fault response options as follows:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

If the user has configured the device to restart, the device will wait the preset delay period (if configured to do so) and will then check the device temperature. If the temperature has dropped below a threshold that is approximately +15°C lower than the selected temperature fault limit, the device will attempt to re-start. If the temperature still exceeds the fault limit the device will wait the preset delay period and retry again.

The default response from a temperature fault is an immediate shutdown of the device. Please refer to Application Note AN2033 for details on how to select specific temperature fault response options via I^2C/SMBus.

Voltage Tracking

High performance systems place stringent demands on the order in which the power supply voltages turn on. This is particularly true when powering FPGAs, ASICs, and other advanced processor devices that require multiple supply voltages to power a single die. In most cases, the I/O interface operates at a higher voltage than the core and therefore the core supply voltage must not exceed the I/O supply voltage according to the manufacturers' specifications. Voltage tracking protects these sensitive ICs by limiting the differential voltage among multiple power supplies during the power-up and power-down sequence. The ZL2106 integrates a lossless tracking scheme that allows its output to track a voltage that is applied to the VTRK pin with no additional components required. Figure 19 shows a basic I2C/SMBus tracking configuration. Please refer to Application Note AN2033

for more information on configuring tracking mode using PMBus commands.

Figure 23 is an example of a basic pin-strap tracking configuration. The VTRK pin is an analog input that, when tracking mode is enabled, the voltage applied to the VTRK pin performs as a reference for the device's output voltage. The ZL2106 offers two modes of tracking: coincident and ratiometric. Figures 20 and 21 illustrate the output voltage waveform for the two tracking modes.

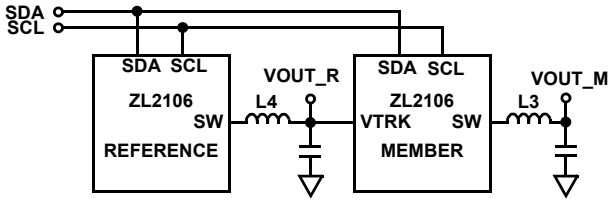


FIGURE 19. BASIC I²C TRACKING CONFIGURATION

1. Coincident. This mode configures the ZL2106 to ramp its output voltage at the same rate as the voltage applied to the VTRK pin. Two options are available for this mode;

a. Track at 100% V_{OUT} limited. Member rail tracks the reference rail and stops when the member reaches its target voltage, Figure 20 (A).

b. Track at 100% VTRK limited. Member rail tracks the reference at the instantaneous voltage value applied to the VTRK pin, Figure 20 (B).

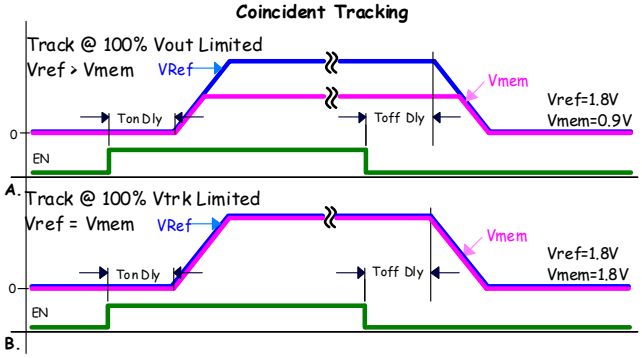


FIGURE 20. COINCIDENT TRACKING

2. Ratiometric. This mode configures the ZL2106 to ramp its output voltage as a percentage of the voltage applied to the VTRK pin. The default setting is 50%, but an external resistor may be used to configure a different tracking ratio.

a. Track at 50% V_{OUT} limited. Member rail tracks the reference rail and stops when the member reaches 50% of the target voltage, Figure 21 (A).

b. Track at 50% VTRK limited. Member rail tracks the reference at the instantaneous voltage value applied to the VTRK pin until the member rail reaches 50% of the reference rail voltage, or if the member is configured to less than 50% of the reference the member will achieve its configured target, Figure 21 (B).

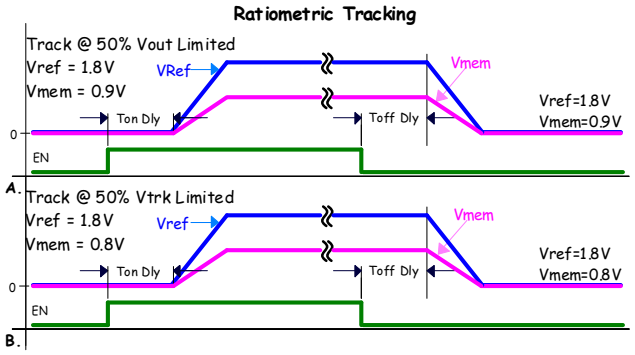


FIGURE 21. RATIOMETRIC TRACKING

Tracking Overview

When the ZL2106 is configured to the voltage tracking mode, the voltage applied to the VTRK pin acts as a reference for the member device(s) output regulation. The soft-start values (Rise/Fall times) are used to calculate the loop gain used during the turn-on/turn-off ramps, therefore the minimum rise/fall time has been constrained to 5ms to ensure accuracy. Tracking accuracy can be improved by increasing the rise and fall times beyond 5ms.

Tracking Groups

In a tracking group, the device configured to the highest voltage within the group is defined as the reference device. The device(s) that track the reference are called the member device(s). The reference device will control the ramp delay and ramp rate of all tracking devices and is not placed in the tracking mode.

The reference device is configured to the highest output voltage for the group and all other device(s) output voltages are meant to track and never exceed the reference device output voltage.

The reference device must be configured to have a minimum Time-On Delay and Time-On Rise as shown in Equation 13.

$$tON_{DLY(REF)} \geq tON_{DLY(MEM)} + tON_{RISE(REF)} + 5ms \geq tON_{DLY(MEM)} + 10ms \quad \text{(EQ. 13)}$$

This delay allows the member device(s) to prepare their control loops for tracking following the assertion of ENABLE.

The member device Time-Off Delay has been redefined to describe the time that the VTRK pin will follow the reference voltage after enable is de-asserted. The delay setting sets the timeout for the member's output voltage to turnoff in the event that the reference output voltage does not achieve zero volts.

The member device(s) must have a minimum Time-Off Delay of as shown in Equation 14.

$$tOFF_{DLY(MEM)} \geq tOFF_{DLY(REF)} + tOFF_{FALL(REF)} + 5ms \quad \text{(EQ. 14)}$$

It is assumed for a tracking group, that all of the ENABLE pins are connected together and driven by a single logic source or PMBus Broadcast Enable is used.

The configuration settings for Figures 20 and 21 are shown below in Figure 22. In each case the reference and member rise times are set to the same value.

Tracking Configuration Figure 20 (A)						
Rail	Vout Set (Volts)	Time On Dly (ms)	Time On Rise (ms)	Time Off Dly (ms)	Time Off Fall (ms)	Mode
Reference	1.8	15	5	5	5	Track Disabled
Member	0.9	5	5	15	5	100% Vout Limited

Tracking Configuration Figure 20 (B)						
Rail	Vout Set (Volts)	Time On Dly (ms)	Time On Rise (ms)	Time Off Dly (ms)	Time Off Fall (ms)	Mode
Reference	1.8	15	5	5	5	Track Disabled
Member	1.8	5	5	15	5	100% VTRK Limited

Tracking Configuration Figure 21 (A)						
Rail	Vout Set (Volts)	Time On Dly (ms)	Time On Rise (ms)	Time Off Dly (ms)	Time Off Fall (ms)	Mode
Reference	1.8	15	5	5	5	Track Disabled
Member	0.9	5	5	15	5	Track 50% Vout Limited

Tracking Configuration Figure 21 (B)						
Rail	Vout Set (Volts)	Time On Dly (ms)	Time On Rise (ms)	Time Off Dly (ms)	Time Off Fall (ms)	Mode
Reference	1.8	15	5	5	5	Track Disabled
Member	1.8	5	5	15	5	Track 50% VTRK Limited

FIGURE 22. TRACKING CONFIGURATION FOR FIGURES 20 AND 21

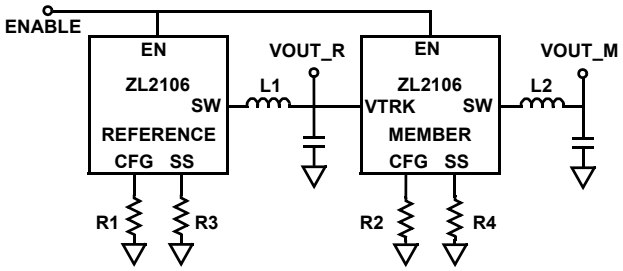


FIGURE 23. BASIC PIN-STRAP TRACKING CONFIGURATION

Tracking Configured by Pin-Strap

Tracking is enabled with the CFG pin as shown in Table 16 on page 24, and configured to a specific ramp rate using the SS pin, as shown in Table 13 on page 22. Figure 23 shows the basic schematic of pin-strap tracking.

Voltage Margining

The ZL2106 offers a simple means to vary its output higher or lower than its nominal voltage setting in order to determine whether the load device is capable of operating over its specified supply voltage range. The MGN command is set by driving the MGN pin or through the I²C/SMBus interface. The MGN pin is a tri-level input that is continuously monitored and can be driven directly by a processor I/O pin or other logic-level output.

The ZL2106's output will be forced higher than its nominal set point when the MGN command is set HIGH, and the output will be forced lower than its nominal set point when the MGN command is set LOW. Default margin limits of V_{NOM} ±5% are pre-loaded in the factory, but the margin limits can be modified through the I²C/SMBus interface to as high as V_{NOM} + 10% or as low as 0V, where V_{NOM} is the nominal output voltage set point determined by the VSET pin. The ZL2106-01 allows 150% margin limits.

The margin limits and the MGN command can both be set individually through the I²C/SMBus interface. Additionally, the transition rate between the nominal output voltage and either margin limit can be configured through the I²C/SMBus interface. Please refer to Application Note AN2033 for detailed instructions on modifying the margining configurations.

TABLE 13. TRACKING MODE CONFIGURATION

R_{SS} (kΩ)	UVLO (V)	TRACKING RATIO (%)	UPPER TRACK LIMIT	RAMP-UP/DOWN BEHAVIOR
19.6	5.5	100	Limited by target voltage	Output not allowed to decrease before PG
21.5				Output will always follow VTRK
23.7			Limited by VTRK pin voltage	Output not allowed to decrease before PG
26.1				Output will always follow VTRK
28.7		50	Limited by target voltage	Output not allowed to decrease before PG
31.6				Output will always follow VTRK
34.8			Limited by VTRK pin voltage	Output not allowed to decrease before PG
38.3				Output will always follow VTRK
56.2	7.5	100	Limited by target voltage	Output not allowed to decrease before PG
61.9				Output will always follow VTRK
68.1			Limited by VTRK pin voltage	Output not allowed to decrease before PG
75				Output will always follow VTRK
82.5		50	Limited by target voltage	Output not allowed to decrease before PG
90.9				Output will always follow VTRK
100			Limited by VTRK pin voltage	Output not allowed to decrease before PG
110				Output will always follow VTRK

I²C/SMBus Communications

The ZL2106 provides an I²C/SMBus digital interface that enables the user to configure all aspects of the device operation as well as monitor the input and output parameters. The ZL2106 can be used with any standard 2-wire I²C host device.

In addition, the device is compatible with SMBus version 2.0 and includes an SALRT line to help mitigate bandwidth limitations related to continuous fault monitoring. Pull-up resistors are required on the I²C/SMBus as specified in the SMBus 2.0 specification. The ZL2106 accepts most standard PMBus commands. When controlling the device with PMBus commands, it is recommended that the enable pin is tied to SGND.

I²C/SMBus Device Address Selection

When communicating with multiple devices using the I²C/SMBus interface, each device must have its own unique address so the host can distinguish between the devices. The device address can be set according to the pin-strap options listed in Table 14. Address values are right-justified.

TABLE 14. SMBUS DEVICE ADDRESS SELECTION

SA PIN SETTING	SMBus ADDRESS
LOW	0x20
OPEN	0x21
HIGH	0x22

If additional device addresses are required, a resistor can be connected to the SA pin according to Table 15 to provide up to 30 unique device addresses.

Digital-DC Bus

The Digital-DC Communications (DDC) bus is used to communicate between Zilker Labs Digital-DC devices. This dedicated bus provides the communication channel between devices for features such as sequencing and fault spreading. The DDC pin on all Digital-DC devices in an application should be connected together. A pull-up resistor is required on the DDC bus in order to guarantee the rise time as expressed in Equation 15:

$$\text{Rise Time} = R_{PU} \bullet C_{LOAD} \approx 1\mu s \quad \text{(EQ. 15)}$$

Where R_{PU} is the DDC bus pull-up resistance and C_{LOAD} is the bus loading. The pull-up resistor may be tied to VRA or to an external 3.3V or 5V supply as long as this voltage is present prior to or during device power-up. As rules of thumb, each device connected to the DDC bus presents approximately 10pF of capacitive loading, and each inch of FR4 PCB trace introduces approximately 2pF. The ideal design will use a central pull-up resistor that is well matched to the total load capacitance. In power module applications, the user should consider whether to place the pull-up resistor on the module or on the PCB of the end application.

The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that will ensure a logic 0 (typically 0.8V at the device monitoring point) given the pull-up voltage (5V if tied to VRA) and the pull-down current capability of the ZL2106 (nominally 4mA).

TABLE 15. SMBus ADDRESS VALUES

R_{SA} (kΩ)	SMBus Address
10	0x20
11	0x21
12.1	0x22
13.3	0x23
14.7	0x24
16.2	0x25
17.8	0x26
19.6	0x27
21.5	0x28
23.7	0x29
26.1	0x2A
28.7	0x2B
31.6	0x2C
34.8	0x2D
38.3	0x2E
42.2	0x2F
46.4	0x30
51.1	0x31
56.2	0x32
61.9	0x33
68.1	0x34
75	0x35
82.5	0x36
90.9	0x37
100	0x38
110	0x39
121	0x3A
133	0x3B
147	0x3C
162	0x3D

Phase Spreading

When multiple point of load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device such that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Since the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

In order to enable phase spreading, all converters must be synchronized to the same switching clock. The CFG pin is used to set the configuration of the SYNC pin for each device as described in “Switching Frequency and PLL” on page 15.

Selecting the phase offset for the device is accomplished by selecting a device address according to the following equation:

Phase offset = device address x 45°

For example:

- A device address of 0x00 or 0x20 would configure no phase offset
- A device address of 0x01 or 0x21 would configure 45° of phase offset
- A device address of 0x02 or 0x22 would configure 90° of phase offset

The phase offset of each device may also be set to any value between 0° and 360° in 22.5° increments via the I^2C/SMBus interface. Refer to Application Note AN2033 for further details.

Output Sequencing

A group of Zilker Labs devices may be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs, and ASICs that require one supply to reach its operating voltage prior to another supply reaching its operating voltage in order to avoid latch-up from occurring. Multi-device sequencing can be achieved by configuring each device through the I^2C/SMBus interface or by using Zilker Labs patented autonomous sequencing mode.

Autonomous sequencing mode configures sequencing by using events transmitted between devices over the DDC bus.

The sequencing order is determined using each device’s SMBus address. Using autonomous sequencing mode (configured using the CFG pin), the devices must be assigned sequential SMBus addresses with no missing addresses in the chain. This mode will also constrain each device to have a phase offset according to its SMBus address as described in section “Phase Spreading” on page 24.

TABLE 16. CFG PIN CONFIGURATIONS FOR SEQUENCING AND TRACKING

R_{CFG}	SYNC PIN CONFIGURATION	SEQUENCING CONFIGURATION
Low	Input	Sequencing and Tracking are disabled.
Open	Auto detect	
High	Output	
10kΩ	Input	Sequencing and Tracking are disabled.
11kΩ	Auto detect	
12.1kΩ	Output	
14.7kΩ	Input	Device is FIRST in nested sequence. Tracking disabled.
16.2kΩ	Auto detect	
17.8kΩ	Output	
21.5kΩ	Input	Device is LAST in nested sequence. Tracking disabled.
23.7kΩ	Auto detect	
26.1kΩ	Output	
31.6kΩ	Input	Device is MIDDLE in nested sequence. Tracking disabled.
34.8kΩ	Auto detect	
38.3kΩ	Output	
46.4kΩ	Input	Sequence disabled. Tracking enabled as defined in Table 13.
51.1kΩ	Auto detect	
56.2kΩ	Output	

The sequencing group will turn on in order starting with the device with the lowest SMBus address and will continue through to turn on each device in the address chain until all devices connected have been turned on. When turning off, the device with the highest SMBus address will turn off first followed in reverse order by the other devices in the group.

Sequencing is configured by connecting a resistor from the CFG pin to ground as described in Table 16. The CFG pin is also used to set the configuration of the SYNC pin as well as to determine the sequencing method and order. Please refer to section “Switching Frequency and PLL” on page 15 for more details on the operating parameters of the SYNC pin.

Multiple device sequencing may also be achieved by issuing PMBus commands to assign the preceding device in the sequencing chain as well as the device that will follow in the sequencing chain. This method places fewer restrictions on the SMBus address (no need of sequential address) and also allows the user to assign any phase offset to any device irrespective of its SMBus device address.

The Enable pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. Enable must be driven low to initiate a sequenced turnoff of the group. Please refer to Application Note AN2033 for details on sequencing via the I^2C/SMBus interface.

Fault Spreading

Digital-DC devices can be configured to broadcast a fault event over the DDC bus to the other devices in the group. When a non-destructive fault occurs and the device is configured to shut down on a fault, the device will shut down and broadcast the fault event over the DDC bus. The other devices on the DDC bus will shut down together if configured to do so, and will attempt to re-start in their prescribed order if configured to do so.

Monitoring via I²C/SMBus

A system controller can monitor a wide variety of different ZL2106 system parameters through the I²C/SMBus interface. The device can monitor for fault conditions by monitoring the SALRT pin, which will be pulled low when any number of pre-configured fault conditions occur.

The device can also be monitored continuously for any number of power conversion parameters including input voltage, output voltage, output current, internal junction temperature, switching frequency and duty cycle.

The PMBus host should respond to SALRT as follows:

1. ZL device pulls SALRT low.
2. PMBus host detects that SALRT is now low, performs transmission with Alert Response Address to find which ZL device is pulling SALRT low.
3. PMBus host talks to the ZL device that has pulled SALRT low. The actions that the host performs are up to the system designer.

If multiple devices are faulting, SALRT will still be low after doing the above steps and will require transmission with the Alert Response Address repeatedly until all faults are cleared. Please refer to Application Note AN2033 for details on how to monitor specific parameters via the I²C/SMBus interface.

Snapshot™ Parametric Capture

The ZL2106 offers a special feature that enables the user to capture parametric data during normal operation or following a fault. The Snapshot functionality is enabled by setting bit 1 of MISC_CONFIG to 1.

See AN2033 for details on using Snapshot in addition to the parameters supported. The Snapshot feature enables the user to read the parameters via a block read transfer through the SMBus. This can be done during normal operation, although it should be noted that reading the 22 bytes will occupy the SMBus for some time.

The SNAPSHOT_CONTROL command enables the user to store the snapshot parameters to Flash memory in response to a pending fault as well as to read the stored data from Flash memory after a fault has occurred. Table 17 describes the usage of this command. Automatic writes to Flash memory following a fault are triggered when any fault threshold level is exceeded, provided that the specific fault's response is to shut down (writing to Flash memory is not allowed if the device is configured to re-try following the specific fault condition).

It should also be noted that the device's V_{DD} voltage must be maintained during the time when the device is writing the data to Flash memory; a process that requires between 700µs to 1400µs depending on whether the data is set up for a block write. Undesirable results may be observed if the device's V_{DD} supply drops below 3.0V during this process.

TABLE 17. SNAPSHOT_CONTROL COMMAND

DATA VALUE	DESCRIPTION
1	Copies current SNAPSHOT values from Flash memory to RAM for immediate access using SNAPSHOT command.
2	Writes current SNAPSHOT values to Flash memory. Only available when device is disabled.

In the event that the device experiences a fault and power is lost, the user can extract the last SNAPSHOT parameters stored during the fault by writing a 1 to SNAPSHOT_CONTROL (transfers data from Flash memory to RAM) and then issuing a SNAPSHOT command (reads data from RAM via SMBus).

Non-Volatile Memory and Device Security Features

The ZL2106 has internal non-volatile memory where user configurations are stored. Integrated security measures ensure that the user can only restore the device to a level that has been made available to them. Refer to "Start-up Procedure" on page 13 for details on how the device loads stored values from internal memory during start-up.

During the initialization process, the ZL2106 checks for stored values contained in its internal memory. The ZL2106 offers two internal memory storage units that are accessible by the user as follows:

1. *Default Store*: A power supply module manufacturer may want to protect the module from damage by preventing the user from being able to modify certain values that are related to the physical construction of the module. In this case, the module manufacturer would use the Default Store and would allow the user to restore the device to its default setting but would restrict the user from restoring the device to the factory settings.
2. *User Store*: The manufacturer of a piece of equipment may want to provide the ability to modify certain power supply settings while still protecting the equipment from modifying values that can lead to a system level fault. The equipment manufacturer would use the User Store to achieve this goal.

Please refer to Application Note AN2033 for details on how to set specific security measures via the I²C/SMBus interface.

Revision History

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DATE	REVISION	CHANGE
February, 01, 2013	FN6852.6	Removed obsolete parts, parts no longer scheduled for release and evaluation board from Ordering Information table. Updated Theta JC in Thermal Information from 1 to 1.7.
March 31, 2011	FN6852.5	In “Absolute Maximum Ratings” on page 6, changed following from: High-Side Supply Voltage for BST Pin. . . . . .-0.3V to 30V to: High-Side Supply Voltage for BST Pin. . . . . .-0.3V to 25V
December 16, 2010	FN6852.4	Added following parts to “Ordering Information” on page 5: ZL2106ALCF-01 ZL2106ALCFT-01 ZL2106ALCFTK-01 ZL2106ALCF ZL2106ALCFT ZL2106ALCFTK Added corresponding Pb-free lead finish note (Note 2) Added corresponding Package Outline Drawing L36.6x6C to page 29. In “Voltage Margining” on page 22, changed the last sentence in the 2nd paragraph from "A safety feature prevents the user from configuring the output voltage to exceed VNOM + 10% under any conditions." to "The ZL2106-01 allows 150% margin limits."
December 15, 2010	FN6852.3	Updated over temp note in MIN MAX columns of spec table from "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested." to new standard "Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design." Removed Note "Limits established by characterization and are not production tested." and all references to it.
November 30, 2010		Added following statement to disclaimer on page 31: “This product is subject to a license from Power One, Inc. related to digital power technology as set forth in U.S. Patent No. 7,000,125 and other related patents owned by Power One, Inc. These license rights do not extend to stand-alone POL regulators unless a royalty is paid to Power One, Inc.”
July 9, 2010		Text above Equation 13 changed From: The reference device must be configured to have a minimum Time-On Delay of 10ms greater than the member device as shown in Equation 13. To: The reference device must be configured to have a minimum Time-On Delay and Time-On Rise as shown in Equation 13. Made correction to Equation 13 to read From: tONDLY(REF) >/- tONRISE(REF) + 5ms To: $tON_{DLY(REF)} \geq tON_{DLY(MEM)} + tON_{RISE(REF)} + 5ms \geq tON_{DLY(MEM)} + 10ms$ Figure 22, last row changed From: 1.8 5 5 15 5 To: 0.8 5 5 15 5
July 1, 2010		Revamped Voltage Tracking Section adding details about the tracking feature. Changed in Page 1, 1st paragraph "The ZL2106 is an innovative power conversion..." to "The ZL2106 is a digital power conversion..." Made correction to Figure 19 - Connected SDA and SCL to Member device. Made correction to Figure 23 by changing SDA and SCL labels in each device to “EN”. Added word “Enable” and added labels CFG, SS, R1, R3, R2 and R4. Changed in Voltage Tracking - Ratiometric on page 23 first sentence changed from: “This mode configures the ZL2106 to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRK pin”. to “This mode configures the ZL2106 to ramp its output voltage as a percentage of the voltage applied to the VTRK pin”. Titles of Table in Figure 22 changed from “Tracking Configuration Example 1A, 1B, 2A, 2B” to “Tracking Configuration Figure 20 (A), 20 (B), 21 (A), 21 (B)”. Figures 20and 21 added “0” and “EN” to Timing Tracking Graphics.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev. **(Continued)**

DATE	REVISION	CHANGE
February 11, 2010	FN6852.2	Typo on Page 24, Table 15, resistor values 34.8 and 31.6 swapped so that 31.6 is 0x2C and 34.8 is 0x2D in the table.
November 20, 2009	FN6852.1	On page 16. Table 9. “RSYNC RESISTOR VALUES”. Changed values of last 4 rows from: 34.8kohm | 727kHz 38.3kohm | 800kHz 46.4kohm | 889kHz 51.1kohm | 1000kHz to: 34.8kohm | 667kHz 38.3kohm | 727kHz 42.2kohm | 889kHz 46.4kohm | 1000kHz
October 13, 2009		Removed “SNAPSHOT PARAMETERS” table. Added “See AN2033 for details on using Snapshot in addition to the parameters supported. “ to “Snapshot™ Parametric Capture ” on page 25
October 1, 2009		1) Updated to new format. Updates include: a) Moving Typical Application Circuits to front of datasheet, per new standard b) Putting Abs Max, Recommended Operating Conditions and Electrical Specs tables into Intersil format - Adding Pb-free reflow link to Thermal info - Adding Intersil's caution statement, per legal - Added ESD ratings c) Put Ordering Info table into Intersil format - Adding Moisture Sensitivity Level note, TB347 tape and reel spec note and Pb-free note (corresponding to lead finish). Added evaluation board. d) Updated sales disclaimer on last page to Intersil's verbiage e) Replaced Zilker POD with Intersil equivalent POD (L36.6x6A) f) Updated graphics to Intersil standards (font change) g) Updated cross references to tables (since table #s were removed from Electrical Specs, Abs Max, Recommended Operating Conditions and Pin Descriptions tables) h) Updated cross references to figures (since figure #s were removed from Block Diagram and Pinout) i) Added equation #s to all equations j) Added Intersil standard over temp notes to Electrical Specs table as follows: - Added Note 18: "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested." to MIN MAX columns of Electrical Specs table. -Added "Boldface limits apply over the operating temperature range, -40°C to +85°C" to common conditions of Electrical Specs table. Bolded all MIN and MAX specs in table. k) Revised page 1. Shortened Features and added Efficiency curve 2) On page 6; Removed "low" from the “Power-good V_{OUT} Low Threshold” line in the Electrical Specs table 3) On page 14; “SOFT-START DELAY AND RAMP SETTINGS” table (was Table 9, now Table 5): Changed UVLO from 4.5V to 7.5V 4) On page 14; “DELAY AND RAMP CONFIGURATION” table (was Table 10, now Table 6): Ramp Time and Delay Time swapped columns and values changed. Updated UVLO values. 5) On page 10; 2nd column, removed 2nd paragraph "Application notes and reference .. .. to order an evaluation kit." 6) On page 22; Table 13, “TRACKING MODE CONFIGURATION”, changed UVLO values "4.5" to "5.5" and "10.8" to "7.5" 7) On page 22; Table 13, “TRACKING MODE CONFIGURATION”, changed Rss values from: "42.2" to "56.2" "46.4" to "61.9" "51.1" to "68.1" "56.2" to "75" "61.9" to "82.5" "68.1" to "90.9" "75" to "100" "82.5" to "110

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev. **(Continued)**

DATE	REVISION	CHANGE
October 1, 2009 (Cont.)	FN6852.1 (Cont.)	8) In Thermal Information, changed Thermal Tja from “35” to “28” and Tjc from “5” to “1” 10) In Thermal Information, changed Dissipation Limits from “3.25W, 2.25W, 1.25W” to “3.5W, 2.5W, 1.4W” 9) In Spec table, changed conditions for VRA and V2P5 Reference Output Voltage from “50mA” to “20mA” 10) In Spec table, added Reference Note 19 (Limits established by characterization and not production tested) to Soft-start Delay Duration in conditions. 11) Changed Part Numbers in Ordering Information from From “ZL2106ALBN, ZL2106ALBNT, ZL2106ALBNTK” to “ZL2106ALCN, ZL2106ALCNT, ZL2106ALCNTK”
February 19, 2009	FN6852.0	Assigned file number FN6852 to datasheet as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read “Intersil and it’s subsidiaries including Zilker Labs, Inc.” No changes to datasheet content
November, 2008	1.1	1) Added Notes 1, 5, 8 and 9 to Electrical Specifications Table 2) Corrected T_j = 25 °C in Figures 5 and 6 3) Added $T_j \leq 125$°C in Figures 8 and 9 4) Added last paragraph to “Multi-mode Pins” on page 11 5) Changed PG delay to 1ms in “Power-good (PG)” on page 15 6) Added note for SYNC clock auto detect in “Switching Frequency and PLL” Section 7) Updated first paragraph of “Current Sensing and Current Limit Threshold Selection” on page 18 8) Changed default fault response to immediate shutdown in “Input Undervoltage Lockout” on page 19, “Output Overvoltage Protection” on page 19, “Output Overcurrent Protection” on page 20 and “Thermal Overload Protection” on page 20. 9) Updated Ordering Information
August, 2008	1.0	Initial Release

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the fastest growing markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil or to find out how to become a member of our winning team, visit our website and career page at www.intersil.com.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective product information page. Also, please check the product information page to ensure that you have the most updated datasheet: ZL2106

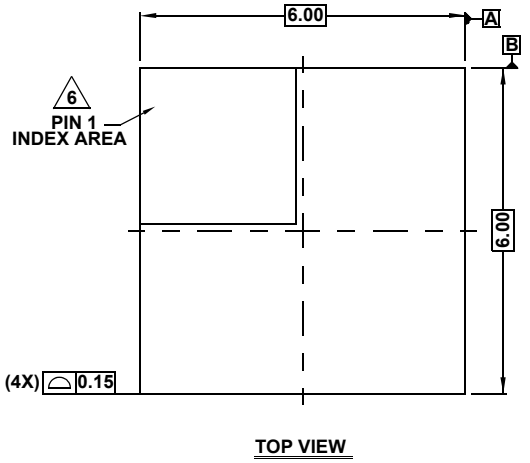
To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

Reliability reports are available from our website at: http://rel.intersil.com/reports/search.php

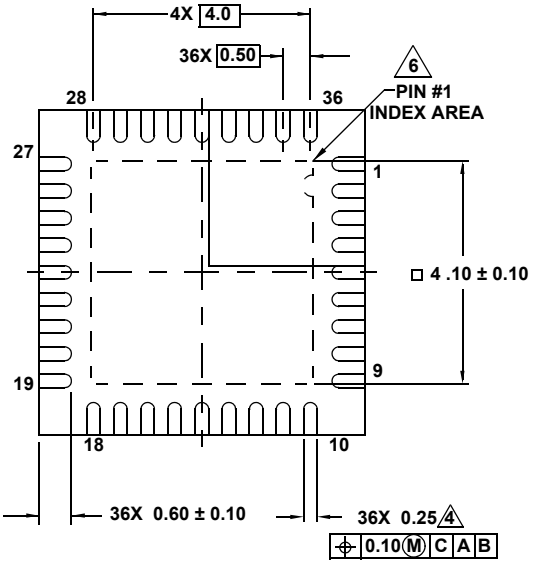
Package Outline Drawing

L36.6x6C

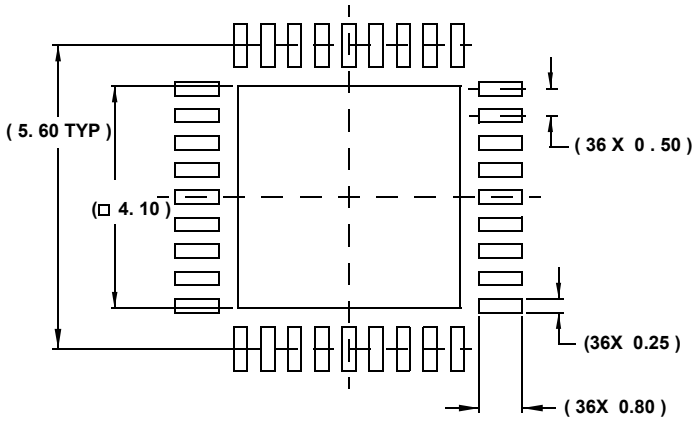
36 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 4/10



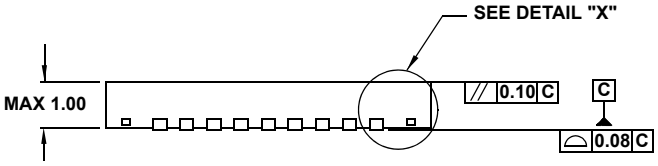
TOP VIEW



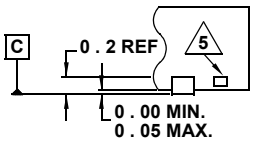
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220VJJD.