Precision Coulomb Counter / Low Side Current Monitor for High-current Applications

BD7220FV-C

General Description

BD7220FV-C is a coulomb counter IC for high-current applications. The product integrates a high-accuracy operational amp, a current accumulation logic circuit and a 16-bit ΔΣADC to perform current accumulation with high precision. The current sense input supports shunt resistors and output current sensors, and uses the SPI communication interface. BD7220FV-C only requires SPI commands to carry out the calibration necessary for high-precision measurement, so it can also get current accumulation information for battery state-of-charge estimation.

Features

- AEC-Q100 Qualified *(Note 1)*
- 16-bit ΔΣADC
- Flexible Noise Filter (4 settings)
- Automatic Calibration via SPI
- High-accuracy Op-amp with 3 Gain Settings (5 V/V, 25 V/V, 51 V/V)
- Supports Current Sensing Using Shunt Resistors
- Supports Current Sensing Using Current Output Type Current Sensors
- SPI I/F (Optional CRC)
- Coulomb Counter Function with SPI External Communication
- Accumulation Current Counter which Counts Charge and Discharge Independently
- Adjustable Current Detection Interruption (3 settings)
- 4 Operation Modes (NORMAL, SLEEP, SSHDN, OFF)
- Wake Up Current Detection Function
- UVLO

(Note 1) Grade 1

Key Specifications

- Input Voltage Range
  - VCC Input Voltage Range 4.5 V to 5.5 V
  - VDD Input Voltage Range 2.5 V to 5.5 V
- Operating Temperature
  - -40 °C to +125 °C

Applications

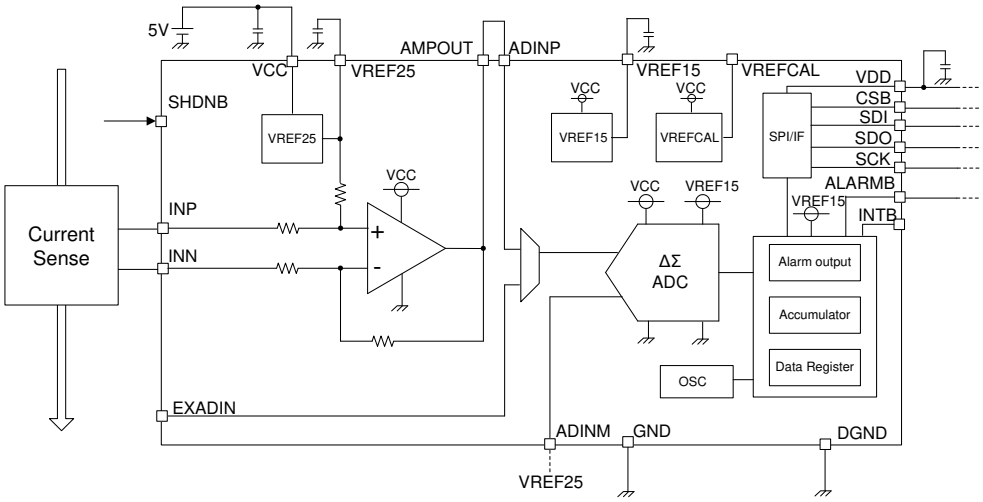
- Battery Current Sense for EV
- Electricity Storage Systems
- Automated Guided Vehicle (AGV)
- Robot

Package

	W (Typ) x D (Typ) x H (Max)
SSOP-B20	6.5 mm x 6.4 mm x 1.45 mm

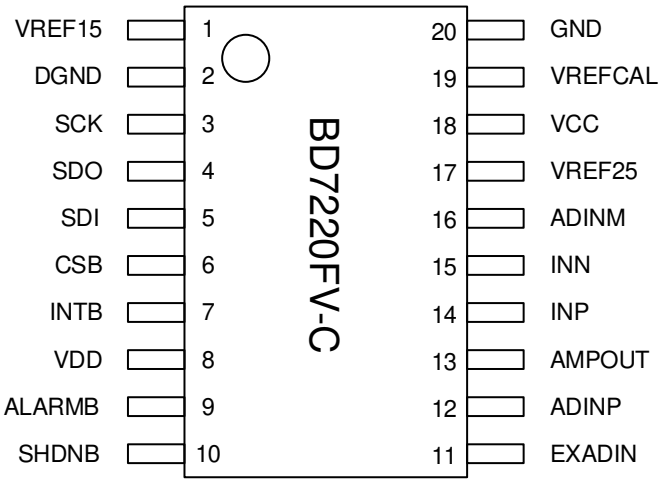
SSOP-B20

Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Pin Configuration

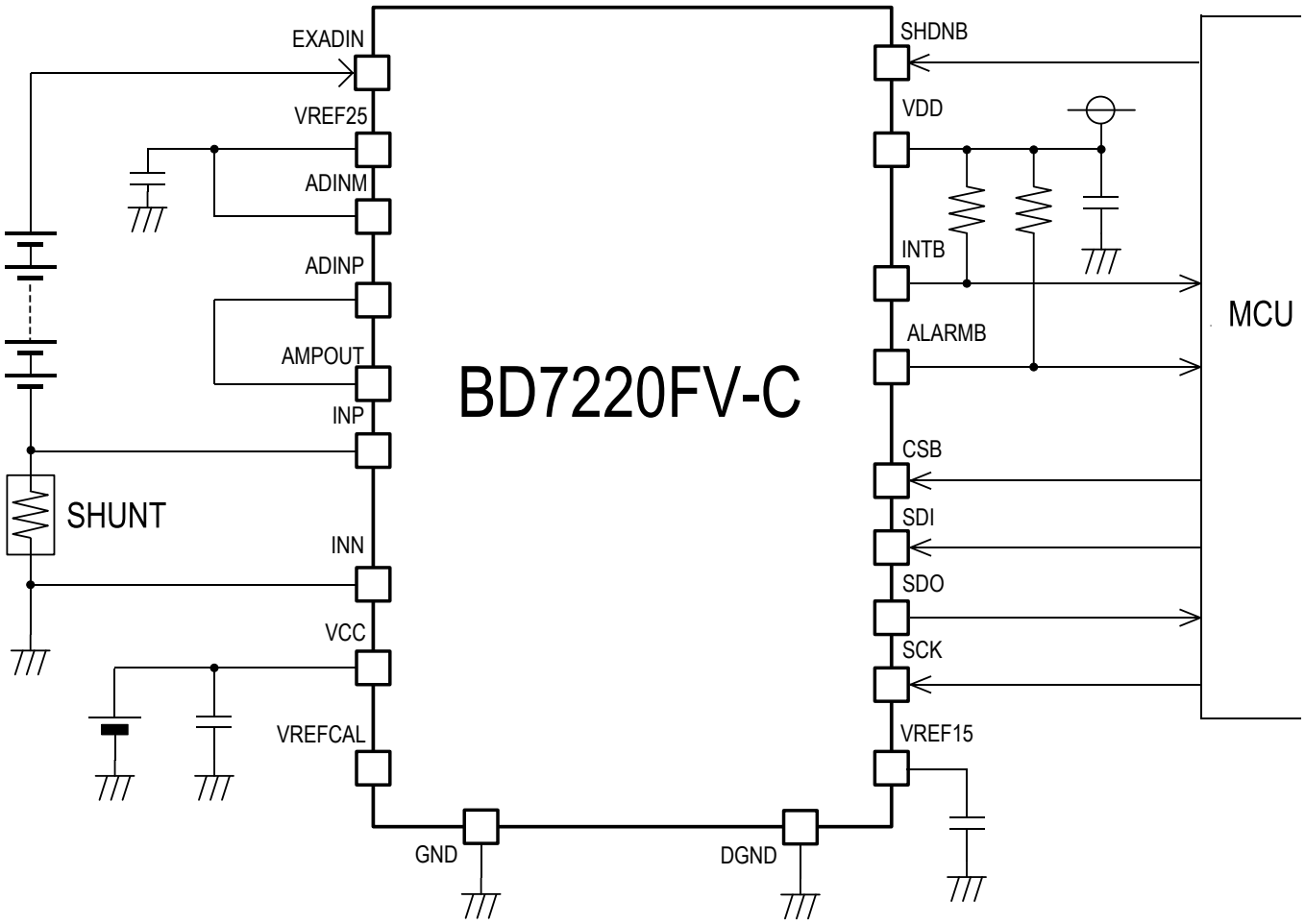


SSOP-B20 (TOP VIEW)

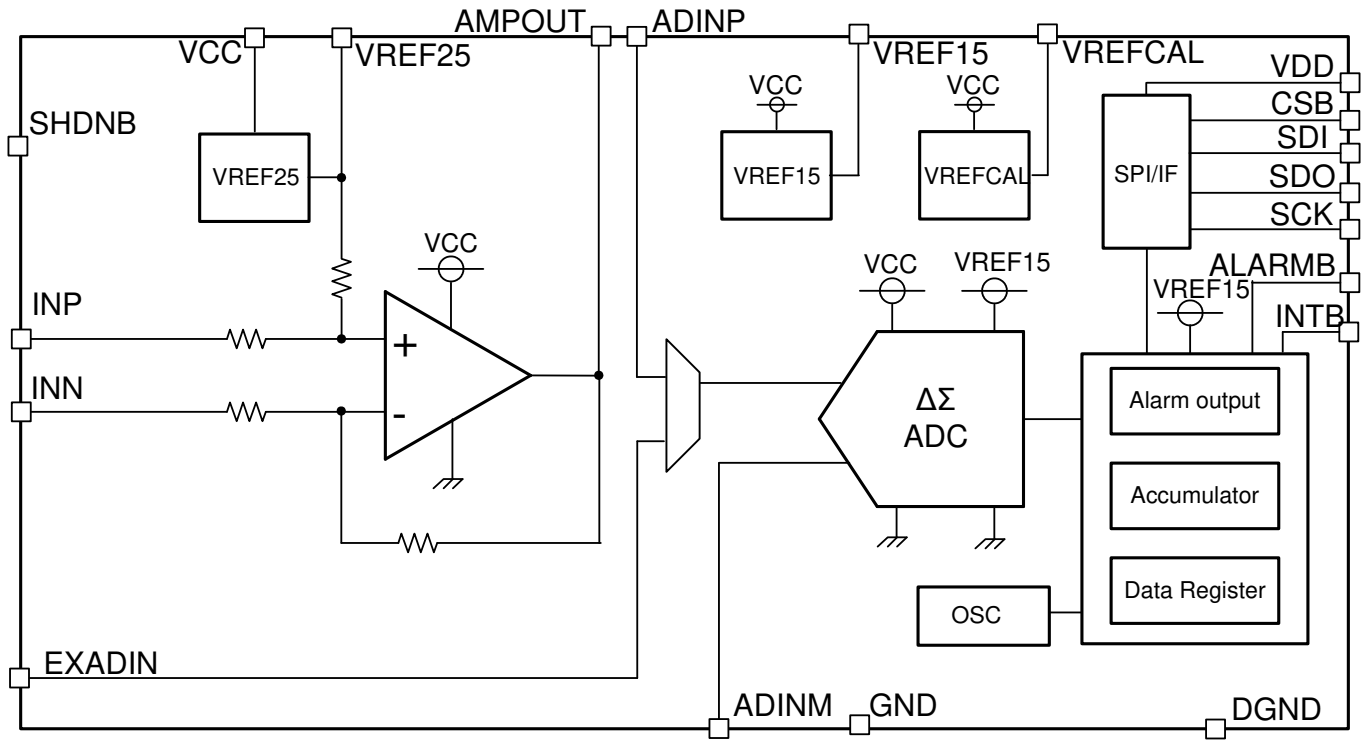
Pin Description

Pin No.	Pin Name	I/O	Function
1	VREF15	O	LDO output for internal power
2	DGND	-	Digital ground
3	SCK	I	SPI clock input
4	SDO	O	SPI data output
5	SDI	I	SPI data input
6	CSB	I	SPI chip select input
7	INTB	O	Event interrupt output open drain
8	VDD	-	Power supply for SPI I/F
9	ALARMB	O	Alarm output open drain
10	SHDNB	I	Shutdown Input (H: operating, L: shutdown)
11	EXADIN	I	Delta sigma ADC select input
12	ADINP	I	Delta sigma ADC monitor input
13	AMPOUT	O	Internal amp output
14	INP	I	Internal amp non-inverting input
15	INN	I	Internal amp inverting input
16	ADINM	I	Delta sigma ADC reference input
17	VREF25	O	Internal reference output
18	VCC	-	Power supply
19	VREFCAL	O	Reference output for calibration in BD7220FV-C shipment process
20	GND	-	Analog ground

Application Example



Block Diagram



Absolute Maximum Ratings (Ta = 25 °C)

Item	Symbol	Limit	Unit
Voltage Range1 (VCC, VDD)	V_{AMR_1}	-0.3 to +7.0	V
Voltage Range2 (VREF15)	V_{AMR_2}	-0.3 to +2.1	V
Voltage Range3 (VREF25, VREFCAL, INP, INN, EXADIN, SHDNB, INTB, ALARMB, AMPOUT, ADINP, ADINM, CSB, SDI, SDO, SCK)	V_{AMR_3}	-0.3 to +7.0	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance *(Note 2)*

Parameter	Symbol	Thermal Resistance(Typ)		Unit
		1s *(Note 4)*	2s2p *(Note 5)*	
SSOP-B20				
Junction to Ambient	θ_{JA}	115.4	57.3	°C/W
Junction to Top Characterization Parameter *(Note 3)*	Ψ_{JT}	10	8	°C/W

(Note 2) Based on JESD51-2A (Still-Air)
(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 4) Using a PCB board based on JESD51-3
(Note 5) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Condition

Item	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Voltage Range1 (VCC)	V_{OPR_1}	4.5	5.0	5.5	V	
Voltage Range2 (VDD)	V_{OPR_2}	2.5	3.3	5.5	V	
Operating Temperature	Topr	-40	+25	+125	°C	

Electrical Characteristics

(Unless otherwise specified, Ta = -40 °C to +125 °C, VCC = 5.0 V, VDD = 3.3 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
VREF15						
Output Voltage1	V_{O15_1}	1.470	1.500	1.530	V	Io = 0 mA, Ta= +25 °C
Output Voltage2	V_{O15_2}	1.450	1.500	1.550	V	Io = 0 mA, Ta= -40 °C to +125 °C
Effective Output Capacitance	C_{VO15}	0.4	-	2.0	µF	Recommended Nominal Capacitor:1 µF
VREF25						
Output Voltage1	V_{O25_1}	2.450	2.500	2.550	V	Io = 0 mA, Ta= +25 °C
Output Voltage2	V_{O25_2}	2.400	2.500	2.600	V	Io = 0 mA, Ta= -40 °C to +125 °C
Effective Output Capacitance	C_{VO25}	0.4	-	2.0	µF	Recommended Nominal Capacitor:1 µF
OSC						
Frequency1	f_{OSC_1}	8110	8192	8274	kHz	Ta= +25 °C
Frequency2	f_{OSC_2}	8028	8192	8356	kHz	Ta= -40 °C to +125 °C
Start up Time	$t_{WAKEOSC}$	-	50	200	µs	

(Unless otherwise specified, Ta = -40 °C to +125 °C, VCC = 5.0 V, VDD = 3.3 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Current Consumption						
Shutdown Current 1_1 (OFF) = HSHDN	I_{QVB1_1}	-	0	5	µA	SHDNB = L, MODE_SEL [1:0] = 2'bXX VREF15 = OFF, VREF25 = OFF AMP = OFF, ΔΣADC = OFF OSC = OFF, Ta= +25 °C
Shutdown Current 1_2 (OFF) = HSHDN	I_{QVB1_2}	-	0	10	µA	SHDNB = L, MODE_SEL [1:0] = 2'bXX VREF15 = OFF, VREF25 = OFF AMP = OFF, ΔΣADC = OFF OSC = OFF, Ta= -40 °C to +125 °C
Shutdown Current 2_1 (Soft Shutdown Mode) = SSHDN	I_{QVB2_1}	-	20	40	µA	SHDNB = H, MODE_SEL [1:0] = 2'b11 VREF15 = ON, VREF25 = OFF AMP = OFF, ΔΣADC = OFF OSC = OFF, Ta= +25 °C
Shutdown Current 2_2 (Soft Shutdown Mode) = SSHDN	I_{QVB2_2}	-	20	200	µA	SHDNB = H, MODE_SEL [1:0] = 2'b11 VREF15 = ON, VREF25 = OFF AMP = OFF, ΔΣADC = OFF OSC = OFF, Ta= -40 °C to +125 °C
Operating Current 1_1 (NORMAL Mode)	I_{QVB3_1}	-	2.50	3.75	mA	SHDNB = H, MODE_SEL [1:0] = 2'b01 VREF15 = ON, VREF25 = ON AMP = ON, ΔΣADC = ON OSC = ON, Ta= +25 °C
Operating Current 1_2 (NORMAL Mode)	I_{QVB3_2}	-	2.50	7.50	mA	SHDNB = H, MODE_SEL [1:0] = 2'b01 VREF15 = ON, VREF25 = ON AMP = ON, ΔΣADC = ON OSC = ON, Ta= -40 °C to +125 °C

Electrical Characteristics – continued

(Unless otherwise specified, Ta = -40 °C to +125 °C, VCC = 5.0 V, VDD = 3.3 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Operating Current 2_1 (SLEEP Mode)	$I_{QVB4\_1\_1}$	-	700	1050	µA	SHDNB = H, MODE_SEL [1:0] = 2'b10, SLEEP_INTERVAL [1:0] = 2'b00, SLEEP_SAMPLING_TIME [1:0] = 2'b00, VREF15 = ON, VREF25 = Intermittent Operation AMP = Intermittent Operation, ΔΣADC = Intermittent Operation, OSC = ON, Ta= +25 °C
Operating Current 2_2 (SLEEP Mode)	$I_{QVB4\_1\_2}$	-	700	1250	µA	SHDNB = H, MODE_SEL [1:0] = 2'b10, SLEEP_INTERVAL [1:0] = 2'b00, SLEEP_SAMPLING_TIME [1:0] = 2'b00, VREF15 = ON, VREF25 = Intermittent Operation AMP = Intermittent Operation, ΔΣADC = Intermittent Operation, OSC = ON, Ta= -40 °C to +125 °C
Operating Current 3_1 (SLEEP Mode)	$I_{QVB4\_2\_1}$	-	600	900	µA	SHDNB = H, MODE_SEL [1:0] = 2'b10, SLEEP_INTERVAL [1:0] = 2'b01, SLEEP_SAMPLING_TIME [1:0] = 2'b00, VREF15 = ON, VREF25 = Intermittent Operation AMP = Intermittent Operation, ΔΣADC = Intermittent Operation, OSC = ON, Ta= +25 °C
Operating Current 3_2 (SLEEP Mode)	$I_{QVB4\_2\_2}$	-	600	1100	µA	SHDNB = H, MODE_SEL [1:0] = 2'b10, SLEEP_INTERVAL [1:0] = 2'b01, SLEEP_SAMPLING_TIME [1:0] = 2'b00, VREF15 = ON, VREF25 = Intermittent Operation AMP = Intermittent Operation, ΔΣADC = Intermittent Operation, OSC = ON, Ta= -40 °C to +125 °C
Operating Current 4_1 (SLEEP Mode)	$I_{QVB4\_3\_1}$	-	540	810	µA	SHDNB = H, MODE_SEL [1:0] = 2'b10, SLEEP_INTERVAL [1:0] = 2'b10, SLEEP_SAMPLING_TIME [1:0] = 2'b00, VREF15 = ON, VREF25 = Intermittent Operation AMP = Intermittent Operation, ΔΣADC = Intermittent Operation, OSC = ON, Ta= +25 °C
Operating Current 4_2 (SLEEP Mode)	$I_{QVB4\_3\_2}$	-	540	1010	µA	SHDNB = H, MODE_SEL [1:0] = 2'b10, SLEEP_INTERVAL [1:0] = 2'b10, SLEEP_SAMPLING_TIME [1:0] = 2'b00, VREF15 = ON, VREF25 = Intermittent Operation AMP = Intermittent Operation, ΔΣADC = Intermittent Operation, OSC = ON, Ta= -40 °C to +125 °C
Operating Current 5_1 (SLEEP Mode)	$I_{QVB4\_4\_1}$	-	500	750	µA	SHDNB=H, MODE_SEL[1:0]=2'b10, SLEEP_INTERVAL[1:0]=2'b11, SLEEP_SAMPLING_TIME[1:0]=2'b00, VREF15=ON, VREF25=Intermittent Operation AMP=Intermittent Operation, ΔΣADC=Intermittent Operation, OSC = ON, Ta= +25 °C
Operating Current 5_2 (SLEEP Mode)	$I_{QVB4\_4\_2}$	-	500	950	µA	SHDNB=H, MODE_SEL[1:0]=2'b10, SLEEP_INTERVAL[1:0]=2'b11, SLEEP_SAMPLING_TIME[1:0]=2'b00, VREF15=ON, VREF25=Intermittent Operation AMP=Intermittent Operation, ΔΣADC=Intermittent Operation, OSC = ON, Ta= -40 °C to +125 °C

Electrical Characteristics – continued

(Unless otherwise specified, Ta = -40 °C to +125 °C, VCC = 5.0 V, VDD = 3.3 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
AMP Block						
Analog Input Valtage Range 1	V_{AIN1}	-200	-	+400	mV	AMP_GAIN [1:0] = 2'b00(Gain = 5 V/V)
Analog Input Valtage Range 2	V_{AIN2}	-80	-	+80	mV	AMP_GAIN [1:0] = 2'b01(Gain = 25 V/V) AMP_GAIN [1:0] = 2'b10(Gain = 25 V/V)
Analog Input Valtage Range 3	V_{AIN3}	-40	-	+40	mV	AMP_GAIN [1:0] = 2'b11(Gain = 51 V/V)
Gain Setting Time	$t_{GAINSET}$	-	-	1.5	ms	
ADC Block						
Resolution	-	-	-	16	bit	
ADC Conversion Time 1	t_{CONV1}	0.20	0.25	0.30	ms	MCIC_R [1:0] = 2'b00 (Down sampling value = 32)
ADC Conversion Time 2	t_{CONV2}	0.80	1.00	1.20	ms	MCIC_R [1:0] = 2'b01 (Down sampling value = 128)
ADC Conversion Time 3	t_{CONV3}	1.60	2.00	2.40	ms	MCIC_R [1:0] = 2'b10 (Down sampling value = 256)
ADC Conversion Time 4	t_{CONV4}	6.40	8.00	9.60	ms	MCIC_R [1:0] = 2'b11 (Down sampling value = 1024)
EXADIN Valtage Range	V_{EXADIN}	0.5	-	4.5	V	

(Unless otherwise specified, Ta = -40 °C to +125 °C, VCC = 5.0 V, VDD = 3.3 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
UVLO (VCC)						
VCC UVLO Detect Voltage	V_{CC_UVLOD}	2.700	2.800	2.900	V	VCC = Sweep down
VCC UVLO Release	V_{CC_UVLOR}	2.717	3.000	3.283	V	VCC = Sweep up
UVLO (VREF15)						
VREF15 UVLO Detect Voltage	V_{REF15_UVLOD}	1.352	1.380	1.408	V	VREF15 = Sweep down
UVLO (VDD)						
VDD UVLO Detect Voltage	V_{DD_UVLOD}	1.550	1.700	1.850	V	VDD = Sweep down
VDD UVLO Release	V_{DD_UVLOR}	1.650	1.800	1.950	V	VDD = Sweep up

Electrical Characteristics - continued

(Unless otherwise specified, Ta = -40 °C to +125 °C, VCC = 5.0 V, VDD = 3.3 V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
IO Interface						
SHDNB Input "H" Level	V_{IH_SHDNB}	VCCx0.7	-	VCC+0.3	V	
SHDNB Input "L" Level	V_{IL_SHDNB}	-0.3	-	+VCCx0.3	V	
SHDNB Input Leak Current	I_{OFF_SHDNB}	-1	-	+1	µA	
INTB Output "L" Level Voltage1	V_{OL_INTB1}	0	-	0.4	V	I_O = 1 mA, Ta= +25 °C
INTB Output "L" Level Voltage2	V_{OL_INTB2}	0	-	0.5	V	I_O = 1 mA, Ta= -40 °C to +125 °C
INTB Output Off Leak Current	I_{OLK_INTB}	-1	-	+1	µA	INTB = 5.5 V
ALARMB Output "L" Level Voltage1	$V_{OL\_ALARMB1}$	0	-	0.4	V	I_O = 1 mA, Ta= +25 °C
ALARMB Output "L" Level Voltage2	$V_{OL\_ALARMB2}$	0	-	0.5	V	I_O = 1 mA, Ta= -40 °C to +125 °C
ALARMB Output Off Leak Current	I_{OLK_ALARMB}	-1	-	+1	µA	ALARMB = 5.5 V
SPI Bus Interface						
CSB, SDI, SCK Input "H" Level Voltage	V_{IH_SPI}	VDDx0.7	-	VDD+0.3	V	
CSB, SDI, SCK Input "L" Level Voltage	V_{IL_SPI}	-0.3	-	+VDDx0.3	V	
SDO Output "L" Level Voltage	V_{OL_SDO}	0	-	0.4	V	I_{OL} = 1 mA
SDO Output "H" Level Voltage	V_{OH_SDO}	VDD-0.2	-	VDD	V	I_{OH} = -100 µA
CSB, SDI, SCK Input Leak Current	I_{OLK_SPI}	-1	0	+1	µA	
SDO Output Off Leak Current	I_{OLK_SDO}	-1	0	+1	µA	
CSB-SCK Setup Time	t_{CSS}	1000	-	-	ns	
SCK-CSB Hold Time	t_{CSH}	1000	-	-	ns	
SCK "H" Pulse Width Time	t_{WH}	1000	-	-	ns	
SCK "L" Pulse Width Time	t_{WL}	1000	-	-	ns	
SCK-SDI Setup Time	t_{DIS}	150	-	-	ns	
SCK-SDI Hold Time	t_{DIH}	150	-	-	ns	
SCK-SDO Delay Time	t_{DOD}	-	-	400	ns	
CSB "H" Pulse Width Time	t_{CS}	500	-	-	ns	

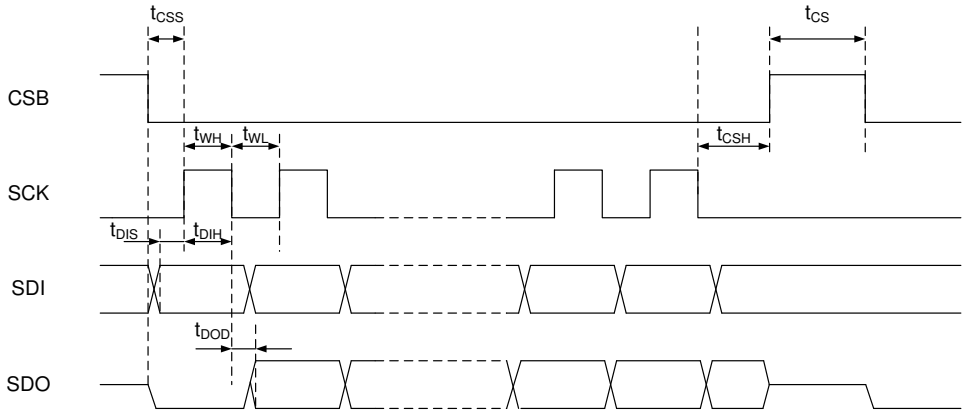


Figure 1. SPI Timing Chart

Typical Performance Curve (Reference Data)

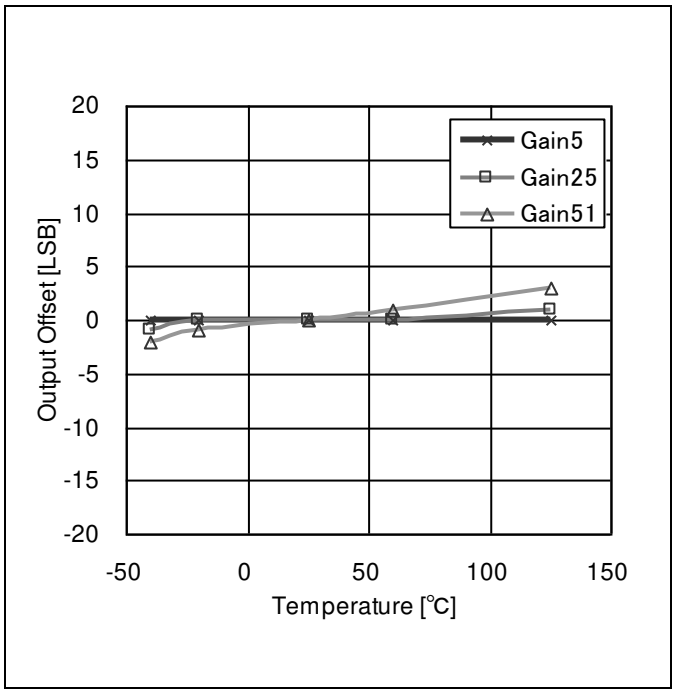


Figure 2. Output Offset vs Temperature
(VCC = 5 V)

Description of Blocks

1. Current Accumulator

1.1 Summary

This product performs accumulation current operation (Coulomb count) by monitoring the battery charge/discharge current. The Coulomb count value obtained is used for battery state-of-charge estimation. It can obtain both the current accumulation level and the current value itself.

1.1.1 Features

·Reading current converted to voltage by an external resistor as a digital value
·Accumulation current counters which monitors the charge/discharge current value
·Independent monitoring of charge and discharge values
·Current value monitoring via SPI
·Fixed-interval average current read function (interval can be adjusted in 4 stages)
·Overwrite function of accumulated current data via SPI I/F

1.1.2 Composition

The Current Accumulator block is comprised of 3 sub-blocks. (See figure 1-1)

Differential op-amp (AMP)

The AMP sub-block monitors the voltage converted by the external resistor R_{SNS} at the INP and INN pins. The voltage difference between INP and INN is then amplified to a voltage suitable for the ΔΣADC input.
Address 00h (AMP_GAIN [1:0]) can be used to adjust voltage amplification gain to 5 V/V, 25 V/V, or 51 V/V. Take note that the input voltage range changes with this gain setting.

ΔΣADC

The 16-bit ΔΣADC has an analog-to-digital conversion rate of 4 kHz using the standard setting.
A digital filter determines the ADC's output rate and frequency response. This filter has 4 settings, accessible through address 00h (MCIC_R [1:0]). Please set an appropriate value considering the influence of the current's frequency response, agitation noise, and the like.

Accumulator

The accumulator operates by using the current value in digital form from the ΔΣADC output.
Chapter 1.3 details the calculation function of the Accumulator, while Chapter 3 describes the interrupt function.

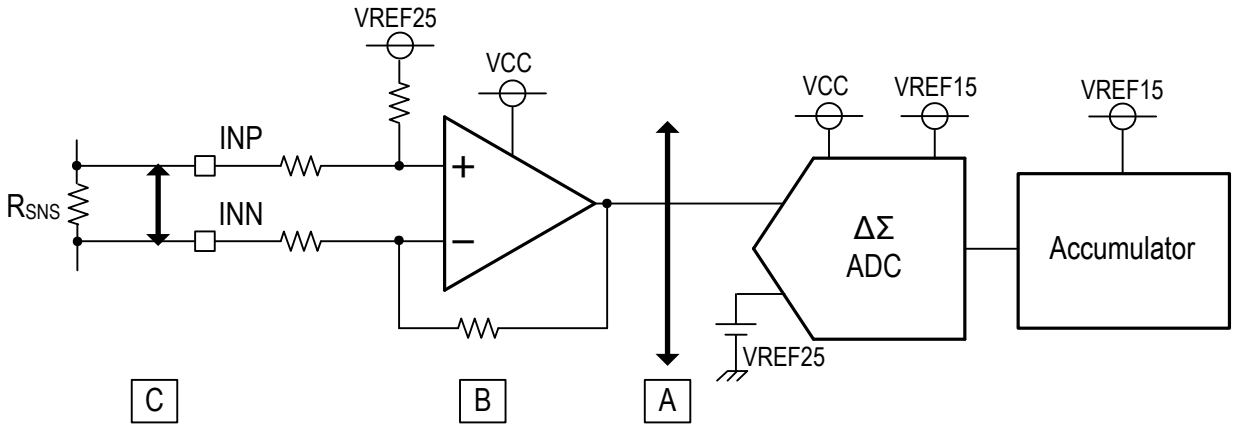


Figure 1-1. Accumulation Current Block Diagram

1.2 Register Structure

Regarding resister structure for current measurement, refer to Figure 1-2.

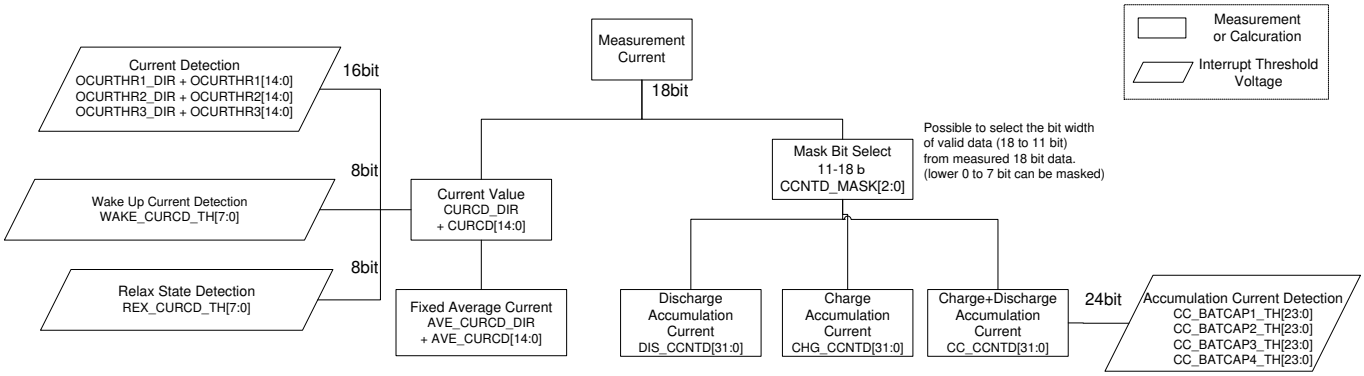


Figure 1-2. Register Structure for Current Measurement

1.3 Function Description

1.3.1 Current Measurement

BD7220FV-C measures current by monitoring the difference in voltage between the ends of the external current sense resistor (R_{SNS}) connected to the differential op-amp inputs INP and INN. The op-amp amplifies the differential input biased on 2.5 V (VREF25) as a reference voltage. The amplified voltage is then used as input to the ΔΣADC. For example, for a difference of 100 mV between the INP and INN pins and a 5 V/V gain setting:

$$2.5\,[\mathrm{V}] + 100\,[\mathrm{mV}] \times 5 = 3.0\,[\mathrm{V}]$$

In this calculation, 3.0 V is input to the ΔΣADC. (ADINP = 3.0 V, ADINM = 2.5 V, ΔV = 0.5 V)

At shipment, the ΔΣADC input voltage is defined as ΔV = 4.5 V. (ADINP=0.25 V to 4.75 V)

$$A{:}\,\Delta\Sigma \quad Input\ \ LSB\ \ Voltage = 4.5 \div 2^{16} \approx \ \pm 68.66455\cdot\cdot\ [\mu\mathrm{V}]$$

The CURCD register indicates the current value and is defined as [sign bit] + [15 bits] based on the computed LSB voltage.

Table 1-1 shows current unit information for each gain setting.
The LSB voltage input for the differential amplifier (Figure 1-1C) is the ΔΣADC input LSB voltage divided by the amplifier gain setting (Figure 1-1B). The current flowing through the sense resistor R_{SNS} is calculated using the 1LSB voltage and the sense resistor value.
The data in Table 1-1 is calculated with the assumption that R_{SNS} = 0.2 mΩ. If, for example, R_{SNS} = 0.1 mΩ, the current value (and, the measurement current range is same) in the table 1-1 is doubled.

Table 1-1. Current Monitor Unit

AMP_GAIN [1:0] register	Gain [times]	ΔΣADC Input 1LSB Voltage [μV]	OPamp Input 1LSB Voltage (INP-INN) [μV]	1LSB Current (@R_{SNS} = 0.2 mΩ) [mA]	OPamp Input Voltage Range [mV]	Available Measurement Current Range (@R_{SNS} = 0.2 mΩ) [A]
2'b00	5	68.66	13.73	68.66	-200 to +400	-1000 to +2000
2'b01, 2'b10	25	68.66	2.75	13.73	±80	±400
2'b11	51	68.66	1.35	6.73	±40	±200

Op-amp input LSB voltage = ΔΣADC input LSB voltage ÷ gain setting value
LSB current = Op-amp input LSB voltage ÷ external current sense resistance (R_{SNS})
Current measurement range = Op-amp input voltage range ÷ external current sense resistance (R_{SNS})

Figure 1-3 shows the structure of the CURCD register.
The MSB indicates the direction of the current and shows a current value using the remaining 15 bits.

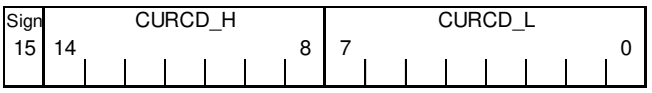


Figure 1-3. CURCD Register

When the current is 100 A, CURCD reads 1C71 [Hex] under the 25 V/V gain setting.

$$100\,[\mathrm{A}] \div 13.7329\,[\mathrm{mA}] \approx 7281.78 \approx 7281\,[\mathrm{DEC}] = 1C71\,[\mathrm{HEX}]$$
$$= 15'h1C71$$

The lower bits that comprise the fractional value will be truncated.

1.3.2 Unit of Accumulation Current

BD7220FV-C can calculate and output accumulation current value based on the measured current. To enable this function, please set the CCNTEN register (address 00h) = 1. (Refer to 1.3.1 Current Measurement) The accumulation current value can be found in the 32-bit register CC_CCNTD. The LSB and MSB values are computed as below. The accumulation current value is calculated with higher precision than the CC_CCNTD register's LSB value.

$$LSB\ for\ internal\ accumulation\ current = current\ LSB\ \times\ (AD\ conversion\ term\ [\mathrm{s}] \div 3600)$$

$$ex.)GAIN = 5:\ \ 68.66\cdot\cdot\ [\mathrm{mA}] \times (250 \times 10^{-6} \div 3600) \approx\ \ 4.77\ [\mathrm{nAh}]$$

$$LSB\ for\ CC_{CCNTD}register = internal\ accumulation\ current\ LSB\ \times internal\ adjustment(6bits)$$

$$ex.)GAIN = 5:\ \ 4.77\ [\mathrm{nAh}] \times 2^6 \approx\ \ 0.3052\ [\mu\mathrm{Ah}]$$

$$MSB\ value\ for\ CC_{CCNTD}register = CC_{CCNTD}register\ LSB \times\ 2^{31} =\ \ 655.36\ [\mathrm{Ah}]$$

Figure 1-4 shows structure of the CC_CCNTD register and approximate accumulation current.

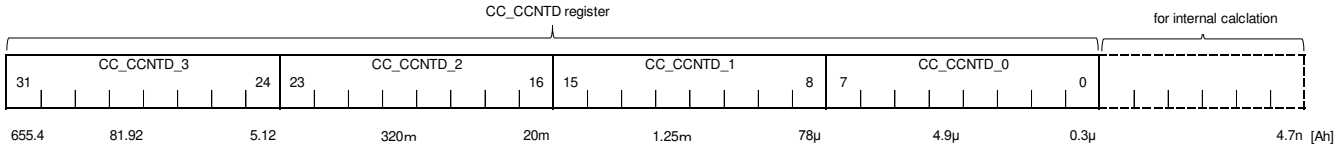


Figure 1-4. Structure of CC_CCNTD Register (CC_UNDIV=0)

To cancel the variation of current LSB in each amplifier gain setting, the current value can be scaled and accumulated in CC_CCNTD register in the logic. This makes the LSB of accumulation current constant regardless of amplifier gain.
For example, when current of 70 mA flows in R_{SNS}, the CURCD register reading is 15'h0001 under a 5 V/V gain setting. Under a 25 V/V setting, CURCD reading is 15'h0005. At 25 V/V gain, not to accumulate 5 times larger from actual value, the logic accumulates the CURCD value divided by 5 to get the equivalent value at 5 V/V gain. At 51 V/V, the divisor is 10.2. The CC_UNDIV register (address 01h) allows the user to enable or disable CURCD value scaling. Using scaling (CC_UNDIV = "0") introduces a small amount of error but allows the user to change three amplifier gain settings. Disabling scaling (CC_UNDIV = "1") requires that the amplifier setting be fixed, but ensures that errors are not introduced. However, the accumulation current capacity changes depending on the gain setting. Comparing to the value of 5 V/V setting, it is 1/5 when the setting is 25 V/V, and 1/10.2 when the setting is 51 V/V. It is possible to write the value of accumulation current into CC_CCNTD resister. Please execute write operation after setting "0" to CCNTEN resister and current accumulating is disabled. When CCNTEN resister is "0", update of accumulation current is discarded.

Table 1-2. Unit of CC_CCNTD Register Accumulation (R_{SNS} = 0.2 mΩ)

	AMP_GAIN [1:0]			
CC_UNDIV = 0 (Variable Gain)	2'b00(5 V/V) 2'b01(25 V/V) 2'b10(25 V/V) 2'b11(51 V/V)	—	—	UNIT
CC_UNDIV = 1 (Fixed Gain)	2'b00(5 V/V)	2'b01(25 V/V) 2'b10(25 V/V)	2'b11(51 V/V)	
Internal Accumulation 1LSB	4.77	0.95	0.47	[nAh]
CC_CCNTD_0 LSB	0.3052	0.0610	0.0299	[µAh]
CC_CCNTD_1 LSB	78.125	15.625	7.659	[µAh]
CC_CCNTD_2 LSB	20.00	4.00	1.96	[mAh]
CC_CCNTD_3 LSB	5.12	1.02	0.50	[Ah]
CC_CCNTD_3 MSB	655.36	131.07	64.25	[Ah]
Maximum Accumulation Current	1310.41	262.08	128.47	[Ah]

Unit of Accumulation Current – continued

In addition, BD7220FV-C can accumulate charging accumulation current (via CHG_CCNTD) and discharging accumulation current (via DIS_CCNTD) separately. Please refer to Figure 1-5 and Figure 1-6 about the structure of CHG_CCNTD and DIS_CCNTD resister and their relationship with CC_CCNTD.
CHG_CCNTD is shifted 2 bits to the left from CC_CCNTD. Accumulation scaling in internal logic for CHG_CCNTD and DIS_CCNTD is the same as in CC_CCNTD, so the unit of accumulation current is the same regardless of the amplifier gain setting. Thus, the value of LSB is greater, but CHG_CCNTD and DIS_CCNTD capacities are 4 times that of CC_CCNTD. The maximum battery capacity of CC_CCNTD is around 1310[Ah], so CHG_CCNTD and DIS_CCNTD can accumulate up to 5240[Ah].

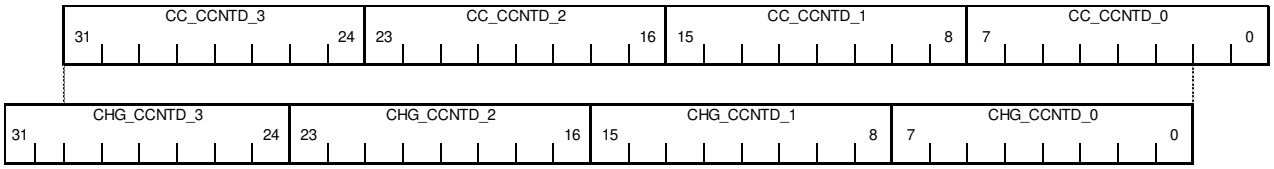


Figure 1-5. Relation between CC_CCNTD and CHG_CCNTD

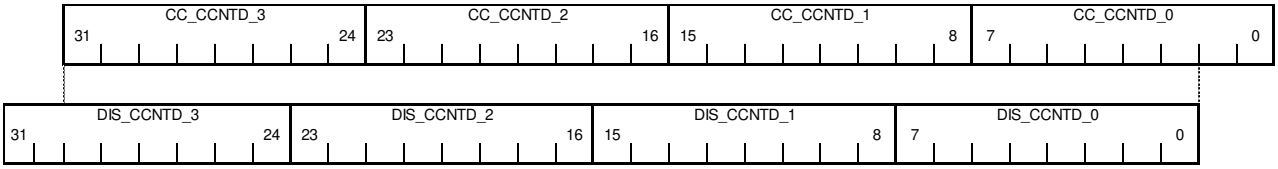


Figure 1-6. Relation between CC_CCNTD and DIS_CCNTD

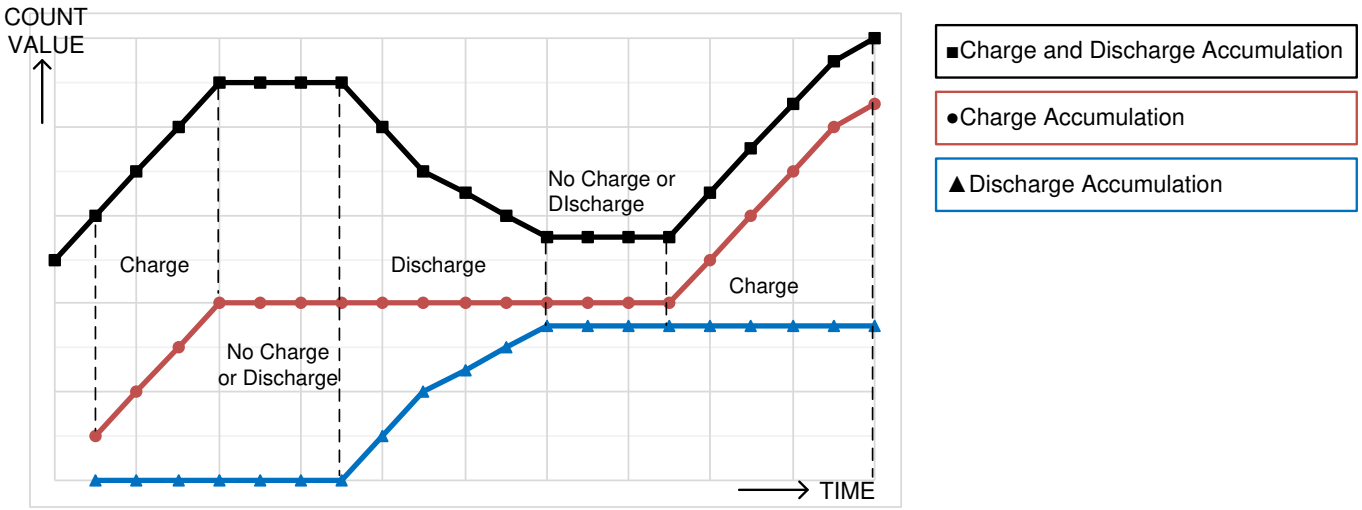


Figure 1-7. Difference between charge accumulation current and charge/discharge accumulation current

The values of CC_CCNTD, CHG_CCNTD and DIS_CCNTD can be cleared by writing “1” to their reset registers. Resetting is valid regardless of the CCNTEN setting. The reset register is automatically cleared to “0” after writing “1”.

Table 1-3. CCNTD Registers and Reset Registers

Register Name	Address	Bit	Bit Name	Function
CC_CCNTD	17h to 1Ah	[7] to [0]	CC_CCNTD [31:0]	Charge and discharge accumulation current
CHG_CCNTD	1Bh to 1Eh	[7] to [0]	CHG_CCNTD [31:0]	Charge accumulation current only
DIS_CCNTD	1Fh to 22h	[7] to [0]	DIS_CCNTD [31:0]	Discharge accumulation current only
CC_TRG_RST_CMD	02h	[0]	CCNTRST	Reset CC_CCNTD
CC_TRG_RST_CMD	02h	[1]	CHG_CCNTD_RST	Reset CHG_CCNTD
CC_TRG_RST_CMD	02h	[2]	DIS_CCNTD_RST	Reset DIS_CCNTD

1.3.3 Fixed-Interval Average Current

BD7220FV-C can output average current at fixed intervals set using registers. Moving average is not used.
The AVE_CURCD_DIR register denotes the current direction and the AVE_CURCD [14:0] register represents the current value. The fixed interval is determined by the ΔΣADC digital filter setting (address 00h: MCIC_R [1:0]), OSR setting (address 01h: OSR [1:0]), and sampling time setting (address 01h: AVE_CURCD_COUNT [1:0]). Table 1-4 contains details regarding the fixed interval setting.
For MCIC_R [1:0] = 2'b00, OSR [1:0] = 2'b00, and AVE_CURCD_COUNT [1:0] = 2'b10, ADC sampling time is 0.25 ms and the fixed interval is 0.25 ms x 64 = 16 ms.

Table 1-4. Fixed interval setting (listed by OSR [1:0] setting)

OSR [1:0] = 2'b00(32) or 2'b11(32)

MCIC_R [1:0]		2'b00(32)	2'b01(128)	2'b10(256)	2'b11(1024)
ADC Conversion Time [ms]		0.25	1	2	8
	Mearsurement Count	Averaging Time[ms]			
AVE_CURCD_COUNT [1:0] = 2'b00	4	1	4	8	32
AVE_CURCD_COUNT [1:0] = 2'b01	16	4	16	32	128
AVE_CURCD_COUNT [1:0] = 2'b10	64	16	64	128	512
AVE_CURCD_COUNT [1:0] = 2'b11	128	32	128	256	1024

(Note) "Averaging Time" = "ADC Conversion Time" x "Muasurement Count"

OSR [1:0] = 2'b01(128)

MCIC_R[1:0]		2'b00(32)	2'b01(128)	2'b10(256)	2'b11(1024)
ADC Conversion Time [ms]		0.25	0.25	0.5	2
	Mearsurement Count	Averaging Time[ms]			
AVE_CURCD_COUNT [1:0] = 2'b00	4	1	1	2	8
AVE_CURCD_COUNT [1:0] = 2'b01	16	4	4	8	32
AVE_CURCD_COUNT [1:0] = 2'b10	64	16	16	32	128
AVE_CURCD_COUNT [1:0] = 2'b11	128	32	32	64	256

(Note) "Averaging Time" = "ADC Conversion Time" x "Muasurement Count"

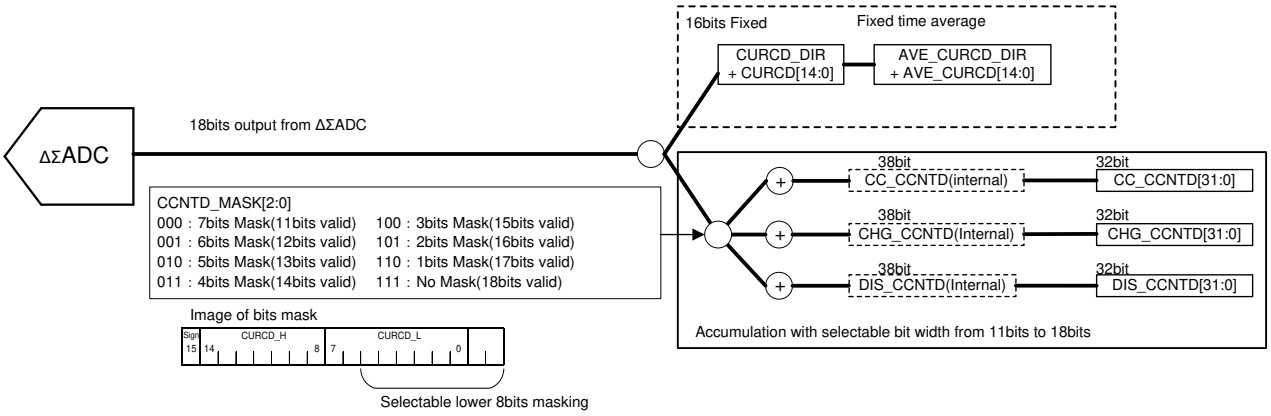
OSR [1:0] = 2'b10(512)

MCIC_R[1:0]		2'b00(32)	2'b01(128)	2'b10(256)	2'b11(1024)
ADC Conversion Time [ms]		0.25	0.25	0.25	0.5
	Mearsurement Count	Averaging Time[ms]			
AVE_CURCD_COUNT [1:0] = 2'b00	4	1	1	1	2
AVE_CURCD_COUNT [1:0] = 2'b01	16	4	4	4	8
AVE_CURCD_COUNT [1:0] = 2'b10	64	16	16	16	32
AVE_CURCD_COUNT [1:0] = 2'b11	128	32	32	32	64

(Note) "Averaging Time" = "ADC Conversion Time" x "Muasurement Count"

1.3.4 Bit Mask Function of Accumulation Current

The current measured by BD7220FV-C is 18 bits valid data and it is stored in the 16 bits CURCD register (see 1.3.1. Current Measurement).In the default setting, 16 bits' width of current value same with CURCD register is accumulated to CC_CCNTD resister, CHG_CCNTD resister and DIS_CCNTD resister, and it can select to mask lower bits of current (fixing lower bits to "0" in accumulation) by setting CCNTD_MASK resister. With this bit mask function, it is possible to reduce the affection from noise in measuring minute current and accumulation.
Note that this function fixing lower bits to "0" in accumulation. This means current is rounded down when sign is positive, and current is rounded up when sign is negative since it is expressed by two's complement. And, complement by user's MCU is recommended, because accumulation current has constant error following to mask lower bits of current. (see next page)
Note that this function affects only the accumulation from CURCD to CC_CCNTD/CHG_CCNTD/DIS_CCNTD. This does not affect CURCD itself. CURCD does not have bit mask function and so always contains the full 16 bits of data.



Example of Internal 18bits valid data

Sign	bit[17]sign	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Current Data[dec] No Bit Mask	Current Data[dec] 2Bits Mask
Positive sign	0	1	0	0	0	0	16	16
	0	0	1	1	1	1	15	12
	0	0	1	1	1	0	14	12
	0	0	1	1	0	1	13	12
	0	0	1	1	0	0	12	12
	0	0	1	0	1	1	11	8
	0	0	1	0	1	0	10	8
	0	0	1	0	0	1	9	8
	0	0	1	0	0	0	8	8
	0	0	0	1	1	1	7	4
	0	0	0	1	1	0	6	4
	0	0	0	1	0	1	5	4
	0	0	0	1	0	0	4	4
	0	0	0	0	1	1	3	0
	0	0	0	0	1	0	2	0
	0	0	0	0	0	1	1	0
	0	0	0	0	0	0	0	0
Negative sign = two's complement	1	1	1	1	1	1	-1	-4
	1	1	1	1	1	0	-2	-4
	1	1	1	1	0	1	-3	-4
	1	1	1	1	0	0	-4	-4
	1	1	1	0	1	1	-5	-8
	1	1	1	0	1	0	-6	-8
	1	1	1	0	0	1	-7	-8
	1	1	1	0	0	0	-8	-8
	1	1	0	1	1	1	-9	-12
	1	1	0	1	1	0	-10	-12
	1	1	0	1	0	1	-11	-12
	1	1	0	1	0	0	-12	-12
	1	1	0	0	1	1	-13	-16
	1	1	0	0	1	0	-14	-16
	1	1	0	0	0	1	-15	-16
	1	1	0	0	0	0	-16	-16

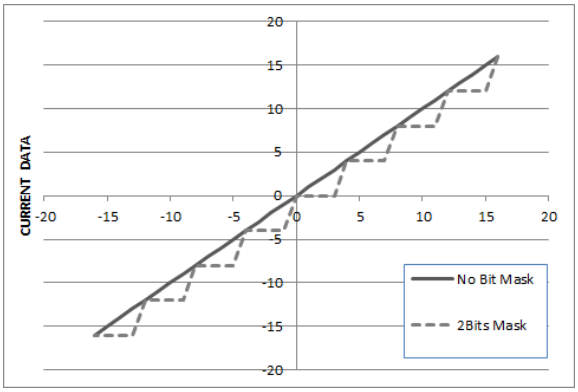


Figure 1-8. Bit Mask Function of Accumulation Current

1.3.4 Bit Mask Function of Accumulation Current - continued

This is the example of CCNTD error complement with bit mask function.

(1) Adding manual offset to CURCD

In the case that measuring minute current value is less than ±1LSB of bit mask, positive sign current data becomes zero and negative sign current data becomes –LSB with bit mask function. Adding manual offset (OFST10: address0Bh) to shift CURCD only positive sign data, current data becomes zero and it saves unintended current accumulation with measuring minute current. But it needs CCNTD error complement, because this offset is added constantly.

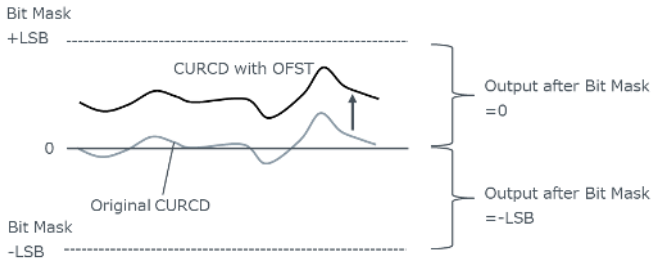


Figure 1-9. Image of Adding Manual Offset to CURCD

(2) Adding error complement to CCNTD

Below is the formula of CCNTD error complement for (1) CURCD manual offset and for increasing lower bits of bit mask function.

Table 1-5. Formula of CCNTD Error Complement

item	Resistor	Formula of Error Complement
Complement of CURCD manual offset	CC_CCNTD	{ −OFST × (TC / AD_conversion_term) / internal_bits_adjustment } = { −OFST × 4000 / 2^6 }
	CHG_CCNTD	{ −OFST × (TC / AD_conversion_term) / internal_bits_adjustment } = { −OFST × 4000 / (2^6 / 2^2) }
	DIS_CCNTD	{ −OFST × (TC / AD_conversion_term) / internal_bits_adjustment } = { −OFST × 4000 / (2^6 / 2^2) }
Complement of bit mask function	CC_CCNTD	{ 2^{N-3} × (TC / AD_conversion_term) / internal_bits_adjustment } = { 2^{N-3} × 4000 / 2^6 }
	CHG_CCNTD	{ 2^{N-3} × (TC / AD_conversion_term) / internal_bits_adjustment } = { 2^{N-3} × 4000 / (2^6 / 2^2) }
	DIS_CCNTD	{ 2^{N-3} × (TC / AD_conversion_term) / internal_bits_adjustment } = { 2^{N-3} × 4000 / (2^6 / 2^2) }

(Note) OFST: Manual Offset Value, TC: CCNTD Read Term, N: Bit Mask Width

(Note) Condition: N > 2, CC_UNDIV=1, CCNTD Read Term = 1 [s]

1.3.5 Setting of ΔΣADC Digital Filter

The ΔΣADC digital filter can be set to one of four filter characteristics depending on the purpose. Using the wideband filter makes it possible to measure steep current changes. While this is not possible using the narrowband filter, using the narrowband filter helps suppress environmental noise.
The characteristic of the Digital Filter is changed using MCIC_R register (address 00h MCIC_R [1:0]). Because the conversion time depends on the MCIC_R register setting, attention is necessary. (Refer to Table 1-6, Table 1-7)

ADC sampling period (AD_SAMP)
-Time to convert 1 sampling. The average current of this period is output to CURCD register, and accumulated to CC_CCNTD register.

ADC conversion latency (AD_LATE) consists of the following wait times.
-Transaction time from OFF to ON in intermittent action
-Reshuffle time for EXADIN pin input voltage measurement action
-After calibration, time to convert initial data from ΔΣADC startup condition
During this period, it cannot output measurement current.

Table 1-6. ADC Sampling Period [ms] (MCIC_R [1:0] / OSR [1:0])

Address 00h MCIC_R[1:0]	Address 01h OSR[1:0]		
	2'b00(32) 2'b11(32)	2'b01(128)	2'b10(512)
2'b11(1024)	8	2	0.5
2'b10(256)	2	0.5	0.25
2'b01(128)	1	0.25	0.25
2'b00(32)	0.25	0.25	0.25

Table 1-7. ADC Conversion Latency [ms] (MCIC_R [1:0] / OSR [1:0])

Address 00h MCIC_R [1:0]	Address 01h OSR [1:0]		
	2'b00(32) 2'b11(32)	2'b01(128)	2'b10(512)
2'b11(1024)	96.5	24.5	6.5
2'b10(256)	24.5	6.5	2.5
2'b01(128)	12.5	3.5	1.5
2'b00(32)	3.5	1.5	1.5

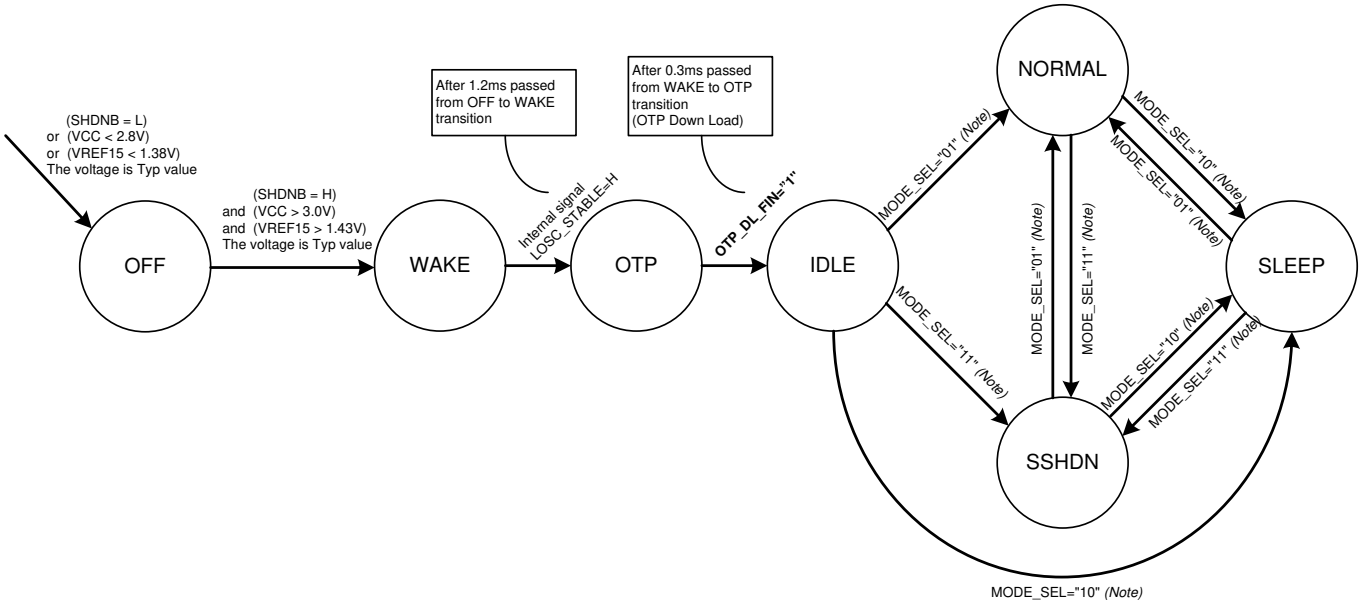
2. Operation Modes

2.1 Features

・Automatic power on by supplying input voltage (VCC)
・Recall of OTP memory automatically in power on sequence
・High accuracy of calculation and accumulation of current in the Normal mode
・Low current consumption thanks to intermittent operation of AMP and ΔΣADC in SLEEP mode
(The timing of the intermittent operation and ON time duration can be set by register)
・Retention of internal registers in SSHDN mode
・SHDNB pin which can turn all blocks off (OFF state, data in internal registers are cleared)

2.2 Structure

BD7220FV-C starts to operate as soon as input power is supplied.
After the reference voltage turns on (WAKE), OTP settings (including calibration settings) are recalled. Then, BD7220FV-C becomes ready for SPI communication (IDLE). With finished recall from OTP, “1” is set to OTP_DL_FIN register. There are three other operating modes from the IDLE state. Using SPI commands, it is possible to freely change between these modes.



(Note) VDD > 2.5V is required to input SPI commands.

Figure 2-1. Operating Modes Transition Diagram

Operating Modes Transition Diagram and Modes Structure - continued

NORMAL mode (MODE_SEL [1:0] = “01”)

AMP and ΔΣADC are ON in this mode. The current is measured and the value is accumulated continuously with high accuracy.

SLEEP mode (MODE_SEL [1:0] = “10”)

AMP, ΔΣADC and VREF25 operate intermittently and the current consumption is reduced. The current cannot be measured during off time but the accumulation error can be reduced by accumulating a certain fixed value during off time. Using the SLEEP_CC_SEL register, the fixed accumulation value can be set to:

- Average current measured during ON time
- Last measured current during ON time

This mode is valid for systems when current do not change frequently. Please refer to the Figure 2-3 for the detailed operation timing.

During intermittent operation, ON time to OFF time ratio in an intermittent period can be set through SLEEP_INTERVAL (03h CC_SET3 [3:2]), and the number of measurement times in ON time can be set through SLEEP_SAMPLING_TIME [1:0] (03h CC_SET3 [5:4]). Each register has 4 settings. Note that as the number of measurement times increase by setting SLEEP_SAMPLING_TIME register, ON time is extended proportionally.

SSHDN mode (MODE_SEL [1:0] = “11”)

Only VREF15, power supply for internal digital circuit, is ON. Internal register settings can be retained by VREF15. Current consumption of BD7220FV-C can be minimized in SSHDN as all blocks other than VREF15 are turned off.

Table 2-1 describes which blocks are turned ON and OFF in each operating mode.

Table 2-1. State of Blocks under each Operating Mode

MODE	MODE_SEL[1:0]	SHDNB (Pin)	VREF15	VREF25	AMP	ΔΣADC	OSC (8.192MHz)	SPI access
OFF (VCC < 2.8V)	-	-	OFF	OFF	OFF	OFF	OFF	Invalid
OFF (SHDNB = L)	-	L	OFF	OFF	OFF	OFF	OFF	Invalid
WAKE (Reference Wake-up)	-	H	ON	OFF	OFF	OFF	ON	Invalid
OTP (OTP Auto Loading)	-	H	ON	OFF	OFF	OFF	ON	Invalid
IDLE	-	H	ON	OFF	OFF	OFF	ON	Valid
NORMAL	2'b01	H	ON	ON	ON	ON	ON	Valid
SLEEP	2'b10	H	ON	Inter-mittent	Inter-mittent	Inter-mittent	ON	Valid
SSHDN (Soft Shutdown)	2'b11	H	ON	OFF	OFF	OFF	OFF	Valid

2.3 Function Description

2.3.1 NORMAL Mode

BD7220FV-C enters NORMAL mode when MODE_SEL [1:0] (00h CC_SET1 [1:0]) is set to “01”. VREF25, AMP, ΔΣADC and OSC turn on and start current measurement when in Normal mode. The actual time for current measurement from writing to the register depends on INI_WAIT [1:0], MCIC_R [1:0] and OSR [1:0] settings.
The INI_WAIT register configures the time delay for VREF25 and AMP startup. The lead time for initial data conversion after ΔΣADC turns on is set by the MCIC_R and OSR registers. Please refer to Table 1-6.
When INI_WAIT [1:0] = 2’b00 (1.5 ms), MCIC_R [1:0] = 2’b00 (down sampling value = 32), and OSR [1:0] = 2’b00, the actual lead time to measure current is 5.0 ms.
To enable the function for accumulating current, “1” needs to be written to CCNTEN. The current can be measured and CURCD register is updated even when the CCNTEN register value is “0”, but CC_CCNTD, CHG_CCNTD and DIS_CCNTD registers are not updated.

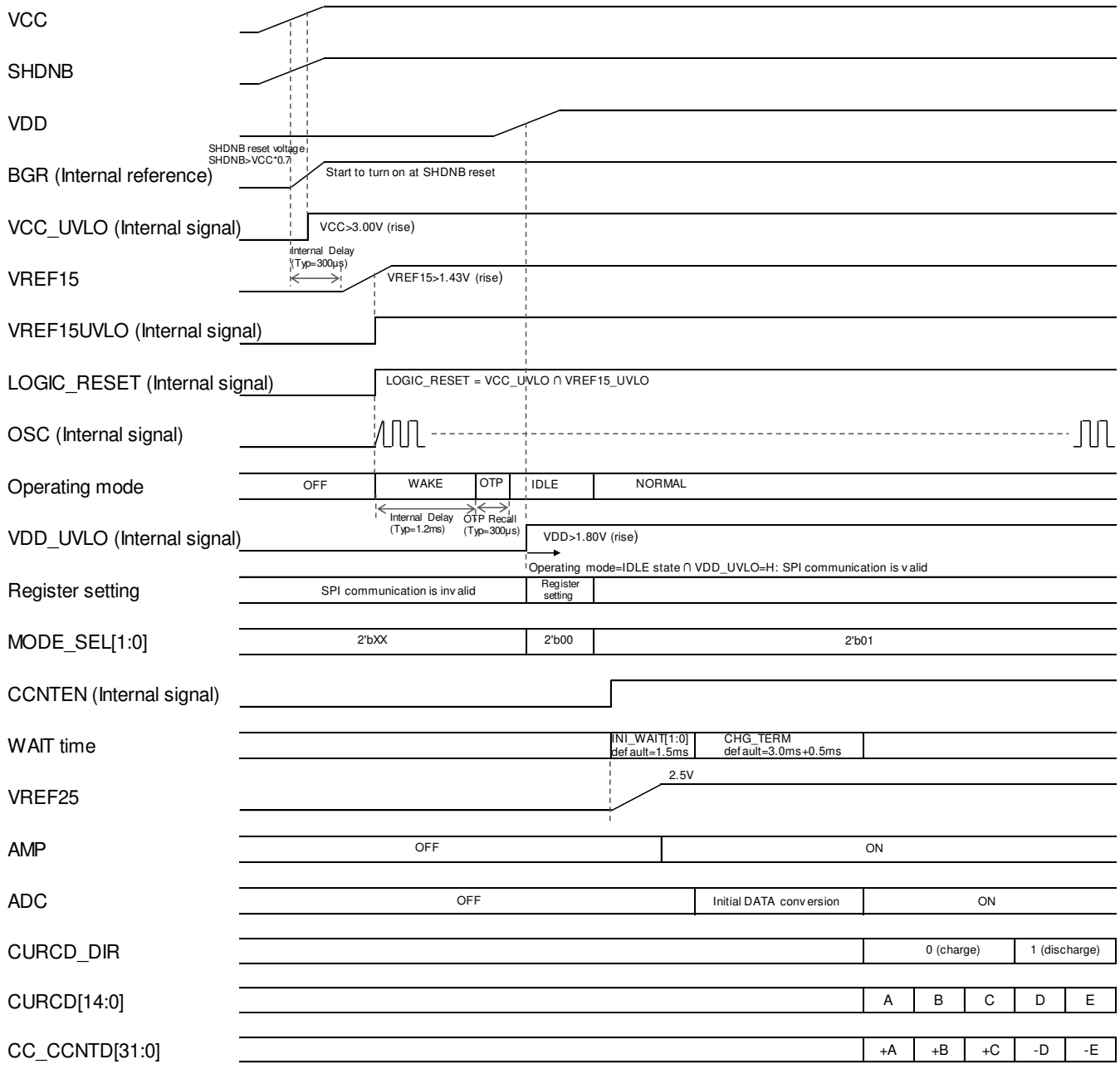


Figure 2-2. OFF to Normal Mode Power ON Sequence

2.3.2 SLEEP Mode

The BD7220FV-C enters SLEEP mode when “10” is written to MODE_SEL [1:0] (00h CC_SET1 [1:0]). In SLEEP mode, the current consumption can be reduced since VREF25, AMP, and ΔΣADC operate intermittently. The timing of intermittent operation can be configured using the SLEEP_INTERVAL register. All available ratios of ON time to OFF time in intermittent operation are listed in Table 2-2.

Table 2-2. Ratio of ON Time to OFF Time in Intermittent Operation in SLEEP Mode

	ON Time	OFF Time
SLEEP_INTERVAL [1:0]=2'b00	1	7
SLEEP_INTERVAL [1:0]=2'b01	1	15
SLEEP_INTERVAL [1:0]=2'b10	1	31
SLEEP_INTERVAL [1:0]=2'b11	1	127

※Ratio when ON time is taken as '1'

The ON time during intermittent operation is calculated by the following formula:

$$ON\ time = INI\_WAIT + AD\_LATE + (ADC\_SAMP \times SLEEP\_SAMPLING\_TIME)$$

INI_WAIT [1:0] (38h):
This is the wait time for VREF25 and AMP startup. The wait time is configurable from 1.5 ms (default) to 12 ms.

AD_LATE (ADC conversion latency):
This is the wait time before outputting digital conversion value after a signal is input into the ADC. It is configured by the digital filter (MCIC_R) and OSR settings. For details, please refer to Table 1-6.

AD_SAMP (ADC sampling period):
This is the time required for one AD conversion. It is configured by the digital filter (MCIC_R) and OSR settings. For details, please refer to Table 1-5.

SLEEP_SAMPLING_TIME [1:0] (03h):
This register determines how many times current measurement is done during ON time of intermittent operation. The number is configured by the digital filter (MCIC_R) and OSR settings. For details, please refer to Table 2-3.

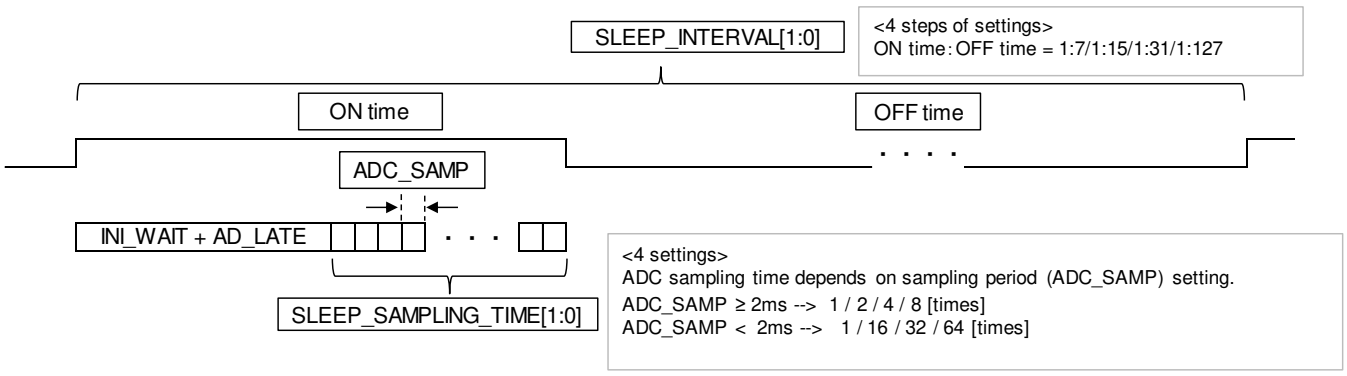


Figure 2-3. Intermittent Operation in SLEEP Mode

ON time and OFF time in default settings are calculated as following;

$$ON\ time = 1.5\ [\text{ms}] + 3.5\ [\text{ms}] + (250\ [\mu\text{s}] \times 1\ time) = 5.25\ [\text{ms}]$$
$$OFF\ time = 5.25\ [\text{ms}] \times 7\ times = 36.75\ [\text{ms}]$$

SLEEP Mode – continued

Table 2-3. Measurement Count during Intermittent Operation (ON Time) in SLEEP Mode

OSR[1:0] = 2'b00(32) or 2'b11(32)

MCIC_R[1:0]	2'b00(32)	2'b01(128)	2'b10(256)	2'b11(1024)
ADC Conversion Time[ms]	0.25	1	2	8
	Measurement Count [times]			
SLEEP_SAMPLING_TIME[1:0] = 2'b00	1	1	1	1
SLEEP_SAMPLING_TIME[1:0] = 2'b01	16	16	2	2
SLEEP_SAMPLING_TIME[1:0] = 2'b10	32	32	4	4
SLEEP_SAMPLING_TIME[1:0] = 2'b11	64	64	8	8

OSR[1:0] = 2'b01(128)

MCIC_R[1:0]	2'b00(32)	2'b01(128)	2'b10(256)	2'b11(1024)
ADC Conversion Time[ms]	0.25	0.25	0.5	2
	Measurement Count [times]			
SLEEP_SAMPLING_TIME[1:0] = 2'b00	1	1	1	1
SLEEP_SAMPLING_TIME[1:0] = 2'b01	16	16	16	2
SLEEP_SAMPLING_TIME[1:0] = 2'b10	32	32	32	4
SLEEP_SAMPLING_TIME[1:0] = 2'b11	64	64	64	8

OSR[1:0] = 2'b10(512)

MCIC_R[1:0]	2'b00(32)	2'b01(128)	2'b10(256)	2'b11(1024)
ADC Conversion Time[ms]	0.25	0.25	0.25	0.5
	Measurement Count [times]			
SLEEP_SAMPLING_TIME[1:0] = 2'b00	1	1	1	1
SLEEP_SAMPLING_TIME[1:0] = 2'b01	16	16	16	16
SLEEP_SAMPLING_TIME[1:0] = 2'b10	32	32	32	32
SLEEP_SAMPLING_TIME[1:0] = 2'b11	64	64	64	64

In SLEEP mode, current measurement is enabled only during ON time. Current is never measured during OFF time (VREF25, APM, and ΔΣADC are OFF) but a fixed current value configured by the SLEEP_CC_SEL register is accumulated. The values of related registers are updated as below.

CURCD:
The current value measured just before turning off is retained. The register value is not updated.

CC_CCNTD, CHG_CCNTD, DIS_CCNTD:
The current value measured in ON time is accumulated during OFF time.
Average value of current measured during ON time or the last value of ON time can be selected as the current value to be accumulated, using the SLEEP_CC_SEL register (03h CC_SET3 [6]).

SLEEP_CC_SEL (03h):
0: The last measured current during the previous ON time is accumulated during OFF time.
1: Average current measured during ON time is accumulated during OFF time.

Please don't change the configuration of the registers related to ON time / OFF time setting (INI_WAIT, MCIC_R, OSR, SLEEP_SAMPLING_TIME, SLEEP_INTERVAL) and SLEEP_CC_SEL in SLEEP mode operating.

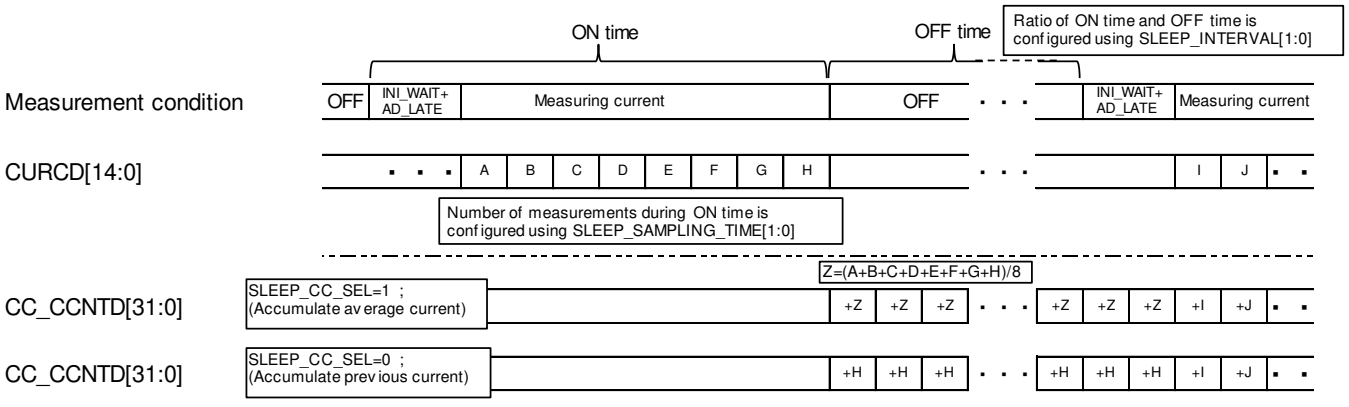


Figure 2-4. Accumulation Current during OFF Time

2.3.3 SSHDN Mode

BD7220FV-C enters SSHDN mode when “11” is written to MODE_SEL [1:0] (00h CC_SET1 [1:0]).
In SSHDN mode, the minimum function blocks to retain register settings are turned on. For details, please refer to Table 2-1. The CURCD register which shows current value is reset to “0” but the CCNTD register which shows accumulation current keeps the value measured at the end.

2.3.4 OFF State

BD7220FV-C is turned off when the SHDNB pin is in “L” state.
In OFF state, all blocks are turned off and the current consumption is at minimum. Note that register settings are cleared and OTP settings are recalled at next power on. The register value of calibration needs to be written again. (Refer to section 4.2.1.)
Finished to recall from OTP at restart from OFF state, “1” is set to OTP_DL_FIN register. The data set to OTP_DL_FIN register is latched and cleared by writing “1” to it. So, to clear OTP_DL_FIN register after startup and monitoring the register value regularly enables to detect unexpected reset of BD7220FV-C.

3. Interrupts

3.1 Summary

6 types of interrupt can be generated through the open-drain INTB pin. All interrupt settings can be masked or unmasked through the register settings.

3.1.1 Features

- 4 types of threshold can be configured for interrupt by the accumulation current [CC_CCNTD]
- 3 types of threshold can be configured for interrupt by the measured current [CURCD]
- Interrupt by the current the configured threshold or more
- Interrupt by detecting battery relaxation
- Interrupt by SPI CRC error detection
- Interrupt by completing the calibration

3.1.2 Structure

BD7220FV-C can generate interrupt signals from multiple sources by asserting the INTB pin low. Each interrupt source has associated status register and enable register. The status register indicates the status of each interrupt source and the enable register allows to output the interruption to the external open drain pin “INTB”.

Regardless of the setting of its enable register, status register corresponding to the source of interrupt is set “1” when detecting each interrupt source event. The status register is latched and is not cleared automatically even if released from the interrupt source. To clear the enable register, write “1” to the register. Only the enabled interrupt event can assert the INTB pin low and announcing the interrupt occurred.

The INTB pin is kept asserted low until all enabled status registers are cleared when multiple interrupt sources occur. The INTB pin goes into Hi-z state when all enabled status registers are cleared. As “0” written in status registers is ignored, write “0” in other bits to clear only one interrupt source.

After power on or restart from OFF state, all status registers are “0” (non-detected) and all enable registers are “0” (interrupt assertion to the INTB pin is disabled). To enable interrupt assertion, configure the interrupt function by SPI.

Please refer to the Table 3-1 for more details about interrupt registers.

3.2 Register Descriptions

The list of interrupt registers are as follows.

Table 3-1. List of Interrupt Registers

Register Name	Bit Name	Function	Register Map			
			Enable		Status/Clear	
			Address	bit	Address	bit
INT_REQ1	CC_MON1_DET	Detection of Charging Current Accumulation Value1 (Threshold Setting)	39h	0	3Ch	0
INT_REQ1	CC_MON1_RES	Detection of Discharging Current Accumulation Value1 (Threshold Setting)	39h	1	3Ch	1
INT_REQ1	CC_MON2_DET	Detection of Charging Current Accumulation Value2 (Threshold Setting)	39h	2	3Ch	2
INT_REQ1	CC_MON2_RES	Detection of Discharging Current Accumulation Value2 (Threshold Setting)	39h	3	3Ch	3
INT_REQ1	CC_MON3_DET	Detection of Charging Current Accumulation Value3 (Threshold Setting)	39h	4	3Ch	4
INT_REQ1	CC_MON3_RES	Detection of Discharging Current Accumulation Value3 (Threshold Setting)	39h	5	3Ch	5
INT_REQ1	CC_MON4_DET	Detection of Charging Current Accumulation Value4 (Threshold Setting)	39h	6	3Ch	6
INT_REQ1	CC_MON4_RES	Detection of Discharging Current Accumulation Value4 (Threshold Setting)	39h	7	3Ch	7
INT_REQ2	ALARM_OCUR1_DET	Alarm Output for Detection of Charging Current (ALARMB Terminal Output for OCUR1_DET)	3Ah	0	3Dh	2
INT_REQ2	ALARM_OCUR1_RES	Alarm Output for Detection of Discharging Current (ALARMB Terminal Output for OCUR1_RES)	3Ah	1	3Dh	3
INT_REQ2	OCUR1_DET	Detection of Charging Current1 (Threshold/Number of Detection Setting)	3Ah	2	3Dh	2
INT_REQ2	OCUR1_RES	Detection of Discharging Current1 (Threshold/Number of Detection Setting)	3Ah	3	3Dh	3
INT_REQ2	OCUR2_DET	Detection of Charging Current2 (Threshold/Number of Detection Setting)	3Ah	4	3Dh	4
INT_REQ2	OCUR2_RES	Detection of Discharging Current2 (Threshold/Number of Detection Setting)	3Ah	5	3Dh	5
INT_REQ2	OCUR3_DET	Detection of Charging Current3 (Threshold/Number of Detection Setting)	3Ah	6	3Dh	6
INT_REQ2	OCUR3_RES	Detection of Discharging Current3 (Threshold/Number of Detection Setting)	3Ah	7	3Dh	7
INT_REQ3	WAKE_DET	Detection of Over Wake-Up Current (Threshold/Number of Detection Setting)	3Bh	0	3Eh	0
INT_REQ3	WAKE_RES	Detection of Under Wake-Up Current (Threshold/Number of Detection Setting)	3Bh	1	3Eh	1
INT_REQ3	REX_DET	Detection of Relax State (Threshold/Time of Detection Setting)	3Bh	2	3Eh	2
INT_REQ3	CRCERR_DET	Detection of CRC Error	3Bh	4	3Eh	4
INT_REQ3	CALIB_FIN	Detection of Calibration Finish	3Bh	6	3Eh	6

(Note) Inside () indicate configurable parameters

3.3 Function Description

3.3.1 Interrupt by Accumulation Current

Interrupt can be generated by detecting the configured threshold crossing to the accumulation current measurement (CC_CCNTD). 4 thresholds can be configured through CC_BATCAP#_TH (# = 1 to 4). CC_BATCAP#_TH are 24-bit registers those are compared to the upper 24 bits (out of 32) of CC_CCNTD.

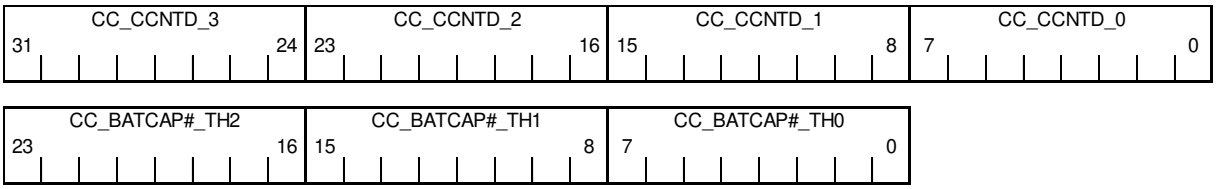


Figure 3-1. Relationship between CC_CCNTD and CC_BAT_CAP_TH

(When CC_UNDIV = 0: scaling in every gain setting is enabled)
LSB of CC_BATCAP1_TH = 78.125 μAh
MSB of CC_BATCAP1_TH = 655.36 Ah

When CC_UNDIV=1: scaling in every gain setting is disabled and in that case LSB / MSB varies.
For example, the threshold of the accumulation current is configured to 1Ah, register value is as below.

$$1[\text{Ah}] \ / \ 78.125[\mu\text{Ah}] \ = \ 12800 \ => \ CC\_BATCAP1\_TH[23:0] \ = \ 24'h003200(24'd12800)$$

Please refer to section 1.3.2 for more details about CC_CCNTD.

Table 3-2. The List of Accumulation Current and Threshold Registers

Address	Register Name	Description
17h to 1Ah	CC_CCNTD [31:0]	Accumulated Current Value
23h to 25h	CC_BATCAP1_TH [23:0]	Interrupt Threshold for Current Accumulation 1 It is compared with the upper 24 bits [31:8] in CC_CCNTD [31:0] register.
26h to 28h	CC_BATCAP2_TH [23:0]	Interrupt Threshold for Current Accumulation 2 It is compared with the upper 24 bits [31:8] in CC_CCNTD [31:0] register.
29h to 2Bh	CC_BATCAP3_TH [23:0]	Interrupt Threshold for Current Accumulation 3 It is compared with the upper 24 bits [31:8] in CC_CCNTD [31:0] register.
2Ch to 2Eh	CC_BATCAP4_TH [23:0]	Interrupt Threshold for Current Accumulation 4 It is compared with the upper 24 bits [31:8] in CC_CCNTD [31:0] register.

3.3.2 Interrupt for Current Measurement

Interrupt can be generated by detecting the configured threshold crossing for current measurement (CURCD). 3 thresholds can be configured through OCURTHR#_DIR (# = 1 to 3) and OCURTHR# (# = 1 to 3). OCURTHR# is a 15-bit register that is compared to the 15 bits of CURCD. OCURDUR# (# = 1 to 3) configures the number of consecutive detections required to generate the interrupt. For example, if set to 4 times, an interrupt is generated only after 4 consecutive detections. The counter starts over from 0 if enough time passes without reaching the set number of consecutive detections.

Only specific to OCURTHR1, interrupts can also be notified through the dedicated ALARMB pin. Unlike interrupt notifications through INTB, the ALARMB interrupt source can be easily identified even without checking the status registers.

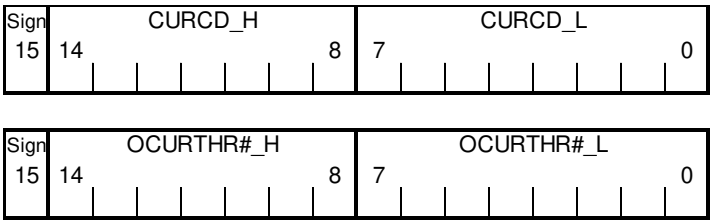


Figure 3-2. Relationship of CURCD and OCURTHR

Table 3-3. List of Current Detection Interrupt Setting Registers

Address	Register Name	Description
13h	CURCD_DIR	Current Direction (0:charging 1:discharging)
13h to 14h	CURCD [14:0]	Measured Current Value
2Fh	OCURTHR1_DIR	OCURTHR1 [14:0] Current Direction(0:charging 1:discharging)
2Fh to 30h	OCURTHR1 [14:0]	Interrupt Threshold for Current Measurment 1
31h	OCURTHR2_DIR	OCURTHR2 [14:0] Current Direction(0:charging 1:discharging)
31h to 32h	OCURTHR2 [14:0]	Interrupt Threshold for Current Measurment 2
33h	OCURTHR3_DIR	OCURTHR3 [14:0] Current Direction(0:charging 1:discharging)
33h to 34h	OCURTHR3 [14:0]	Interrupt Threshold for Current Measurment 3
35h	OCURDUR1 [1:0]	Crossing Detection Threshold for OCURTHR1 (00: 1 time, 01: 4 times, 10: 8 times, 11: 16 times)
35h	OCURDUR2 [1:0]	Crossing Detection Threshold for OCURTHR2 (00: 1 time, 01: 4 times, 10: 8 times, 11: 16 times)
35h	OCURDUR3 [1:0]	Crossing Detection Threshold for OCURTHR3 (00: 1 time, 01: 4 times, 10: 8 times, 11: 16 times)

3.3.3 Interrupt by Battery Relaxation and Wakeup Current Detection

Relaxation state Interrupt can be generated when a relaxation state of the battery is detected. The detection threshold can be configured through REX_CURCD_TH. REX_CURCD_TH is an 8-bit register and set to the lower 8 bits (out of 15) of CURCD. REX_CURCD_TH cannot be set the CURCD_DIR register indicate the sign of the current value. A Relax Timer starts counting up when REX_CURCD_TH is set to 100 mA and the value of CURCD is within -100 mA to +100 mA. The counter resets once the current increases higher than the threshold. REX_EN should be set to "1" to enable the Relax Timer. Writing "0" to the REX_EN stops the timer and resets the timer counter to "0". Once the Relax Timer is expired and the counter needs to be reset, writing REX_EN = 1→0→1 is required. Relax timer detect time can be configured in 4 steps from 30 min to 120 min through the REX_DUR register. Relaxation state interrupt is generated when relax timer is over the detect time.

Wakeup current interrupt is generated when an occurrence of charge or discharge current toward the battery is detected. The detection threshold can be configured through WAKE_CURCD_TH an 8-bit register which is set to the lower 8 bits (out of 15) of CURCD. WAKE_CURCD_TH cannot be set the CURCD_DIR register indicate the sign of the current value. An interrupt is generated when WAKE_CURCD_TH is set to 100 mA and the value of CURCD is less than -100 mA or greater than +100 mA. The WAKE_COUNT register configures the number of consecutive detections required to generate the interrupt. For example, if set to 4 times, an interrupt is generated only after 4 consecutive detections are detected. The counter starts over from 0 if enough time passes without reaching the set number of consecutive detections.

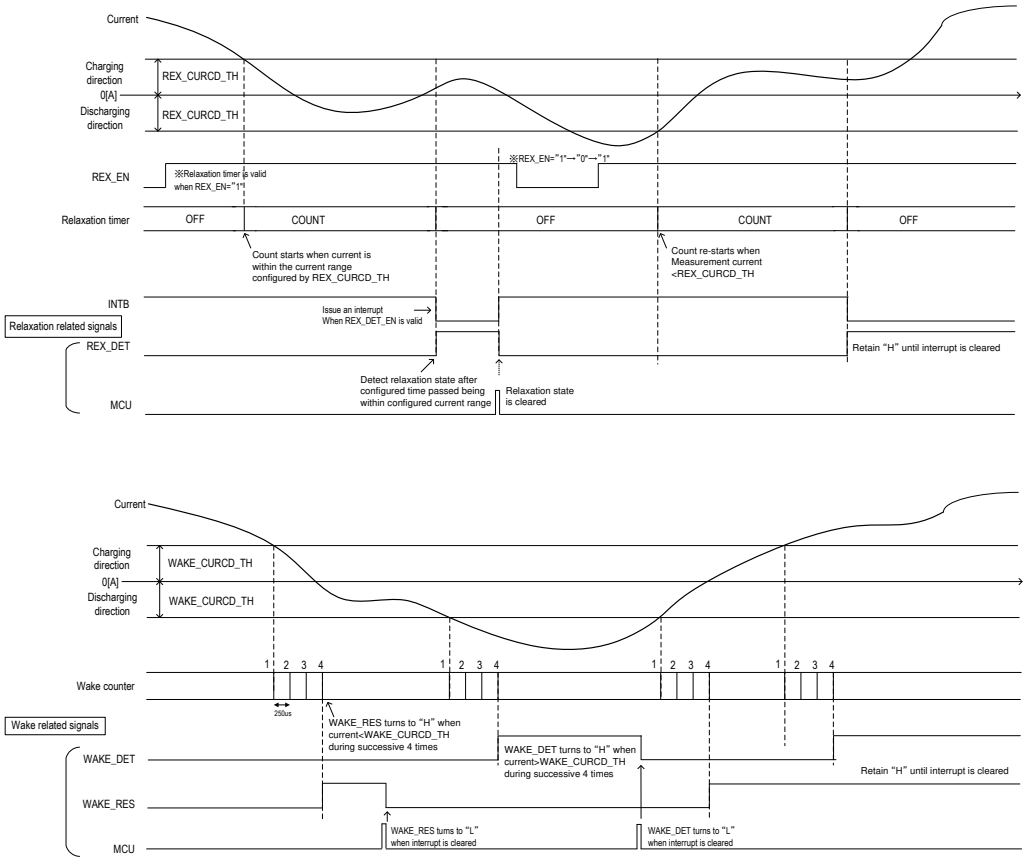


Figure 3-3. Relaxation State and Wake Up Current Detection Interrupt Timing Chart

Table 3-4. List of Relaxation State / Wake Up Interrupt Setting Registers

Address	Register Name	Description
13h to 14h	CURCD [14:0]	Measured Current Value
03h	REX_EN	Relax State Detection Timer Enable (0 : Timer OFF (0 Clear) 1 : Timer ON)
35h	REX_DUR [1:0]	Relax State Detection Time (00 : 30 minutes 01 : 60 minutes 10 : 90 minutes 11 : 120 minutes)
36h	REX_CURCD_TH [7:0]	Relaxation State Detection Threshold It is compared with the lower 8bits[7:0] of the CURCD [14:0] register.
37h	WAKE_CURCD_TH [7:0]	Wake up Detection Threshold It is compared with the lower 8bits[7:0] of the CURCD [14:0] register.
38h	WAKE_COUNT [1:0]	Number of Detection times for Wake up (00 : 1 time 01 : 4 times 10 : 8 times 11 : 16 times)

3.3.4 Interrupt for Detection of CRC Error

The BD7220FV-C incorporates SPI interface.
It is possible to add CRC code to the transmission and reception of SPI commands. Having CRC code or not is selectable by the leading EC bit of the data. For details, please refer to the section of 5.
CRC error can trigger interrupt.

In case of Data write:
Please add a CRC bit to the command when it is transmitted from the MCU.
When CRC error is detected at the time of the command reception, a CRC error triggers interrupt.
Please write “1” to CRCERR_DET_EN register to produce an interrupt signal through INTB.

In case of Data read:
CRC bits cannot be added to a read command from the MCU.
Please judge the CRC error on the MCU side as CRC bit is added to all transmitted and received data as a result of BD7220FV-C sending “read data” and “read command”.

3.3.5 Interrupt for Completion of Calibration

The BD7220FV-C has two calibration modes. (For details, please refer to section 4.1.2.)
When calibration is completed with mode 2, interrupt is triggered. Please write “1” to CALIB_FIN_EN register to produce an interrupt signal through INTB.

Customer’s product shipment:
It is assumed that the calibration is executed with the condition where the BD7220FV-C and external components are mounted in the process. Dispersion of external components can be considered when the calibration is executed with a mounted external current detection device such as a shunt resistor or current sensor.

4. Calibration

4.1 Summary

By communicating with SPI, BD7220FV-C can calibrate the variation of gain and offset. There are an auto calibration by SPI communication and a manual calibration by setting the calibration value into the registers. Because BD7220FV-C has a sequence circuit and a calculation circuit for calibration, it can output a calibration value automatically only by setting the input information and inputting a trigger signal. However, non-volatile memory is not built-in for this product. To be able to store values generated from automatic and manual calibration, it is necessary to use and maintain external memory.
Figure 4-1 shows the flow chart of calibration.

4.1.1 Features

·Calibration in BD7220FV-C shipment process:
The calibration values are kept in the built-in OTP and are downloaded automatically
·Calibration in customer's product shipment:
The calibration (gain and offset calibration) including the external current detection element in customer's process
·Manual calibration enabled to set the calibration value externally

4.1.2 Structure

BD7220FV-C can calibrate gain and offset error.
The three available calibration modes are explained below.

4.1.2.1 Calibration Mode 1 (in BD7220FV-C shipment process)

This calibration is carried out at the shipment of BD7220FV-C. Calibration is done with the internal regulator VREFCAL for calibration as a reference. An external capacitor at VREFCAL pin is not needed on customer's product, so please make the pin open. The external current detection element (shunt resistor or current sensor) is not calibrated. Only the gain and offset error of the built in AMP and ΔΣADC are calibrated. The calibration values are kept in the built in OTP in BD7220FV-C, and are read back automatically at startup. Offset calibration is tuned to the 25 V/V AMP gain setting by default, so it is necessary to use Mode 2 and Mode 3 for 5 V/V and 51 V/V settings.

4.1.2.2 Calibration Mode 2 (in customer's product process)

Calibration mode 2 is the calibration used in the customer's product shipment. This calibration includes the external current detection element.
It is possible to measure a highly precise current by carrying out the calibration when the external current detection element (shunt resistor or current sensor) is connected. To carry out this calibration, it is necessary to force as much current as will be used in the actual application. Mode 2 or Mode 3 offset calibration is necessary when using an AMP gain of 5 V/V or 51 V/V. If measurement will be performed using multiple AMP gain settings, Mode 2 calibration needs to be performed on each setting to be used.
BD7220FV-C outputs the calibration value after automatic operation. However, as BD7220FV-C does not have non-volatile memory, external memory is required to store the calibration values used. These values should be rewritten each time BD7220FV-C is reset.

4.1.2.3 Calibration Mode 3 (manual calibration)

This calibration is carried out manually by calculating the calibration value using MCUs or other methods.
Mode 3 can be used to compensate gain or offset variations caused by the measurement environment, such as the temperature. The value to be set for gain calibration is calculated by following the equation written later. The value to set for offset calibration is calculated referring to Table 1-1. Mode 2 or Mode 3 offset calibration is needed when using the 5 V/V and 51 V/V AMP gain settings, or for each gain setting used when measuring using multiple gain settings. However, as BD7220FV-C does not have non-volatile memory, external memory is required to store the calibration values used. These values should be rewritten each time BD7220FV-C is reset.

Calibration Mode 3 (manual calibration) – continued

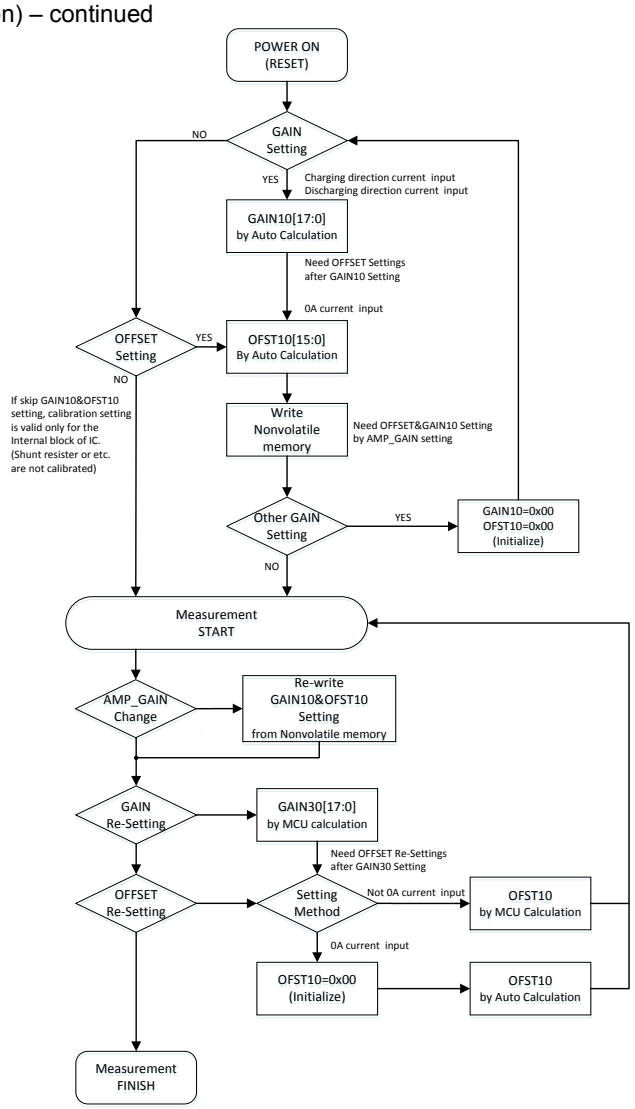


Figure 4-1. Flow Chart of Calibration

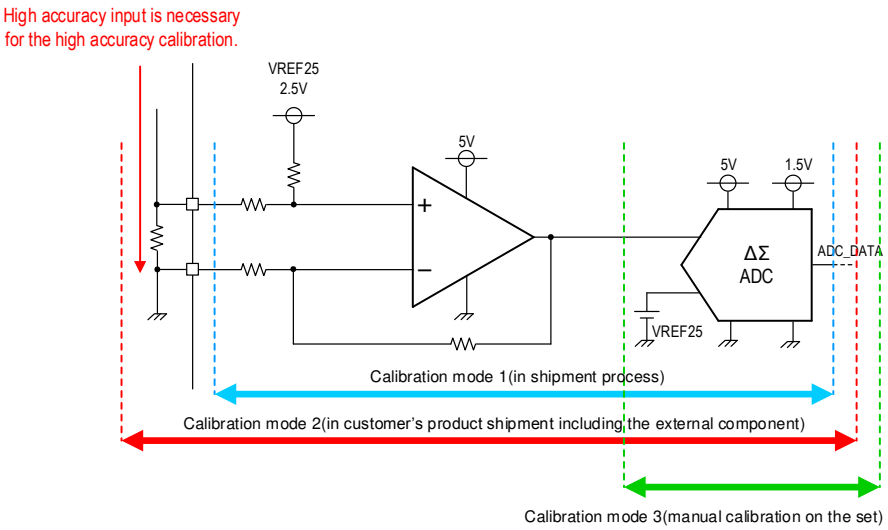


Figure 4-2. Calibration (Mode 1, Mode 2 and Mode 3)

4.2 Function Description

4.2.1 Calibration Mode 2

At customer's shipment, gain and offset error can be calibrated using Calibration Mode 2.
The calibration is carried out while forcing a certain differential voltage across the INP and INN pins. Calibrating with an external current detection element (such as a shunt resistor) enables higher accuracy current measurement. Note that in Mode 2, Gain Calibration must be performed before Offset Calibration. The calibration values in the register are discarded when BD7220FV-C is reset, so please write these to external memory and rewrite when BD7220FV-C starts up.

4.2.1.1 Calibration Mode2: Gain Calibration

Gain calibration is carried out by forcing voltage that correspond to 2 points of current value, one of charging current, PFS (current direction of INP voltage is positive); the other of discharging current, MFS (current direction of INP voltage is negative). Please set the data of differential voltage between PFS and MFS into the CALVIN_DIFF register. Please refer to Figure 4-3 for the relationship between PFS, MFS and CALVIN_DIFF registers. The current values in the figure are a 25 V/V AMP gain setting and R_{SNS} of 0.2 mΩ.

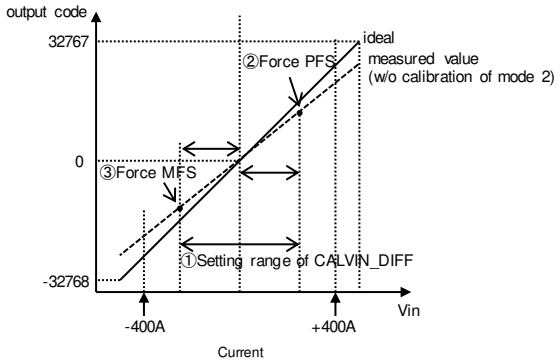


Figure 4-3. Force Setting for Gain Calibration

The flow of calibration is as follows.

1. Setting CALVIN_DIFF register (Data of differential voltage between PFS and MFS)
2. Forcing charging current PFS and executing calibration (writing "1" to CALIB_TRG register)
3. Forcing discharging current MFS and executing calibration (writing "1" to CALIB_TRG register)

Notice 1
Please carry out the calibration for each gain if you will measure with changing amp gain settings. The value set to GAIN10 register is needed with each amp gain setting.

Notice 2
Calibrating discharge current before charge current results in a wrong calibration value, so the order of calibrating charge current before discharge current must be strictly followed. If the calibration order was not followed, please reset BD7220FV-C.

The data of differential input voltage is set in CALVIN_DIFF [11:0] register.
The value to set is determined by the value of the external shunt resistor R_{SNS} and the amp gain setting as in the following equation. The differential current between PFS and MFS is over the possible setting range when calculated result is a negative value.

$$CALVIN\_DIFF\ \ value\ \ = \left\{2^{13} \times \frac{(\Delta I \times R_{SNS} \times AMP\_GAIN)}{4.5}\right\} -\ \ 2^{12}$$

$$R_{SNS}: resistance\ \ of\ \ shunt\ \ [\Omega]$$

Please refer to Table 4-1 for the possible setting range of CALVIN_DIFF for each amp gain setting.
For an AMP gain of 25 V/V and R_{SNS} of 0.2 mΩ, the range of CALVIN_DIFF is from 450 A to 800 A and the step is 109.86 mA. Please force 225 A for PFS and -225 A for MFS when CALVIN_DIFF is 450 A.

Calibration Mode2: Gain Calibration - continued

The minimum setting of differential current ΔI_{MIN} between PFS and MFS is changed by the value of R_{SNS} and gain setting. It is calculated with the following equation.

$$\Delta I_{MIN} = 2.25 \ / \ (AMP\_GAIN \times R_{SNS})$$
$$R_{SNS}: resistance \ of \ shunt \ [\Omega]$$

Table 4-1. Unit of CALVIN_DIFF Register Setting Current

	AMP_GAIN = 5 times				AMP_GAIN = 25 times				AMP_GAIN = 51 times			
	AMP Input Differential Voltage	UNIT	AMP Input Differential Current (R_{SNS} = 0.2 mΩ)	UNIT	AMP Input Differential Voltage	UNIT	AMP Input Differential Current (R_{SNS} = 0.2 mΩ)	UNIT	AMP Input Differential Voltage	UNIT	AMP Input Differential Current (R_{SNS} = 0.2 mΩ)	UNIT
Minimum Setting	450.00	mV	2250.00	A	90.00	mV	450.00	A	44.12	mV	220.59	A
Maximum Setting	599.96	mV	2999.82	A	160.00	mV	800.02	A	80.01	mV	400.03	A
Step Width	109.86	µV	549.32	mA	21.97	µV	109.86	mA	10.77	µV	53.85	mA

For example, considering an amp gain setting is 25 V/V, PFS = +300 A and MFS = -300 A, the differential current between PFS and MFS is 600 A. The differential current is within the possible setting range from 450 A to 800 A in Table 4-1, so it is possible to carry out calibration. If the differential current is outside the range, adjustment of input current is needed. The value to set to CALVIN_DIFF register is calculated as following.

$$CALVIN\_DIFF \ value = \left\{2^{13} \times \frac{(\Delta I \times R_{SNS} \times AMP\_GAIN)}{4.5}\right\} - 2^{12}$$
$$R_{SNS}: resistance \ of \ shunt [\Omega]$$

$$CALVIN\_DIFF = \{2^{13} \times (600[\text{A}] \times 0.2 \times 10^{-3} \times 25) \ / \ 4.5\} - 2^{12} = 1365[\text{DEC}] = 555[\text{HEX}]$$

Table 4-2 shows the flow of SPI communication in carrying out Gain Calibration.
After setting the register configurations and input voltage between INP and INN, you can carry out the calibration by writing "1" to CALIB_TRG register. After writing "1" to CALIB_TRG, the value will automatically clear to "0".
To complete gain calibration, 2 times trigger input for charge and discharge is needed.

Table 4-2. Calibration Mode 2: Flow of SPI Communication in Carrying Out Gain Calibration

Item	Register	Description	SPI				INP-INN Input
			R/W	REG ADDR	CONT ADDR	DATA	
Initial Configuration	CALVIN_DIFF_H = XXXX	Configuration of Diffrential Input Between	W	0Fh	1Eh	0Xh	-
	CALVIN_DIFF_L = XXXX	INP and INN	W	10h	20h	XXh	
	AMP_GAIN = XX MCIC_R = 11	Configure AMP_GAIN as Actual Use (For Higher Accurate Calibration, Configure MCIC_R Resister 2'b11 Regardless of Actual Use)	W	00h	00h	X0h	
Charge Configuration	GAIN_CAL_FS = 1, CALIB_MODE = 001	Forcing Charge Current Configure CALIB_MODE	W	04h	08h	09h	Input Differential Voltage of Charge
Charge Calibration	CALIB_TRG = 1	Trigger Input to Start Calibration	W	02h	04h	20h	
Discharge Configuration	GAIN_CAL_FS = 0, CALIB_MODE = 001	Forcing Discharge Current Configure CALIB_MODE	W	04h	08h	01h	Input Differential Voltage of Discharge
Discharge Calibration	CALIB_TRG = 1	Trigger Input to Start Calibration	W	02h	04h	20h	
Read Calibration Output in GAIN10 Resister	read GAIN10_2	Read Calibration Output	R	05h	0Bh	-	-
	read GAIN10_1		R	06h	0Dh	-	
	read GAIN10_0_GAIN30_2		R	07h	0Fh	-	

REG ADDR: Addresses in register map of BD7220FV-C
CONT ADDR: The first 1 byte data in SPI communication

Ex.1) Write REG ADDR = 0Fh → 8'b0000 1111 → 0(EC) + 6b'001111 + 0(Write) = 1Eh (EC Bit = 0, CRC is invalid)
Ex.2) Read REG ADDR = 02h → 8'b0000 0010 → 0(EC) + 6'b000010 + 1(Read) = 05h (EC Bit = 0, CRC is invalid)

*Calibration finishes (Detection of CALIB_FIN interrupt)
You will know when calibration is finished by using the CALIB_FIN register for interrupt. CALIB_FIN turns to "1" when Mode 2 Calibration is completed, so please clear the CALIB_FIN register before carrying out calibration. To validate the interrupt of INTB pin, please write CALIB_FIN_EN register "1".
If you need to perform Mode 2 Gain Calibration again, please do so after resetting GAIN10, OFST10 and GAIN30 registers to "0".

4.2.1.2 Calibration Mode2: Offset Calibration

Offset Calibration is carried out by input differential voltage without drawing current between the INP and INN pins. Write “1” to CALIB_TRG under forcing differential voltage and Offset Calibration is automatically carried out.
The flow of calibration is only one step:

1. After input differential voltage without drawing current between the INP and INN pins, and carry out calibration (Write “1” to CALIB_TRG)

Notice 1
Please carry out the calibration for each gain if you will measure with multiple amp gain settings.

Table 4-3 shows the flow of SPI communication in carrying out Offset Calibration.

Table 4-3. Calibration Mode 2: Flow of SPI Communication in Carrying Out Offset Calibration

Item	Register	Description	SPI				INP-INN Input
			R/W	REG ADDR	CONT ADDR	DATA	
Initial Configuration	AMP_GAIN = XX MCICR = 11,	Configure AMP_GAIN as Actual Use (For Higher Accurate Calibration, Configure MCIC_R Resister 2'b11 Regardless of Actual Use)	W	00h	00h	X0h	Input Differntial Voltage at No Current Flow (INP and INN Shorted)
	CALIB_MODE = 010	Configure CALIB_MODE	W	04h	08h	02h	
Offset Calibration	CALIB_TRG = 1	Trigger Input to Start Calibration	W	02h	04h	20h	
Read Calibration Output in OFST10	read OFST10_H	Read Caliration Output	R	0Ah	15h	-	-
	read OFST10_L		R	0Bh	17h	-	

* The way of to check if calibration is finished is the same as in Gain Calibration.

If you need to perform Mode 2 Offset Calibration again, please do so after resetting OFST10 to “0”.

4.2.2 Calibration Mode 3: Manual Calibration

Under typical usage conditions, gain and offset error can be calibrated using Calibration Mode 3.

4.2.2.1 Calibration Mode 3: Manual Calibration

Manual gain calibration uses the GAIN30 and GAIN31 registers. GAIN30 register is for configuration of the calibration value. Writing in the value calculated from an equation written later, gain is calibrated. GAIN31 register is a read-only register for reading the gain calibration configuration contained in the IC. When in Calibration Mode 2, the IC automatically calculates the needed gain adjustment ratio and sets the calibration value, but in Mode 3, you can calibrate by setting the configuration of gain adjustment ratio from 0.8x to 1.2x by 0.006% step. Gain adjustment ratio is calculated with the forced current value of 2 points, IP and IM, the corresponds output value of CURCD, PD and MD, the value of the external shunt resistor R_{SNS} and the amp gain setting in the following equation. Any combinations of current polarity are possible to be used, and not restricted to the combination of charge and discharge.

$$Gain\ \ adjustment\ \ ratio\ \ = \frac{(IP - IM) \times R_{SNS} \times AMP\_GAIN \times (2^{15} - 1)}{(PD - MD) \times 2.25}$$

$$R_{SNS}: resistance\ \ of\ \ shunt[\Omega]$$

For example, considering an amp gain setting is x25 V/V, external shut resister value is 0.2 mΩ, forced current IP=+100 A and IM=-250 A, values of CURCD PD=7645 and MD=-19113, gain adjustment ratio is calculated as following.

$$Gain\ \ adjustment\ \ ratio\ \ = \frac{\{100 - (-250)\} \times 0.2 \times 10^{-3} \times 25 \times (2^{15} - 1)}{\{7654 - (-19113)\} \times 2.25} = 0.95244$$

The value to set in GAIN30 register is calculated with the value of GAIN31 and the ratio of gain adjustment in the following equation. If the adjustment ratio is less than 1x, set the negative value as a 2's complement representation.

$$GAIN30\ \ value = \{GAIN31[\text{DEC}]\ \ \times (Gain\ \ adjustment\ \ ratio)\} - GAIN31[\text{DEC}]$$

For example, when GAIN31 register is 0xBD2C (48428[DEC]) and Gain Adjustment Ratio is 1.05x,

$$GAIN30\ \ value = \{48428[\text{DEC}]\ \ \times 1.05\} - 48428 = 2421[\text{DEC}] = 975[\text{HEX}]$$

And in case of the adjustment ratio is less than 1x as above example, calculation is as following.

$$GAIN30 = \{48428\ \ \times 0.95244\} - 48428 = -2303[\text{DEC}] = 3F701[\text{HEX}]$$

Notice 1
Please write registers for manual gain calibration in IDLE state or SSHDN mode, and do not write when measuring current.
Notice 2
If you operate Mode 3 Gain Calibration again, please re-calculate the value to set after resetting GAIN30 register to "0" and reading the value of GAIN31 register.
Notice 3
The value of GAIN31 register changes depending on the configuration of amp gain. So, if you will measure with multiple AMP gain configurations, the value of GAIN30 register must be calculated for each gain configuration. Please read GAIN31 register again and re-calculate the value after resetting GAIN30 register when gain configuration is changed.
Notice 4
The value of GAIN31 register changes depending on the calibration value obtained from Mode 2 Calibration (and stored in GAIN10 register.) If Mode 2 Calibration is to be performed again, please read GAIN31 register and re-calculate the value after resetting GAIN30 register.

4.2.2.2 Calibration Mode 3: Manual Offset Calibration

Manual Offset Calibration uses the OFST10 register. Writing OFST10 with the value added or subtracted corresponding to the amount of current you want to adjust, will calibrate the offset. To convert from current to adjust to register value, please refer to LSB current in Table 1-1. The value to set to OFST10 register is calculated with the original value of OFST10 register and adjustment current as in the following equation.

$$OFST10\ \ value = (original\ \ \ OFST10\ \ register\ \ value[\text{DEC}]) + (adjustment\ \ current[\text{DEC}])$$

In the case that the original value of OFST10 register is 16'h012C (=16'd300), the external current sense resistance is 0.2 mΩ, configuration of amp gain is 25 V/V, and adjust current is +5 A, LSB current is 13.73 mA. And the converted register value corresponding to the adjust current and setting value of OFST10 register is calculated as following.

$$adjust\ \ current[\text{DEC}] = 5[\text{A}] \div 13.73[\text{mA}] \ \approx 364.17 \ \approx 364[\text{DEC}]$$

$$OFST10\ \ value[\text{DEC}] = 300[\text{DEC}] + 364[\text{DEC}] = 664[\text{DEC}] = 298[\text{HEX}]$$

Notice 1
Please write registers for manual offset calibration in IDLE state or SSHDN mode, and do not write when measuring current.
Notice 2
If you operate Mode 3 Offset Calibration again, please overwrite OFST10 register with added/subtracted value corresponding to the additional adjust current.
Notice 3
When the configuration of amp gain is changed, please re-calculate OFST10 register value because of changing LSB current.

5. SPI Interface

5.1 Summary

BD7220FV-C is equipped with 500 kHz (Max) SPI interface. And also, it has the selectable (with/without) CRC code to improve the reliability of the communication (Mode 0 correspondence).

5.1.1 Features

- SPI Interface
- “Data write” carried out for every 1byte unit
- “Data read” carried out for every consecutive byte unit (setting number of bytes).
- Selectable with/without CRC cord (by the EC bit MSB of the control address)
- CRC polynomial: X^8+X^2+X+1

5.1.2 Constitution

BD7220FV-C has SPI interface.
Power supply of the SPI interface is the VDD pin.
SPI interface is enabled by turning the CSB pin to “L” level. The IC takes in the MSB-first input data on the SDI pin synchronous to the rising edges of SCK clock. Output- data is supplied on the SDO pin in the MSB-first order synchronous to the falling edges of SCK clock. SPI interface is disabled with “H” level input on the CSB pin and returns to the initial state. The CSB pin should be fixed to “H” level every time after one data write/read operation is completed. (Regarding the data reading, consecutive read in byte is available.)

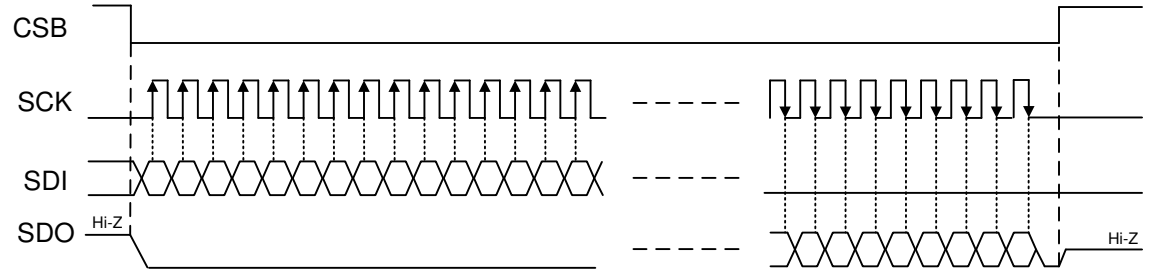


Figure 5-1. SPI Timing Chart

Configurations and controls can be done by reading/writing corresponding addresses in the control register. Write data is one-byte length, while read data length is specified in read commands. Set the RW bit to “0” for data write and “1” for data read. Also, set the EC bit to “1” if the CRC code for detecting a communication error is required or to “0” otherwise.

7	6	5	4	3	2	1	0
EC	Control register address						RW

	"0"	"1"
EC	without CRC	with CRC
RW	write	read

Figure 5-2. Control Address Constitution

5.2 Function Description

The below figures show the communication format of the data read/write with/without CRC

5.2.1 Data Write Communication Format without CRC

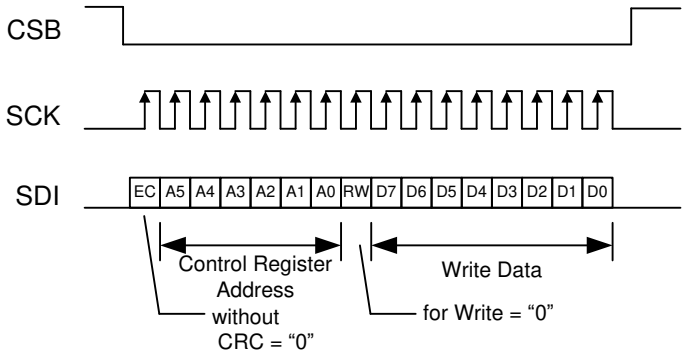


Figure 5-3. Data Write Communication Format without CRC

5.2.2 Data Read Communication Format without CRC

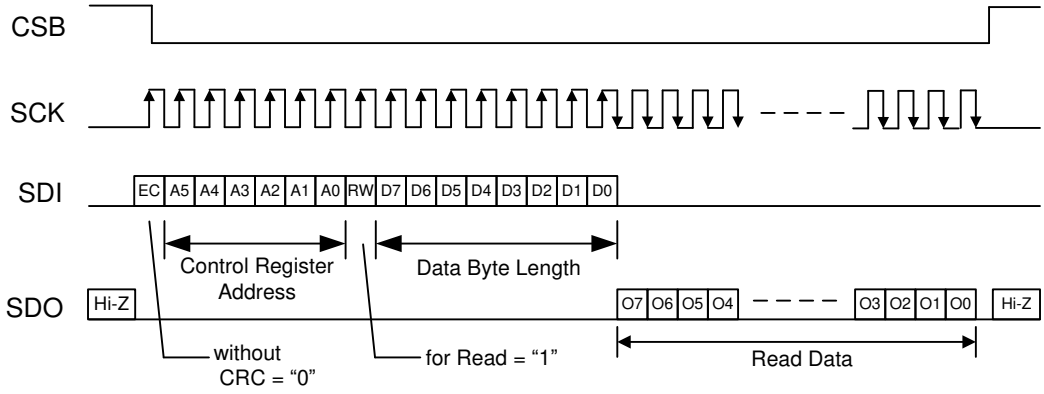


Figure 5-4. Data Read Communication Format without CRC

5.2.3 Data Write Communication Format with CRC

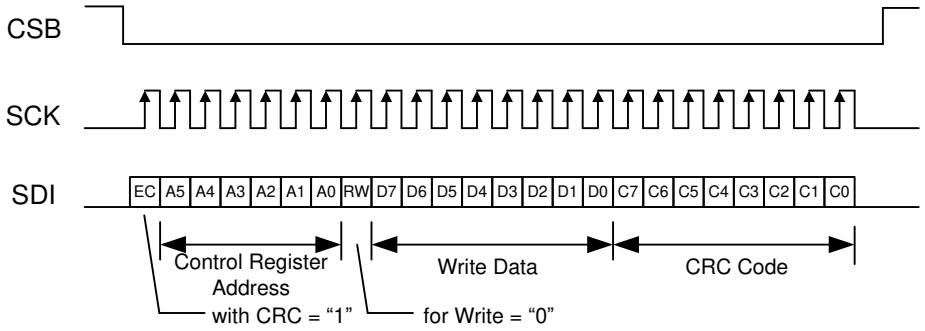


Figure 5-5. Data Write Communication Format with CRC

If a communication with CRC is selected (EC = "1"), 1-byte CRC (Cyclic Redundancy Code) is generated according to an X^8+X^2+X+1 equation, and added at the end of each communication data. Set the CSB pin to "H" level to initialize CRC computation to the default FFh.
Data write is performed on the specified control register only if the result from CRC computation matches the received CRC. Otherwise, data write is not performed. CRC error flag is set when CRC error is detected, and an interrupt signal is output to MCU from the INTB pin. Refer to the chapter 3 about detail interrupt explanation.

5.2.4 Data Read Communication Format with CRC

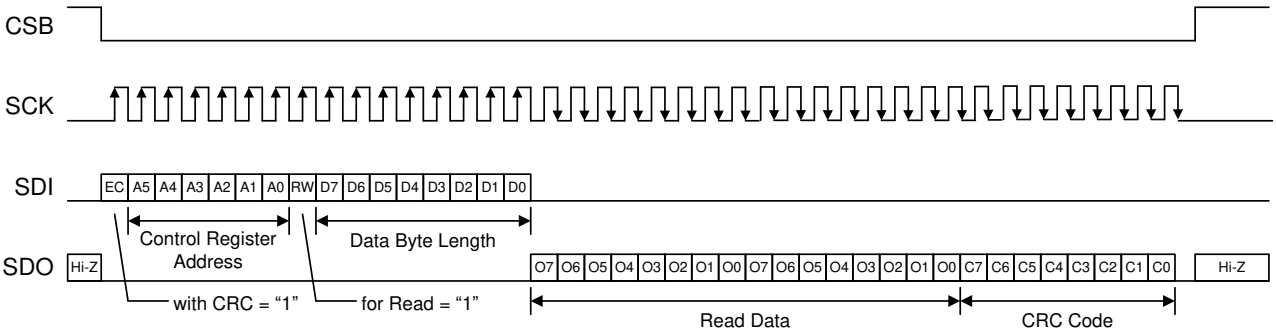


Figure 5-6. Data Read Communication Format with CRC

The CRC computation is also performed for each transmitted/received data during data read operation and the result is appended at the end of the read data. The external MCU can detect any communication errors by comparing the CRC computation result and the received CRC. The CRC code is not included in the data byte length.
The above figure is the example that the number of the read byte data is 2 bytes (data of read byte's number : 02h).

5.3 Multi Bytes Data Reading

The values of CURCD, AVE_CURCD, CC_CCNTD, CHG_CCNTD, DIS_CCNTD and EXADIN_VALUE registers are updated on current measurement and current accumulation and when EXADIN_TRG is triggered.
Please start reading from MSB address regarding these registers. By reading MSB address of multiple bytes' data, the value is retained in the internal buffer. This avoids updating the read data while reading over multiple address. Reading from LSB address may cause updating the data before finish reading all bytes.
If an access to another address is performed before reach to LSB address, read start from MSB address again. In this case, the read data is the value at the time of starting to read MSB again.

Ex.) CURCD Reading
Correct order : address 13h CURCD_H → address 14h CURCD_L
Incorrect order : address 14h CURCD_L → address 13h CURCD_H

6. EXADIN

6.1 Summary

ΔΣADC in BD7220FV-C has an input channel selectable function. A current value is monitored through AMP in normal operation. It can also monitor the voltage of the outside EXADIN pin by a setting signal from SPI.
It is possible to measure a value such as voltage of a battery or a thermistor by time sharing by this EXADIN function. (During the EXADIN pin measurement, it cannot measure a current value)

6.1.1 Features

·The EXADIN pin which can A-D convert the analog data besides current is available (EXADIN Input voltage range: 0.5 V to 4.5 V)

6.1.2 Structure

Figure 6-1 indicates the connection and structure of the EXADIN pin.

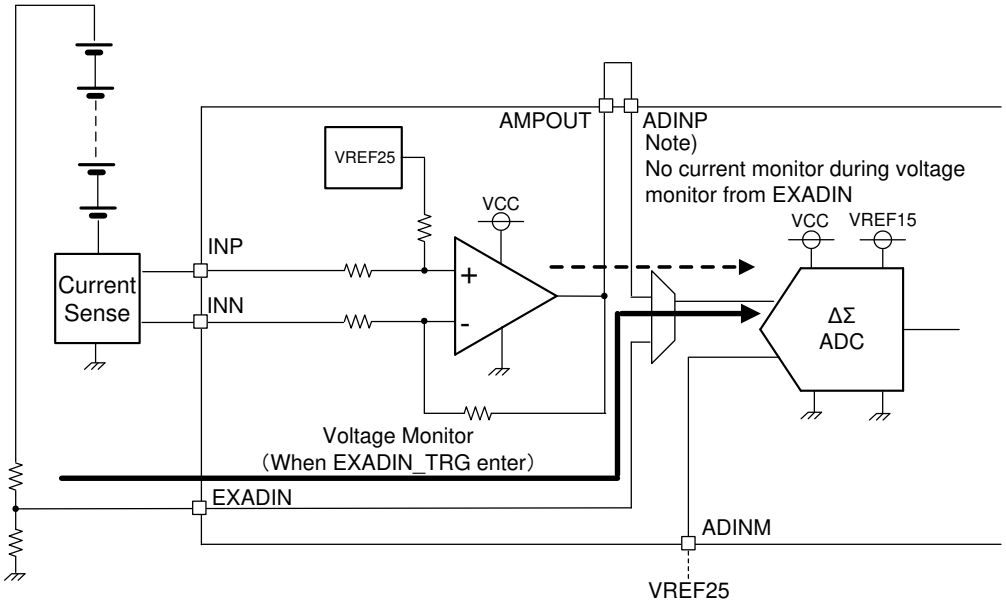


Figure 6-1. EXADIN Block Diagram

6.2 Function Description

To monitor of the EXADIN pin voltage is carried out by writing in “1” to EXADIN_TRG register (address 02h CC_TRG_RST_CMD [3]). After “1” was written in, EXADIN_TRG becomes “0” automatically.

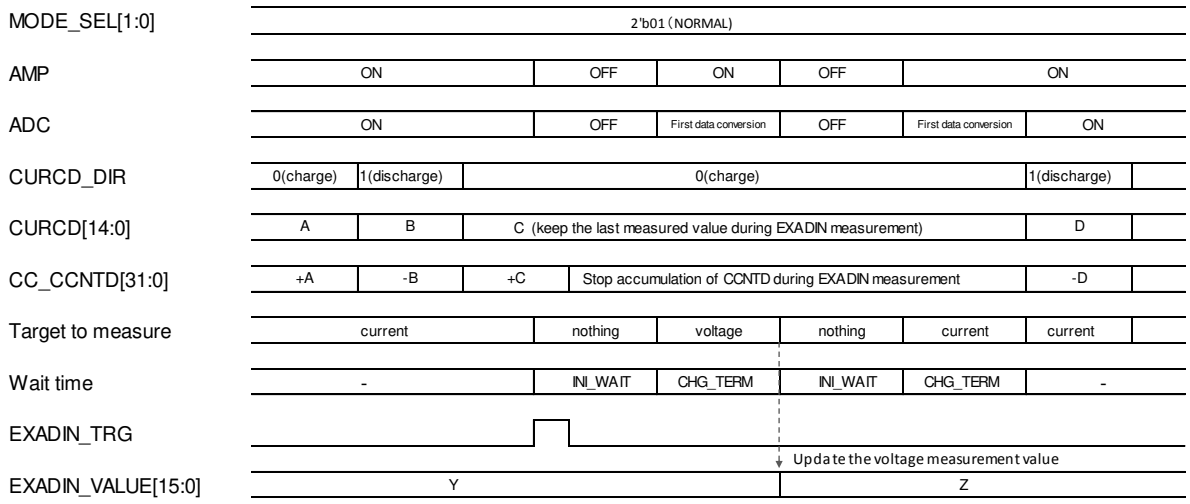


Figure 6-2. EXADIN Monitor Timing Chart

7. Register Map

Register address (dec)	Register address (Hex)	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Access (R, R/W)
0	00h	CC_SET1	AMP_GAIN[1:0]		MCIC_R[1:0]		-	CCNTEN	MODE_SEL[1:0]		80h	R/W
1	01h	CC_SET2	OSR[1:0]		CC_UNDIV	AVE_CURCD_COUNT[1:0]		CCNTD_MASK[2:0]			05h	R/W
2	02h	CC_TRG_RST_CMD	-	-	CALIB_TRG	-	EXADIN_TRG	DIS_CCNTD_RST	CHG_CCNTD_RST	CCNTRST	00h	R/W
3	03h	CC_SET3	-	SLEEP_CC_SEL	SLEEP_SAMPLING_TIME[1:0]		SLEEP_INTERVAL[1:0]		-	REX_EN	01h	R/W
4	04h	ADC_CALIB	-	-	-	-	GAIN_CAL_FS	CALIB_MODE[2:0]			00h	R/W
5	05h	GAIN10_2	-	-	-	-	GAIN10[17:14]				00h	R/W
6	06h	GAIN10_1	GAIN10[13:6]								00h	R/W
7	07h	GAIN10_0_GAIN30_2	GAIN10[5:0]						GAIN30[17:16]		00h	R/W
8	08h	GAIN30_1	GAIN30[15:8]								00h	R/W
9	09h	GAIN30_0	GAIN30[7:0]								00h	R/W
10	0Ah	OFST10_H	OFST10[15:8]								00h	R/W
11	0Bh	OFST10_L	OFST10[7:0]								00h	R/W
12	0Ch	GAIN31_2	-	-	-	-	-	-	GAIN31[17:16]		00h	R
13	0Dh	GAIN31_1	GAIN31[15:8]								40h	R
14	0Eh	GAIN31_0	GAIN31[7:0]								00h	R
15	0Fh	CALVIN_DIFF_H	-	-	-	-	CALVIN_DIFF[11:8]				00h	R/W
16	10h	CALVIN_DIFF_L	CALVIN_DIFF[7:0]								00h	R/W
17	11h	EXADIN_VALUE_H	EXADIN_VALUE[15:8]								00h	R
18	12h	EXADIN_VALUE_L	EXADIN_VALUE[7:0]								00h	R
19	13h	CURCD_H	CURCD_DIR	CURCD[14:8]							00h	R
20	14h	CURCD_L	CURCD[7:0]								00h	R
21	15h	AVE_CURCD_H	AVE_CURCD_DIR	AVE_CURCD[14:8]							00h	R
22	16h	AVE_CURCD_L	AVE_CURCD[7:0]								00h	R
23	17h	CC_CCNTD_3	CC_CCNTD[31:24]								00h	R/W
24	18h	CC_CCNTD_2	CC_CCNTD[23:16]								00h	R/W
25	19h	CC_CCNTD_1	CC_CCNTD[15:8]								00h	R/W
26	1Ah	CC_CCNTD_0	CC_CCNTD[7:0]								00h	R/W
27	1Bh	CHG_CCNTD_3	CHG_CCNTD[31:24]								00h	R/W
28	1Ch	CHG_CCNTD_2	CHG_CCNTD[23:16]								00h	R/W
29	1Dh	CHG_CCNTD_1	CHG_CCNTD[15:8]								00h	R/W
30	1Eh	CHG_CCNTD_0	CHG_CCNTD[7:0]								00h	R/W
31	1Fh	DIS_CCNTD_3	DIS_CCNTD[31:24]								00h	R/W
32	20h	DIS_CCNTD_2	DIS_CCNTD[23:16]								00h	R/W
33	21h	DIS_CCNTD_1	DIS_CCNTD[15:8]								00h	R/W
34	22h	DIS_CCNTD_0	DIS_CCNTD[7:0]								00h	R/W
35	23h	CC_BATCAP1_TH_2	CC_BATCAP1_TH[23:16]								00h	R/W
36	24h	CC_BATCAP1_TH_1	CC_BATCAP1_TH[15:8]								00h	R/W
37	25h	CC_BATCAP1_TH_0	CC_BATCAP1_TH[7:0]								00h	R/W
38	26h	CC_BATCAP2_TH_2	CC_BATCAP2_TH[23:16]								00h	R/W
39	27h	CC_BATCAP2_TH_1	CC_BATCAP2_TH[15:8]								00h	R/W
40	28h	CC_BATCAP2_TH_0	CC_BATCAP2_TH[7:0]								00h	R/W
41	29h	CC_BATCAP3_TH_2	CC_BATCAP3_TH[23:16]								00h	R/W
42	2Ah	CC_BATCAP3_TH_1	CC_BATCAP3_TH[15:8]								00h	R/W
43	2Bh	CC_BATCAP3_TH_0	CC_BATCAP3_TH[7:0]								00h	R/W
44	2Ch	CC_BATCAP4_TH_2	CC_BATCAP4_TH[23:16]								00h	R/W
45	2Dh	CC_BATCAP4_TH_1	CC_BATCAP4_TH[15:8]								00h	R/W
46	2Eh	CC_BATCAP4_TH_0	CC_BATCAP4_TH[7:0]								00h	R/W
47	2Fh	OCURTHR1_H	OCURTHR1_DIR	OCURTHR1[14:8]							00h	R/W
48	30h	OCURTHR1_L	OCURTHR1[7:0]								00h	R/W
49	31h	OCURTHR2_H	OCURTHR2_DIR	OCURTHR2[14:8]							00h	R/W
50	32h	OCURTHR2_L	OCURTHR2[7:0]								00h	R/W
51	33h	OCURTHR3_H	OCURTHR3_DIR	OCURTHR3[14:8]							00h	R/W
52	34h	OCURTHR3_L	OCURTHR3[7:0]								00h	R/W
53	35h	CC_SET4	REX_DUR[1:0]		OCURDUR3[1:0]		OCURDUR2[1:0]		OCURDUR1[1:0]		00h	R/W
54	36h	REX_CURCD_TH	REX_CURCD_TH[7:0]								00h	R/W
55	37h	WAKE_CURCD_TH	WAKE_CURCD_TH[7:0]								00h	R/W
56	38h	CC_SET5	-	-	INI_WAIT[1:0]		-	-	WAKE_COUNT[1:0]		00h	R/W
57	39h	INT_EN1	CC_MON4_RES_EN	CC_MON4_DET_EN	CC_MON3_RES_EN	CC_MON3_DET_EN	CC_MON2_RES_EN	CC_MON2_DET_EN	CC_MON1_RES_EN	CC_MON1_DET_EN	00h	R/W
58	3Ah	INT_EN2	OCUR3_RES_EN	OCUR3_DET_EN	OCUR2_RES_EN	OCUR2_DET_EN	OCUR1_RES_EN	OCUR1_DET_EN	ALARM_OCUR1_RES_EN	ALARM_OCUR1_DET_EN	00h	R/W
59	3Bh	INT_EN3	-	CALIB_FIN_EN	-	CRCERR_DET_EN	-	REX_DET_EN	WAKE_RES_EN	WAKE_DET_EN	00h	R/W
60	3Ch	INT_REQ1	CC_MON4_RES	CC_MON4_DET	CC_MON3_RES	CC_MON3_DET	CC_MON2_RES	CC_MON2_DET	CC_MON1_RES	CC_MON1_DET	00h	R/W
61	3Dh	INT_REQ2	OCUR3_RES	OCUR3_DET	OCUR2_RES	OCUR2_DET	OCUR1_RES	OCUR1_DET	-	-	00h	R/W
62	3Eh	INT_REQ3	-	CALIB_FIN	OTP_DL_FIN	CRCERR_DET	-	REX_DET	WAKE_RES	WAKE_DET	00h	R/W
63	3Fh	PAGE_SEL	HOSC_ON	-	-	-	-	-	PAGE_SEL[1:0]		00h	R/W

Address 00h: CC_SET1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	CC_SET1	R/W	AMP_GAIN[1:0]		MCIC_R[1:0]		-	CCNTEN	MODE_SEL[1:0]	
	Initial Value	80h	1	0	0	0	0	0	0	0

Bit 7-6 : AMP_GAIN[1:0]
00: 5 V/V
01: 25 V/V
10: 25 V/V (default)
11: 51 V/V

Differential amplifier gain reshuffling register

Depending on the measurement current range, it is necessary to choose an appropriate amplifier gain setting. Reference measurement current range when attaching a shunt resistance of 0.2 mΩ is as follows. (Refer to Table 1-1)
-1000 A to +2000 A -> 5 V/V
±400 A -> 25 V/V
±200 A -> 51 V/V

Bit 5-4 : MCIC_R[1:0]
00: 32 (default)
01: 128
10: 256
11: 1024

Built-in digital filter of Δ Σ ADC (down sampling)

Changing the sampling time and filter response of built-in digital filter for ADC.
The parameters that change under the influence of MCIC_R are as follows.

CURCD[14:0]
CURCD data are updated every ADC sampling time, based on Table 1-5.

AVE_CURCD[14:0]
AVE_CURCD data are updated every Average time, based on Table 1-4.

CC_CCNTD[31:0], CHG_CCNTD[31:0], DIS_CCNTD[31:0]
According to Table 2-3, the number of measurements during SLEEP mode is changed by MCIC_R.
CC_CCNTD, CHG_CCNTD, DIS_CCNTD data update is constant (250μs).

Bit 2 : CCNTEN
0: Coulomb counter OFF (default)
1: Coulomb counter ON

Enable Coulomb counter

CCNTEN=1 enables current accumulation.
Based on CURCD data (refer to section 1.3.1), current accumulation and output current accumulation data. (refer to section 1.3.2) Current accumulation data can read via SPI.
There are 3 kinds of current accumulation data: CC_CCNTD[31:0], CHG_CCNTD[31:0], DIS_CCNTD[31:0]

CCNTEN=0 to disables current accumulation.
When disabled, CC_CCNTD[31:0], CHG_CCNTD[31:0], DIS_CCNTD[31:0] keep the last data written.
When CCNTEN = 0, CC_CCNTD[31:0], CHG_CCNTD[31:0], DIS_CCNTD[31:0] can overwrite by SPI command.

Whether CCNTEN = 0 or 1, CC_CCNTD[31:0] is reset to "0" by CCNTRST=1.
Whether CCNTEN = 0 or 1, CHG_CCNTD[31:0] is reset to "0" by CHG_CCNTD_RST=1.
Whether CCNTEN = 0 or 1, DIS_CCNTD[31:0] is reset to "0" by DIS_CCNTD_RST=1.

Bit 1-0 : MODE_SEL[1:0]
00: (default) which does not shift
01: NORMAL
10: SLEEP
11: SSHDN

Operation mode choice

Operation mode can be changed from IDEL to any of three mode in left, NORMAL, SLEEP and SSHDN.
In the NORMAL, SLEEP and SSHDN mode, transition is possible by SPI command freely.
Operation mode is not changed by writing "00". (Remaining current mode)

Address 01h: CC_SET2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01h	CC_SET2	R/W	OSR[1:0]		CC_UNDIV	AVE_CURCD_COUNT[1:0]		CCNTD_MASK[2:0]		
	Initial Value	05h	0	0	0	0	0	1	0	1

Bit 7-6 : OSR[1:0]
00: 32(OSF=128kHz) (default)
01: 128(OSF=512kHz)
10: 512(OSF=2.048MHz)
11: 32(OSF=128kHz)

Over sampling rate setting
※OSF=Over Sampling Frequency

Over sampling rate settings for built in Δ Σ ADC.
The parameters to change under the influence of OSR are as follows.

CURCD[14:0]
CURCD data are updated every ADC sampling time of table 1-5.

AVE_CURCD[14:0]
AVE_CURCD data are updated every average time of table 1-4.

CC_CCNTD[31:0], CHG_CCNTD[31:0], DIS_CCNTD[31:0]
According to setting of table 2-3, the Number of measurement during SLEEP mode is changed by MCIC_R setting. CC_CCNTD, CHG_CCNTD, DIS_CCNTD data update is constant in every 250 μs.

Bit 5 : CC_UNDIV
0: Enable (default)
1: Disable

Enable scaled accumulation

To cancel the variation of LSB current in each gain setting, built-in calculation logic circuit can perform scaled calculation of current accumulation.
So, LSB of current accumulation is constant regardless of gain setting.

CC_UNDIV controls if this function is enabled.
Under the configulation of CC_UNDIV = 0, scaled calculation, gain setting can be changed with small error.
Under the configulation of CC_UNDIV = 1, not scaled caluclation, gain setting is fixed but there is no error caused by scaling.
Note that, compare to the capacity at 5 V/V gain, the current accumulation capacity is reduced depending on setting of gain, 1/5 at 25 V/V and 1/10.2 at 51 V/V.
(LSB of current accumulation is changed)

Bit 4-3 : AVE_CURCD_COUNT[1:0]
00: 4 times (default)
01: 16 times
10: 64 times
11: 128 times

Measurement count for average current calculation of a fixed time interval

The current measurement value of each fixed time interval can be calculated as an average value. It is not a moving average.
AVE_CURCD_COUNT sets the number of measurements to be averaged.
Average is caluculated from accumulating the A-D converted data for the times configured in AVE_CURCD_COUNT.
Fixed interval is configured with the setting of digital filter (address 00h:MCIC_R[1:0]), the setting of OSR(address 00h:OSR[1:0]), and the setting of measurement number (address 01h: AVE_CURCD_COUNT[1:0])

Bit 2-0 : CCNTD_MASK[2:0]
000: 7bits mask (effective 11bits)
001: 6bits mask (effective 12bits)
010: 5bits mask (effective 13bits)
011: 4bits mask (effective 14bits)
100: 3bits mask (effective 15bits)
101: 2bits mask (effective 16bits) (default)
110: 1bit mask (effective 17bits)
111: 0bit mask (effective 18bits)

Bit mask function for current accumulation

CCNTD_MASK sets the lower bit masked from the measurement current value during current accumulation. When masked, these bits are set to "0".

Address 02h: CC_TRG_RST_CMD Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02h	CC_TRG_RST_CMD	R/W	-	-	CALIB_TRG	-	EXADIN_TRG	DIS_CCNTD_RST	CHG_CCNTD_RST	CCNTRST
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 5 : CALIB_TRG — Calibration trigger — ※After "1" is written, value returns to "0" automatically
0: No trigger for calibration
1: Calibration start trigger

Bit 3 : EXADIN_TRG — Δ Σ ADC input signal change trigger — ※After "1" is written, value returns to "0" automatically
0: Current measurement
1: Switch Δ Σ ADC input to EXADIN (EXADIN pin voltage reading)

Bit 2 : DIS_CCNTD_RST — Discharge current accumulation (DIS_CCNTD) reset — ※After "1" is written, value returns to "0" automatically
0: No Reset
1: Reset DIS_CCNTD

Bit 1 : CHG_CCNTD_RST — Charge current accumulation (CHG_CCNTD) reset — ※After "1" is written, value returns to "0" automatically
0: No Reset
1: Reset CHG_CCNTD

Bit 0 : CCNTRST — Current accumulation (CC_CCNTD) reset — ※After "1" is written, value returns to "0" automatically
0: No Reset
1: Reset CC_CCNTD

Address 03h: CC_SET3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
03h	CC_SET3	R/W	-	SLEEP_CC_SEL	SLEEP_SAMPLING_TIME[1:0]		SLEEP_INTERVAL[1:0]		-	REX_EN
	Initial Value	01h	0	0	0	0	0	0	0	1

Bit 6 : SLEEP_CC_SEL — Current accumulation method in SLEEP mode, during the OFF period
0: Accumulate the last current measurement taken during the ON period. (default)
1: Accumulate the average of measurements taken during the ON period.

Bit 5-4 : SLEEP_SAMPLING_TIME[1:0] — Number of current accumulation when ON during SLEEP mode.
The parameters that change under the influence of SLEEP_SAMPLING_TIME are as follows. CC_CCNTD[31:0], CHG_CCNTD[31:0], DIS_CCNTD[31:0]
The number of current accumulations in SLEEP mode are decided as in Table 2-3.
The current accumulation data update is constant for every 250 µs.

If ADC sampling period < 2 [ms]:
00: 1 (default)
01: 16
10: 32
11: 64

If ADC sampling period ≥2 [ms]:
00: 1 (default)
01: 2
10: 4
11: 8

Bit 3-2 : SLEEP_INTERVAL[1:0] — ON/OFF time ratio during SLEEP mode
00: ON/OFF=1:7 (default)
01: ON/OFF=1:15
10: ON/OFF=1:31
11: ON/OFF=1:127

Bit 0 : REX_EN — Relax state detection timer enable
0: RELAX timer OFF
1: RELAX timer ON (default)
When REX_EN=1, if CURCD[14:0](13h+14h) ≤ { 7'd0, REX_CURCD_TH[7:0](36h)}, the relax timer starts.
If REX_EN = 1 → 0 is set while the timer is counting, the timer counter is reset to 0.
(Note that not keep the value but reset)
If REX_EN= 0 → 1 again, start counting from value = 0.

Address 04h: ADC_CALIB Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
04h	ADC_CALIB	R/W	-	-	-	-	GAIN_CAL_FS	CALIB_MODE[2:0]		
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 3 : GAIN_CAL_FS — Input polarity for GAIN calibration
0: Negative full scale (MFS) direction
1: Positive full scale (PFS) direction

Bit 2-0 : CALIB_MODE[2:0] — Calibration mode setting
000: Normal operation (default)
001: Mode2 (GAIN)
010: Mode2 (OFFSET)
011: Reserved
100: Reserved
101: Reserved
110: Reserved
111: Reserved
*Do not use any of the "Reserved" modes. (011, 100, 101, 110, 111)
Calibration revision value may shift.

Address 05h: GAIN10_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
05h	GAIN10_2	R/W	-	-	-	-	GAIN10[17:14]			
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 06h: GAIN10_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
06h	GAIN10_1	R/W	GAIN10[13:6]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 07h: GAIN10_0_GAIN30_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
07h	GAIN10_0_GAIN30_2	R/W	GAIN10[5:0]						GAIN30[17:16]	
	Initial Value	00h	0	0	0	0	0	0	0	0

GAIN10[17:0] Mode 2 gain calibration value

※Register data is cleared on reset (SHDNB=L or VCC UVLO).
Please keep register data in nonvolatile memory on the system and rewrite after IC restarts.

Address 08h: GAIN30_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
08h	GAIN30_1	R/W	GAIN30[15:8]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 09h: GAIN30_0 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
09h	GAIN30_0	R/W	GAIN30[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

GAIN30[17:0] Mode 3 gain calibration value

※Register data is cleared on reset (SHDNB=L or VCC UVLO).
Please keep register data in nonvolatile memory on the system and rewrite after IC restarts.

Address 0Ah: OFST10_H Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ah	OFST10_H	R/W	OFST10[15:8]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 0Bh: OFST10_L Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Bh	OFST10_L	R/W	OFST10[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

OFST10[15:0] Mode 2 offset calibration value

※Register data is cleared on reset (SHDNB=L or VCC UVLO).
Please keep register data in nonvolatile memory on the system and rewrite after IC restarts.

Address 0Ch: GAIN31_2 Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ch	GAIN31_2	R	-						GAIN31[17:16]	
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 0Dh: GAIN31_1 Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Dh	GAIN31_1	R	GAIN31[15:8]							
	Initial Value	40h	0	1	0	0	0	0	0	0

Address 0Eh: GAIN31_0 Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Eh	GAIN31_0	R	GAIN31[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

GAIN31[17:0] Register for the GAIN30 operation
(GAIN30 is register for the manual setting)

Address 0Fh: CALVIN_DIFF_H Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Fh	CALVIN_DIFF_H	R/W	-	-	-	-	CALVIN_DIFF[11:8]			
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 10h: CALVIN_DIFF_L Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
10h	CALVIN_DIFF_L	R/W	CALVIN_DIFF[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

CALVIN_DIFF[11:0] Mode 2 calibration setting register Input differential voltage information between INP and INN for GAIN calibration

Address 11h: EXADIN_VALUE_H Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
11h	EXADIN_VALUE_H	R	EXADIN_VALUE[15:8]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 12h: EXADIN_VALUE_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
12h	EXADIN_VALUE_L	R	EXADIN_VALUE[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

EXADIN_VALUE[15:0] Measurement value of EXADIN input

Address 13h: CURCD_H Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
13h	CURCD_H	R	CURCD_DIR	CURCD[14:8]						
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7: CURCD_DIR Current direction bit
0: Charge
(INP pin voltage > INN pin voltage)
1: Discharge
(INP pin voltage < INN pin voltage)

Address 14h: CURCD_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
14h	CURCD_L	R	CURCD[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

CURCD[14:0] Current value

LSB unit of CURCD depending on the gain setting is described in Chapter 1.3.1.
The reference level when attaching an external 0.2 mΩ resistance is as follows.
(see Table 1-1)
5 V/V gain: LSB current = 68.66 mA
25 V/V gain: LSB current =13.73 mA
51 V/V gain: LSB current = 6.73 mA

ex.) When a 1,000 mA current flows, the register level is as follows.
5 V/V gain: 1000/LSB current = 1000/68.66=14 => CURCD=15'h000E
25 V/V gain: 1000/LSB current = 1000/13.73=72 => CURCD=15'h0048
51 V/V gain: 1000/LSB current = 1000/6.73=148 => CURCD=15'h0094

Address 15h: AVE_CURCD_H Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
15h	AVE_CURCD_H	R	AVE_CURCD_DIR	AVE_CURCD[14:8]						
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7: AVE_CURCD_DIR Average current direction bit
0: Charge
(INP pin voltage > INN pin voltage)
1: Discharge
(INP pin voltage <INN pin voltage)

Address 16h: AVE_CURCD_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
16h	AVE_CURCD_L	R	AVE_CURCD[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

AVE_CURCD[14:0] Average Current value

Number of averaging is set in AVE_CURCD_COUNT(01h)
LSB unit of CURCD depending on the gain setting is described in Chapter 1.3.1.
The reference level when attaching an external 0.2 mΩ resistance is as follows.
(see Table 1-1)
5 V/V gain: LSB current = 68.66 mA
25 V/V gain: LSB current =13.73 mA
51 V/V gain: LSB current = 6.73 mA

ex.) When a 1,000 mA current flows, the register level is as follows.
5 V/V gain: 1000/LSB current = 1000/68.66=14 => CURCD=15'h000E
25 V/V gain: 1000/LSB current = 1000/13.73=72 => CURCD=15'h0048
51 V/V gain: 1000/LSB current = 1000/6.73=148 => CURCD=15'h0094

Address 17h: CC_CCNTD_3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
17h	CC_CCNTD_3	R/W	CC_CCNTD[31:24]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 18h: CC_CCNTD_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
18h	CC_CCNTD_2	R/W	CC_CCNTD[23:16]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 19h: CC_CCNTD_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
19h	CC_CCNTD_1	R/W	CC_CCNTD[15:8]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 1Ah: CC_CCNTD_0 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Ah	CC_CCNTD_0	R/W	CC_CCNTD[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

CC_CCNTD[31:0] Current Accumulation register

LSB unit of CC_CCNTD depending on the gain setting is described in Chapter 1.3.2.
The reference level when attaching an external 0.2 mΩ resistance and CC_UNDIV=0 is as follows.
LSB level = 0.3052 μAh
MSB level = 655.36 Ah
When CC_UNDIV=1, the current accumulation unit varies depending on setting of AMP_GAIN. (see table 1-2)

Address 1Bh: CHG_CCNTD_3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Bh	CHG_CCNTD_3	R/W	CHG_CCNTD[31:24]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 1Ch: CHG_CCNTD_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Ch	CHG_CCNTD_2	R/W	CHG_CCNTD[23:16]							
	Initial Value	00h	0	0	0	0	0	0	0	0

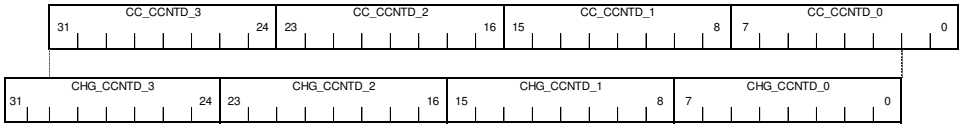
Address 1Dh: CHG_CCNTD_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Dh	CHG_CCNTD_1	R/W	CHG_CCNTD[15:8]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 1Eh: CHG_CCNTD_0 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Eh	CHG_CCNTD_0	R/W	CHG_CCNTD[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

CHG_CCNTD[31:0] Charge Current Accumulation register ※see Chapter 1.3.2



LSB of CHG_CCNTD is equivalent to bit[2] of CC_CCNTD.

Address 1Fh: DIS_CCNTD_3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Fh	DIS_CCNTD_3	R/W	DIS_CCNTD[31:24]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 20h: DIS_CCNTD_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20h	DIS_CCNTD_2	R/W	DIS_CCNTD[23:16]							
	Initial Value	00h	0	0	0	0	0	0	0	0

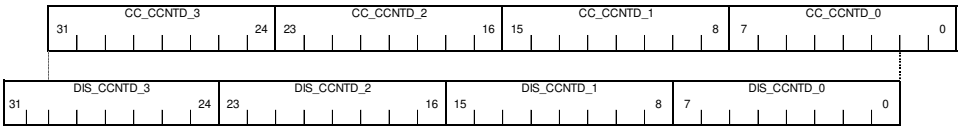
Address 21h: DIS_CCNTD_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
21h	DIS_CCNTD_1	R/W	DIS_CCNTD[15:8]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 22h: DIS_CCNTD_0 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
22h	DIS_CCNTD_0	R/W	DIS_CCNTD[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

DIS_CCNTD[31:0] Discharge Current Accumulation register ※see chapter 1.3.2



LSB of DIS_CCNTD is equivalent to bit[2] of CC_CCNTD.

Address 23h: CC_BATCAP1_TH_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
23h	CC_BATCAP1_TH_2	R/W	CC_BATCAP1_TH[23:16]							
	Initial Value	00h	0	0	0	0	0	0	0	0

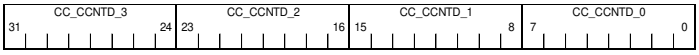
Address 24h: CC_BATCAP1_TH_1 Register (R/W)

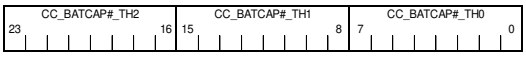
Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
24h	CC_BATCAP1_TH_1	R/W	CC_BATCAP1_TH[15:8]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 25h: CC_BATCAP1_TH_0 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
25h	CC_BATCAP1_TH_0	R/W	CC_BATCAP1_TH[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

CC_BATCAP1_TH[23:0] Threshold of current accumulation detection1





For higher 24bit of CC_CCNTD, set the detection of current accumulation threshold.
(The setting method is the same for CC_BATCAP1 to 4_TH)

LSB level of CC_BATCAP1_TH and the MSB levels are as follows
(when CC_UNDIV=0)

LSB level =78.125 µAh
MSB level =655.36 Ah

The LSB value and MSB value of CC_CCNTD are as follows. (Refer to section 1.3.2)

LSB level =0.3052 µAh
MSB level =655.36 Ah

ex.) To set the detection threshold of current accumulation to 1Ah,
the register values are as follows.

1[Ah]/78.125[µAh]=12800 => CC_BATCAP1_TH[23:0]=24'h003200(24'd12800)

The threshold range is as follows.

Thresholding range =78.125 µAh to 1310.72 Ah

When CC_UNDIV=1, unit of current accumulation varies depending on setting of AMP_GAIN. (see Table 1-2)

Address 26h: CC_BATCAP2_TH_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
26h	CC_BATCAP2_TH_2	R/W	CC_BATCAP2_TH[23:16]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 27h: CC_BATCAP2_TH_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
27h	CC_BATCAP2_TH_1	R/W	CC_BATCAP2_TH[15:8]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 28h: CC_BATCAP2_TH_0 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
28h	CC_BATCAP2_TH_0	R/W	CC_BATCAP2_TH[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

CC_BATCAP2_TH[23:0]: Threshold of current accumulation detection2 ※Refer to CC_BATCAP1_TH for the setting

Address 29h: CC_BATCAP3_TH_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
29h	CC_BATCAP3_TH_2	R/W	CC_BATCAP3_TH[23:16]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 2Ah: CC_BATCAP3_TH_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Ah	CC_BATCAP3_TH_1	R/W	CC_BATCAP3_TH[15:8]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 2Bh: CC_BATCAP3_TH_0 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Bh	CC_BATCAP3_TH_0	R/W	CC_BATCAP3_TH[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

CC_BATCAP3_TH[23:0] Threshold of current accumulation detection3 ※Refer to CC_BATCAP1_TH for the setting

Address 2Ch: CC_BATCAP4_TH_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Ch	CC_BATCAP4_TH_2	R/W	CC_BATCAP4_TH[23:16]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 2Dh: CC_BATCAP4_TH_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Dh	CC_BATCAP4_TH_1	R/W	CC_BATCAP4_TH[15:8]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 2Eh: CC_BATCAP4_TH_0 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Eh	CC_BATCAP4_TH_0	R/W	CC_BATCAP4_TH[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

CC_BATCAP4_TH[23:0] Threshold of current accumulation detection4 ※Refer to CC_BATCAP1_TH for the setting

Address 2Fh: OCURTHR1_H Register (R/W)

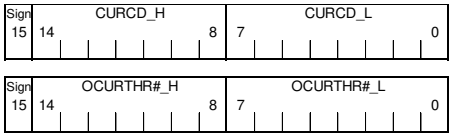
Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Fh	OCURTHR1_H	R/W	OCURTHR1_DIR	OCURTHR1[14:8]						
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7: OCURTHR1_DIR: Current direction setting of OCURTHR1
0: Charge
(INP pin voltage > INN pin voltage)
1: Discharge
(INP pin voltage <INN pin voltage)

Address 30h: OCURTHR1_L Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
30h	OCURTHR1_L	R/W	OCURTHR1[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

OCURTHR1[14:0]: Threshold of measurement current detection1



LSB unit of CURCD depending on the gain setting is described in Chapter 1.3.1.
The reference level when attaching an external 0.2mΩ resistance is as follows.
(Refer to table 1-1)
5 V/V gain: LSB electric current level ≒ 68.66 mA
25 V/V gain: LSB electric current level ≒ 13.73 mA
51 V/V gain: LSB electric current level ≒ 6.73 mA

ex.) When a current value of 1,000mA flows, the register level is as follows.
OCCURTHR1_DIR = 0 and
5 V/V gain: 1000/LSB current ≒ 1000/68.66≒14 => OCURTHR1=15'h000E
25 V/V gain: 1000/LSB current ≒ 1000/13.73≒72 => OCURTHR1=15'h0048
51 V/V gain: 1000/LSB current ≒ 1000/6.73≒148 => OCURTHR1=15'h0094

The thresholding ranges are as follows.
5 V/V gain: Thresholding range ≒ -1000 A to +2000 A
25 V/V gain: Thresholding range ≒ -400A to +400 A
51 V/V gain: Thresholding range ≒ -200 A to +200 A
Threshold range is different from measurement current range.

When OCURTHR1_DIR = 0, detection of charging direction of measurement current interrupt be set. An interrupt occurs when:
OCUR1_DET_EN (3Ah) = 1 and
CURCD (13h + 14h) > OCURTHR1 (2Fh + 30h) and
over the consecutive detection setting by OCURDUR1[1:0](35h)
OCUR1_RES_EN (3Ah) = 1 and
CURCD (13h + 14h) ≤ OCURTHR1 (2Fh + 30h) and
over the consecutive detection setting by OCURDUR1[1:0](35h)

When OCURTHR1_DIR = 1, detection of discharging direction of measurement current interrupt be set.An interrupt occurs when:
OCUR1_DET_EN (3Ah) = 1 and
CURCD (13h + 14h) > OCURTHR1 (2Fh + 30h) and
over the consecutive detection setting by OCURDUR1[1:0](35h)
OCUR1_RES_EN (3Ah) = 1 and
CURCD (13h + 14h) ≤ OCURTHR1 (2Fh + 30h) and
over the consecutive detection setting by OCURDUR1[1:0](35h)

Address 31h: OCURTHR2_H Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
31h	OCURTHR2_H	R/W	OCURTHR2_DIR	OCURTHR2[14:8]						
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7: OCURTHR2_DIR Current direction setting of OCURTHR2
0: Charge
(INP pin voltage > INN pin voltage)
1: Discharge
(INP pin voltage <INN pin voltage)

Address 32h: OCURTHR2_L Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
32h	OCURTHR2_L	R/W	OCURTHR2[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

OCURTHR2[14:0] Threshold of measurement current detection2 Refer to OCURTHR1 for the setting

Address 33h: OCURTHR3_H Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
33h	OCURTHR3_H	R/W	OCURTHR3_DIR	OCURTHR3[14:8]						
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7: OCURTHR3_DIR — Current direction setting of OCURTHR3
0: Charge
(INP pin voltage > INN pin voltage)
1: Discharge
(INP pin voltage <INN pin voltage)

Address 34h: OCURTHR3_L Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
34h	OCURTHR3_L	R/W	OCURTHR3[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

OCURTHR3[14:0] — Threshold of measurement current detection3 — Refer to OCURTHR1 for the setting

Address 35h: CC_SET4 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
35h	CC_SET4	R/W	REX_DUR[1:0]		OCURDUR3[1:0]		OCURDUR2[1:0]		OCURDUR1[1:0]	
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7-6: REX_DUR[1:0] — Relaxation state detection time — Refer to REX_CURCD_TH for the relaxation state detection setting
00:30 minutes(default)
01:60 minutes
10:90 minutes
11:120 minutes

Bit 5-4: OCURDUR3[1:0] — Count for detection of measurement current — ex. If CURDUR3 = 4 times, when detect over or under current value 4times, interrupt occurs. Refer to OCURTHR1, OCUR1_DET_EN, OCUR1_RES_EN
00:1 time(default)
01:4 times
10:8 times
11:16 times

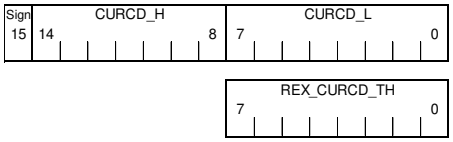
Bit 3-2: OCURDUR2[1:0] — Count for detection of measurement current — ex. If CURDUR2 = 4 times, when detect over or under current value 4times, interrupt occurs. Refer to OCURTHR1, OCUR1_DET_EN, OCUR1_RES_EN
00:1 time(default)
01:4 times
10:8 times
11:16 times

Bit 1-0: OCURDUR1[1:0] — Count for detection of measurement current — ex. If CURDUR1 = 4 times, when detect over or under current value 4times, interrupt occurs. Refer to OCURTHR1, OCUR1_DET_EN, OCUR1_RES_EN
00:1 time(default)
01:4 times
10:8 times
11:16 times

Address 36h: REX_CURCD_TH Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
36h	REX_CURCD_TH	R/W	REX_CURCD_TH[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

REX_CURCD_TH[7:0] Threshold of the relaxation state detection measurement current



Refer to REX_EN about relax timer setting
(Relaxation timer is enable when REX_EN=1)
REX_CURCD_TH can be set in the lower 8 bits of CURCD. (unsigned 8 bits expression)

LSB unit of CURCD depending on the gain setting is described in Chapter 1.3.1.
The reference level when attaching an external 0.2mΩ resistance is as follows.
(Refer to Table 1-1)
5 V/V gain: LSB current = 68.66 mA
25 V/V gain: LSB current = 13.73 mA
51 V/V gain: LSB current = 6.73 mA

ex.) When a 1,000mA current flows, the register level is as follows.
5 V/V gain: 1000/LSB current = 1000/68.66 = 14 => REX_CURCD_TH=15'h000E
25 V/V gain: 1000/LSB current = 1000/13.73 = 72 => REX_CURCD_TH=15'h0048
51 V/V gain: 1000/LSB current = 1000/6.73 = 148 => REX_CURCD_TH=15'h0094

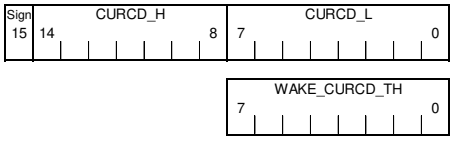
The threshold ranges are as follows.
5 V/V gain: Threshold range = 0 to 17.51 A
25 V/V gain: Threshold range = 0 to 3.50 A
51 V/V gain: Threshold range = 0 to 1.72 A

An interrupt occurs when:
REX_DET_EN(3Bh) = 1 and
CURCD[14:0] (13h + 14h) ≤ { 7'd0, REX_CURCD_TH[7:0] (36h) } and
Relaxation state detection time over the setting by REX_DUR[1:0](35h)

Address 37h: WAKE_CURCD_TH Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
37h	WAKE_CURCD_TH	R/W	WAKE_CURCD_TH[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

WAKE_CURCD_TH[7:0] Threshold of wake-up current detection



WAKE_CURCD_TH can be set in the lower 8 bits of CURCD. (unsigned 8 bits expression)

LSB unit of CURCD depending on the gain setting is described in Chapter 1.3.1.
The reference level when attaching an external 0.2 mΩ resistance is as follows.
(Refer to Table 1-1)
5 V/V gain: LSB current = 68.66 mA
25 V/V gain: LSB current = 13.73 mA
51 V/V gain: LSB current = 6.73 mA

ex.) When a 1,000 mA current flows, the register level is as follows.
5 V/V gain: 1000/LSB current = 1000/68.66≈14 => WAKE_CURCD_TH=15'h000E
25 V/V gain: 1000/LSB current = 1000/13.73≈72 => WAKE_CURCD_TH=15'h0048
51 V/V gain: 1000/LSB current = 1000/6.73≈148 => WAKE_CURCD_TH=15'h0094

The threshold ranges are as follows.
5V/V gain: Threshold range = 0 to 17.51A
25V/V gain: Threshold range = 0 to 3.50A
51V/V gain: Threshold range = 0 to 1.72A

The WAKE_RES interrupt occurs when:
WAKE_RES_EN(3Bh) = 1 and
CURCD[14:0] (13h + 14h) ≤ { 7'd0, WAKE_CURCD_TH[7:0] (37h) } and
Wake up current detection over the setting by WAKE_COUNT[1:0](38h)

The WAKE_DET interrupt occurs when:
WAKE_DET_EN(3Bh) = 1 and
CURCD[14:0] (13h + 14h) > { 7'd0, WAKE_CURCD_TH[7:0] (37h) } and
Wake up current detection over the setting by WAKE_COUNT[1:0](38h)

Address 38h: CC_SET5 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
38h	CC_SET5	R/W	-	-	INI_WAIT[1:0]		-		WAKE_COUNT[1:0]	
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 5-4 : INI_WAIT[1:0] Initial wait time setting
00: 1.5ms(default)
01: 3.0ms
10: 6.0ms
11: 12.0ms

The INI_WAIT register sets initial wait time for start of VREF25 and AMP

Bit 1-0 : WAKE_COUNT[1:0] Wake up current detection count
00: 1 time(default)
01: 4 times
10: 8times
11: 16times

Refer to WAKE_CURCD_TH for the wake up current detection setting

Address 39h: INT_EN1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
39h	INT_EN1	R/W	CC_MON4_RES_EN	CC_MON4_DET_EN	CC_MON3_RES_EN	CC_MON3_DET_EN	CC_MON2_RES_EN	CC_MON2_DET_EN	CC_MON1_RES_EN	CC_MON1_DET_EN
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7 : CC_MON4_RES_EN
Interrupt Enable : Detection of discharging direction current accumulation value4
1: Enable 0: Disable
CC_MON4_RES_EN=1: CC_MON4_RES=1 -> INTB=L,CC_MON4_RES=0 -> INTB=Hi-z
CC_MON4_RES_EN=0: INTB=Hi-z (regardless of CC_MON4_RES)

Bit 6 : CC_MON4_DET_EN
Interrupt Enable : Detection of charging direction current accumulation value4
1: Enable 0: Disable
CC_MON4_DET_EN=1: CC_MON4_DET=1 -> INTB=L, CC_MON4_DET=0 -> INTB=Hi-z
CC_MON4_DET_EN=0: INTB=Hi-z (regardless of CC_MON4_DET)

Bit 5 : CC_MON3_RES_EN
Interrupt Enable : Detection of discharging direction current accumulation value3
1: Enable 0: Disable
CC_MON3_RES_EN=1: CC_MON3_RES=1 -> INTB=L,CC_MON3_RES=0 -> INTB=Hi-z
CC_MON3_RES_EN=0: INTB=Hi-z (regardless of CC_MON3_RES)

Bit 4 : CC_MON3_DET_EN
Interrupt Enable : Detection of charging direction current accumulation value3
1: Enable 0: Disable
CC_MON3_DET_EN=1: CC_MON3_DET=1 -> INTB=L,CC_MON3_DET=0 -> INTB=Hi-z
CC_MON3_DET_EN=0: INTB=Hi-z (regardless of CC_MON3_DET)

Bit 3 : CC_MON2_RES_EN
Interrupt Enable : Detection of discharging direction current accumulation value2
1: Enable 0: Disable
CC_MON2_RES_EN=1: CC_MON2_RES=1 -> INTB=L, CC_MON2_RES=0 -> INTB=Hi-z
CC_MON2_RES_EN=0: INTB=Hi-z (regardless of CC_MON2_RES)

Bit 2 : CC_MON2_DET_EN
Interrupt Enable : Detection of charging direction current accumulation value2
1: Enable 0: Disable
CC_MON2_DET_EN=1: CC_MON2_DET=1 -> INTB=L, CC_MON2_DET=0 -> INTB=Hi-z
CC_MON2_DET_EN=0: INTB=Hi-z (regardless of CC_MON2_DET)

Bit 1 : CC_MON1_RES_EN
Interrupt Enable : Detection of discharging direction current accumulation value1
1: Enable 0: Disable
CC_MON1_RES_EN=1: CC_MON1_RES=1 -> INTB=L, CC_MON1_RES=0 -> INTB=Hi-z
CC_MON1_RES_EN=0: INTB=Hi-z (regardless of CC_MON1_RES)

Bit 0 : CC_MON1_DET_EN
Interrupt Enable : Detection of charging direction current accumulation value1
1: Enable 0: Disable
CC_MON1_DET_EN=1: CC_MON1_DET=1 -> INTB=L, CC_MON1_DET=0 -> INTB=Hi-z
CC_MON1_DET_EN=0: INTB=Hi-z (regardless of CC_MON1_DET)

Address 3Ah: INT_EN2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Ah	INT_EN2	R/W	OCUR3_RES_EN	OCUR3_DET_EN	OCUR2_RES_EN	OCUR2_DET_EN	OCUR1_RES_EN	OCUR1_DET_EN	ALARM_OCUR1_RES_EN	ALARM_OCUR1_DET_EN
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7 : OCUR3_RES_EN
Interrupt Enable : Detection of discharging direction current measurement value3
1: Enable 0: Disable
OCUR3_RES_EN=1: OCUR3_RES=1 -> INTB=L, OCUR3_RES=0 -> INTB=Hi-z
OCUR3_RES_EN=0: INTB=Hi-z (regardless of OCUR3_RES)

Bit 6 : OCUR3_DET_EN
Interrupt Enable : Detection of charging direction current measurement value3
1: Enable 0: Disable
OCUR3_DET_EN=1: OCUR3_DET=1 -> INTB=L, OCUR3_DET=0 -> INTB=Hi-z
OCUR3_DET_EN=0: INTB=Hi-z (regardless of OCUR3_DET)

Bit 5 : OCUR2_RES_EN
Interrupt Enable : Detection of discharging direction current measurement value2
1: Enable 0: Disable
OCUR2_RES_EN=1: OCUR2_RES=1 -> INTB=L, OCUR2_RES=0 -> INTB=Hi-z
OCUR2_RES_EN=0: INTB=Hi-z (regardless of OCUR2_RES)

Bit 4 : OCUR2_DET_EN
Interrupt Enable : Detection of charging direction current measurement value2
1: Enable 0: Disable
OCUR2_DET_EN=1: OCUR2_DET=1 -> INTB=L, OCUR2_DET=0 -> INTB=Hi-z
OCUR2_DET_EN=0: INTB=Hi-z (regardless of OCUR2_DET)

Bit 3 : OCUR1_RES_EN
Interrupt Enable : Detection of discharging direction current measurement value1
1: Enable 0: Disable
OCUR1_RES_EN=1: OCUR1_RES=1 -> INTB=L, OCUR1_RES=0 -> INTB=Hi-z
OCUR1_RES_EN=0: INTB=Hi-z (regardless of OCUR1_RES)

Bit 2 : OCUR1_DET_EN
Interrupt Enable : Detection of charging direction current measurement value1
1: Enable 0: Disable
OCUR1_DET_EN=1: OCUR1_DET=1 -> INTB=L, OCUR1_DET=0 -> INTB=Hi-z
OCUR1_DET_EN=0: INTB=Hi-z (regardless of OCUR1_DET)

Bit 1 : ALARM_OCUR1_RES_EN
Alarm output Enable : Alarm detection of discharging direction current measurement value1
1: Enable 0: Disable
ALARM_OCUR1_RES_EN=1:
OCUR1_RES=1 -> ALARMB=L, OCUR1_RES=0 -> ALARMB=Hi-z
ALARM_OCUR1_RES_EN=0: ALRMB=Hi-z (regardless of OCUR1_RES)

Bit 0 : ALARM_OCUR1_DET_EN
Alarm output Enable : Alarm detection of charging direction current measurement value1
1: Enable 0: Disable
ALARM_OCUR1_DET_EN=1:
OCUR1_DET=1 -> ALARMB=L, OCUR1_DET=0 -> ALARMB=Hi-z
ALARM_OCUR1_DET_EN=0: ALRMB=Hi-z (regardless of OCUR1_DET)

Address 3Bh: INT_EN3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Bh	INT_EN3	R/W	-	CALIB_FIN_EN	-	CRCERR_DET_EN	-	REX_DET_EN	WAKE_RES_EN	WAKE_DET_EN
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 6 : CALIB_FIN_EN
Interrupt Enable :
Detection of calibration finish
1: Enable 0: Disable
CALIB_FIN_EN=1: CALIB_FIN=1 -> INTB=L, CALIB_FIN=0 -> INTB =Hi-z
CALIB_FIN_EN=0: INTB=Hi-z (regardless of CALIB_FIN)

Bit 5 : Reserved
When writing this register, "0" must be written

Bit 4 : CRCERR_DET_EN
Interrupt Enable :
Detection of CRC Error
1: Enable 0: Disable
CRCERR_DET_EN=1: CRCERR_DET=1 -> INTB=L, CRCERR_DET=0 -> INTB=Hi-z
CRCERR_DET_EN=0: INTB=Hi-z (regardless of CRCERR_DET)

Bit 2 : REX_DET_EN
Interrupt Enable :
Detection of Relax state
1: Enable 0: Disable
REX_DET_EN=1: REX_DET=1 -> INTB=L, REX_DET=0 -> INTB=Hi-z
REX_DET_EN=0: INTB=Hi-z (regardless of REX_DET)

Bit 1 : WAKE_RES_EN
Interrupt Enable :
Detection of under wake-up current measurement
1: Enable 0: Disable
WAKE_RES_EN=1: WAKE_RES=1 -> INTB=L, WAKE_RES=0-> INTB=Hi-z
WAKE_RES_EN=0: INTB=Hi-z (regardless of WAKE_RES)

Bit 0 : WAKE_DET_EN
Interrupt Enable :
Detection of over wake-up current measurement
1: Enable 0: Disable
WAKE_DET_EN=1: WAKE_DET=1 -> INTB=L, WAKE_DET=0 -> INTB=Hi-z
WAKE_DET_EN=0: INTB=Hi-z (regardless of WAKE_DET)

Address 3Ch: INT_REQ1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Ch	INT_REQ1	R/W	CC_MON4_RES	CC_MON4_DET	CC_MON3_RES	CC_MON3_DET	CC_MON2_RES	CC_MON2_DET	CC_MON1_RES	CC_MON1_DET
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7 : CC_MON4_RES
Read:
Interrupt Status for Detection of discharging direction current accumulation value4
1: Event occurred 0: No event
Bit is set to "1" when detect below condition
CC_CCNTD[31:8](17h+18h+19h+1A) ≤ CC_BATCAP4_TH[24:0](2Ch+2Dh+2Eh)

Write:
Interrupt status clear
1: Clear 0: Not Clear

Bit 6 : CC_MON4_DET
Read:
Interrupt Status for Detection of charging direction current accumulation value4
1: Event occurred 0: No event
Bit is set to "1" when detect below condition
CC_CCNTD[31:8](17h+18h+19h+1A) ≤ CC_BATCAP4_TH[24:0](2Ch+2Dh+2Eh)

Write:
Interrupt status clear
1: Clear 0: Not Clear

Bit 5 : CC_MON3_RES
Read:
Interrupt Status for Detection of discharging direction current accumulation value3
1: Event occurred 0: No event
Bit is set to "1" when detect below condition
CC_CCNTD[31:8](17h+18h+19h+1A) ≤ CC_BATCAP3_TH[24:0](29h+2Ah+2Bh)

Write:
Interrupt status clear
1: Clear 0: Not Clear

Bit 4 : CC_MON3_DET
Read:
Interrupt Status for Detection of charging direction current accumulation value3
1: Event occurred 0: No event
Bit is set to "1" when detect below condition
CC_CCNTD[31:8](17h+18h+19h+1A) > CC_BATCAP3_TH[24:0](29h+2Ah+2Bh)

Write:
Interrupt status clear
1: Clear 0: Not Clear

Bit 3 : CC_MON2_RES
Read:
Interrupt Status for Detection of discharging direction current accumulation value2
1: Event occurred 0: No event
Bit is set to "1" when detect below condition
CC_CCNTD[31:8](17h+18h+19h+1A) ≤ CC_BATCAP2_TH[24:0](26h+27h+28h)

Write:
Interrupt status clear
1: Clear 0: Not Clear

Bit 2 : CC_MON2_DET
Read:
Interrupt Status for Detection of charging direction current accumulation value2
1: Event occurred 0: No event
Bit is set to "1" when detect below condition
CC_CCNTD[31:8](17h+18h+19h+1A) > CC_BATCAP2_TH[24:0](26h+27h+28h)

Write:
Interrupt status clear
1: Clear 0: Not Clear

Bit 1 : CC_MON1_RES
Read:
Interrupt Status for Detection of discharging direction current accumulation value1
1: Event occurred 0: No event
Bit is set to "1" when detect below condition
CC_CCNTD[31:8](17h+18h+19h+1A) ≤ CC_BATCAP1_TH[24:0](23h+24h+25h)

Write:
Interrupt status clear
1: Clear 0: Not Clear

Bit 0 : CC_MON1_DET
Read:
Interrupt Status for Detection of charging direction current accumulation value1
1: Event occurred 0: No event
Bit is set to "1" when detect below condition
CC_CCNTD[31:8](17h+18h+19h+1A) > CC_BATCAP1_TH[24:0](23h+24h+25h)

Write:
Interrupt status clear
1: Clear 0: Not Clear

Address 3Dh: INT_REQ2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Dh	INT_REQ2	R/W	OCUR3_RES	OCUR3_DET	OCUR2_RES	OCUR2_DET	OCUR1_RES	OCUR1_DET	-	-
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7 : OCUR3_RES

Read:
Interrupt Status for Detection of discharging direction current measurement3

1: Event occurred 0: No event
Bit is set to "1" when detect below condition
CURCD_DIR+CURCD(13h+14h) ≤ OCURTHR3_DIR+OCURTHR3(33h+34h) and over the consecutive detection setting by OCURDUR3[1:0](35h)

Write:
Interrupt status clear

1: Clear 0: Not Clear

Bit 6 : OCUR3_DET

Read:
Interrupt Status for Detection of charging direction current measurement3

1: Event occurred 0: No event
Bit is set to "1" when detect below condition
CURCD_DIR+CURCD(13h+14h) > OCURTHR3_DIR+OCURTHR3(33h+34h) and over the consecutive detection setting by OCURDUR3[1:0](35h)

Write:
Interrupt status clear

1: Clear 0: Not Clear

Bit 5 : OCUR2_RES

Read:
Interrupt Status for Detection of discharging direction current measurement2

1: Event occurred 0: No event
Bit is set to "1" when detect below condition
CURCD_DIR+CURCD(13h+14h) ≤ OCURTHR2_DIR+OCURTHR2(31h+32h) and over the consecutive detection setting by OCURDUR2[1:0](35h)

Write:
Interrupt status clear

1: Clear 0: Not Clear

Bit 4 : OCUR2_DET

Read:
Interrupt Status for Detection of charging direction current measurement2

1: Event occurred 0: No event
Bit is set to "1" when detect below condition
CURCD_DIR+CURCD(13h+14h) > OCURTHR2_DIR+OCURTHR2(31h+32h) and over the consecutive detection setting by OCURDUR2[1:0](35h)

Write:
Interrupt status clear

1: Clear 0: Not Clear

Bit 3 : OCUR1_RES

Read:
Interrupt Status for Detection of discharging direction current measurement1

1: Event occurred 0: No event
Bit is set to "1" when detect below condition
CURCD_DIR+CURCD(13h+14h) ≤ OCURTHR1_DIR+OCURTHR1(2Fh+30h) over the consecutive detection setting by OCURDUR1[1:0](35h)

Write:
Interrupt status clear

1: Clear 0: Not Clear

Bit 2 : OCUR1_DET

Read:
Interrupt Status for Detection of charging direction current measurement1

1: Event occurred 0: No event
Bit is set to "1" when detect below condition
CURCD_DIR+CURCD(13h+14h) > OCURTHR1_DIR+OCURTHR1(2Fh+30h) and over the consecutive detection setting by OCURDUR1[1:0](35h)

Write:
Interrupt status clear

1: Clear 0: Not Clear

Address 3Eh: INT_REQ3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Eh	INT_REQ3	R/W	-	CALIB_FIN	OTP_DL_FIN	CRCERR_DET	-	REX_DET	WAKE_RES	WAKE_DET
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7: Reserved

Bit 6 : CALIB_FIN
- Read: Interrupt Status for calibration finish — 1: Event occurred 0: No event
- Write: Interrupt status clear — 1: Clear 0: Not Clear

Bit 5 : OTP_DL_FIN
- Read: Status for OTP data download finish — 1: Event occurred 0: No event
- Write: Interrupt status clear — 1: Clear 0: Not Clear

Bit 4 : CRCERR_DET
- Read: Interrupt status for CRC Error — 1: Event occurred 0: No event
- Write: Interrupt status clear — 1: Clear 0: Not Clear

Bit 2 : REX_DET
- Read: Interrupt status for Relax state — 1: Event occurred 0: No event. Bit is set to "1" when detect below condition CURCD[14:0](13h+14h) ≤ { 7'd0, REX_CURCD_TH[7:0](36h) } and after detection time setting by REX_DUR[1:0](35h)
- Write: Interrupt status clear — 1: Clear 0: Not Clear

Bit 1 : WAKE_RES
- Read: Interrupt status for Detection of under wake-up current — 1: Event occurred 0: No event. Bit is set to "1" when detect below condition CURCD[14:0](13h+14h) ≤ { 7'd0, WAKE_CURCD_TH[7:0](37h) } and over the consecutive detection setting by WAKE_COUNT[1:0](38h)
- Write: Interrupt status clear — 1: Clear 0: Not Clear

Bit 0 : WAKE_DET
- Read: Interrupt status for Detection of over wake-up current — 1: Event occurred 0: No event. Bit is set to "1" when detect below condition CURCD[14:0](13h+14h) > { 7'd0, WAKE_CURCD_TH[7:0](37h) } and over the consecutive detection setting by WAKE_COUNT[1:0](38h)
- Write: Interrupt status clear — 1: Clear 0: Not Clear

Address 3Fh: PAGE_SEL Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Fh	PAGE_SEL	R/W	HOSC_ON	-	-	-	-	-	Reserved	
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7 : HOSC_ON — Built-in OSC force enable
0: Built-in OSC normal operation (default)
1: Built-in OSC turns ON by force

Force Built-in OSC to turn on when HOSC_ON=1.
Before transitioning from SSHDN mode to another mode, set HOSC_ON = 1 and the built-in OSC will turn ON.
When HOSC_ON=0, built-in OSC operate normally.
The built-in OSC will turn on in WAKE, OTP, IDLE, NORMAL, SLEEP modes. (Refer to Table 2-1)

Bit 1-0: Reserved[1:0]
When writing this register, always write "00" to these bits.

I/O Equivalence Circuit

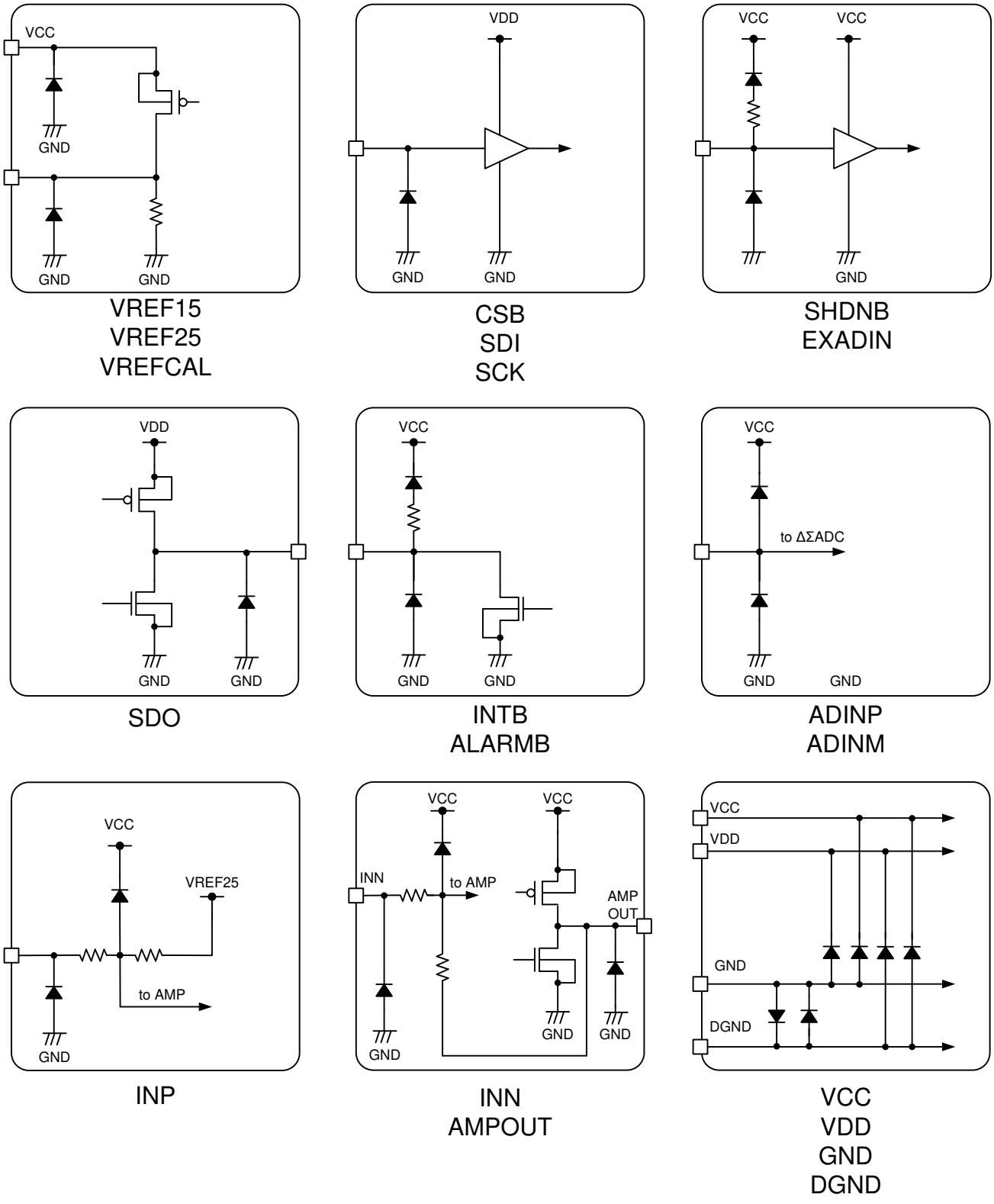
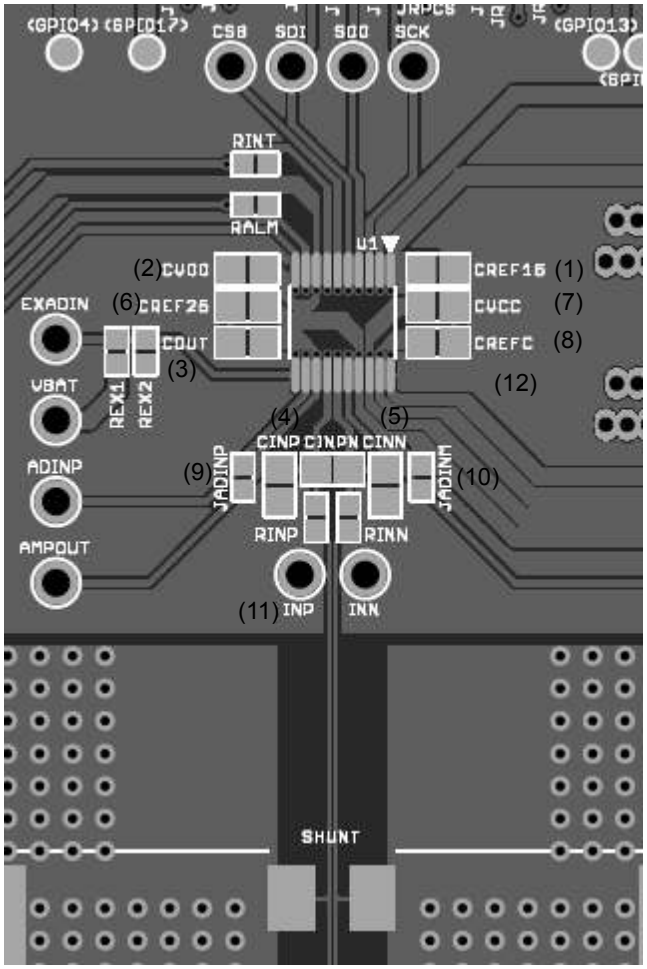


Figure 7. I/O Equivalence Circuit

Layout

Optimum performance of this product cannot be achieved without taking the circuit board layout into consideration.
The following points are important.

(1) Place CREF15 as close as possible to the VREF15 pin and GND.
(2) Place CVDD as close as possible to the VDD pin and GND.
(3) Place COUT as close as possible to the AMPOUT pin and GND.
(4) Place CINP as close as possible to the INP pin and GND.
(5) Place CINN as close as possible to the INN pin and GND.
(6) Place CREF25 as close as possible to the VREF25 pin and GND.
(7) Place CVCC as close as possible to the VCC pin and GND.
(8) Place CREFC as close as possible to the VREFCAL pin and GND.
(9) Connect the ADINP pin and the AMPOUT pin as close as possible.
(10) Connect the ADINM pin and the VREF25 pin as close as possible.
(11) Draw a line the INP pin and the INN pin as equal as possible.
(12) Draw a ground line as thick as possible for the low impedance.



Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**

   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes -continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

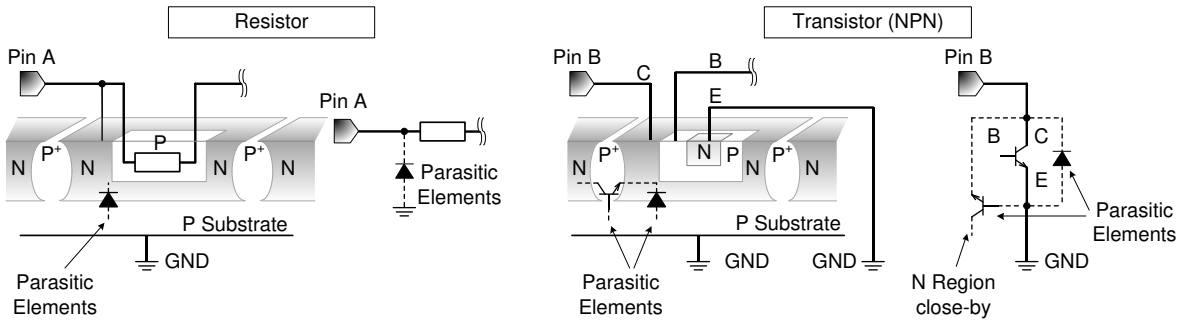


Figure 8. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

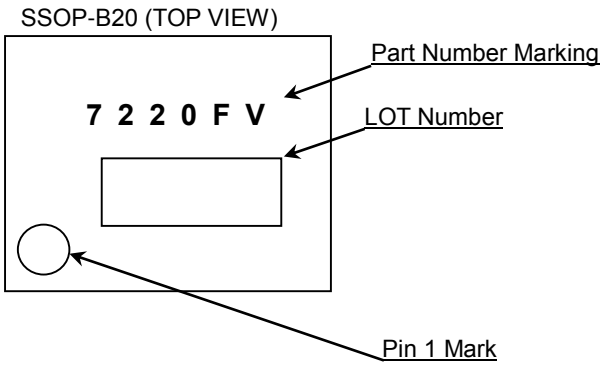
B D 7 2 2 0 F V - C E 2

Part Number

Package
FV: SSOP-B20

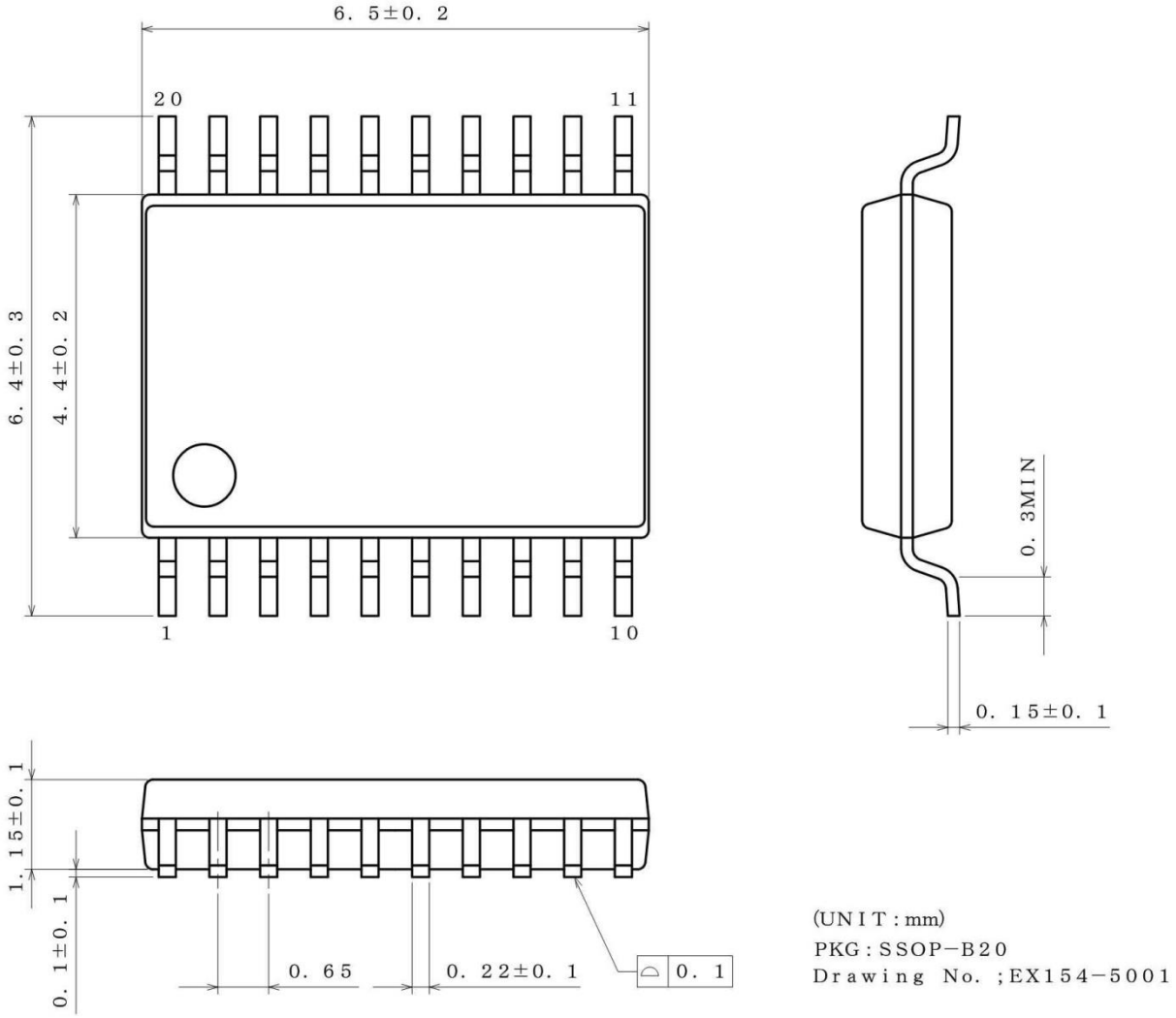
Product rank
C: for Automotive applications
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram



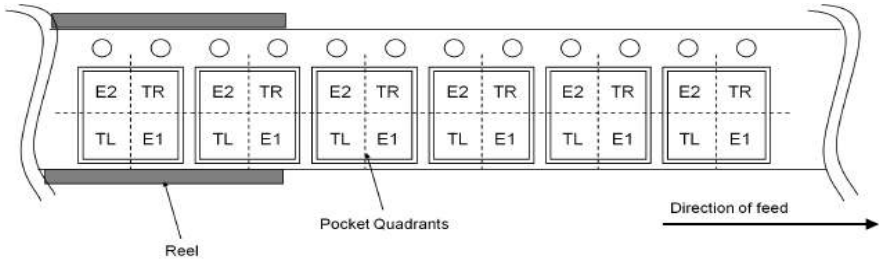
Physical Dimension and Packing Information

Package Name	SSOP-B20



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision Number	Description
17. Dec. 2019	001	New Release
24. Sep. 2020	002	Page.16, Page.17 Bit Mask Function of Accumulation Current Corrected Figure 1-8 typo of “image of bits mask” and updated Figure 1-8. Add explanatory text. Add explanatory of example for CCNTD error complement.

Notice

Precaution on using ROHM Products

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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