BLC9G10XS-120A

Power LDMOS transistor

Rev. 1 — 29 November 2018

AMPLEON

Product data sheet

1. Product profile

1.1 General description

120 W LDMOS power transistor for base station applications at frequencies from 920 MHz to 960 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty application demo circuit.

Test signal	f	I_{Dq}	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	925 to 960	150	28	18	20	50	−28 [1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 10.5 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

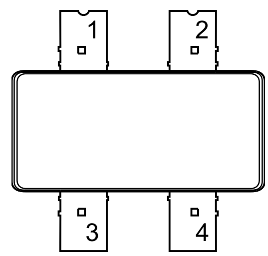
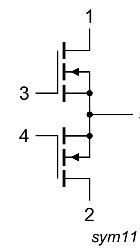
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Designed for broadband operation
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifier for W-CDMA base stations and multi carrier applications in the 920 MHz to 960 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC9G10XS-120A	-	air cavity plastic earless flanged package; 4 leads	SOT1273-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; I_{Dq} = 120 mA; $V_{GS(am)peak}$ = 0.8 V		
		P_L = 18 W	0.349	k/W
		P_L = 28.2 W	0.301	k/W

6. Characteristics

Table 6. DC characteristics
T_j = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.4 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 40 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 240 mA	1.5	2.17	2.5	V
I_{DSS}	drain leakage current	V_{DS} = 28 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	8	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 2 A	-	2.91	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 1.4 A	-	326	-	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.81 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 81mA	1.5	1.9	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 486 mA	1.5	2.0	2.5	V
I_{DSS}	drain leakage current	V_{DS} = 28 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	15.7	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 2 A	-	5.75	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 1.4 A	-	165	-	mΩ

Table 7. RF characteristics
Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on CCDF; 3GPP test model 1; 64 DPCH; f_1 = 927.5 MHz; f_3 = 957.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 120 mA; $V_{GS(amp)peak}$ = 0.8 V; T_{case} = 25 °C; unless otherwise specified; in a Doherty production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 18 W	19.8	21	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 18 W	44	49	-	%
RL_{in}	input return loss	$P_{L(AV)}$ = 18 W	-	−12	−8	dB
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 18 W	-	−32	−27	dBc

Table 8. RF characteristics
Test signal: pulsed CW; t_p = 100 μs; δ = 10 %; f = 960 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 120 mA (main); $V_{GS(amp)peak}$ = 0.8 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 925 MHz to 960 MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression		125	140	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC9G10XS-120A is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 120 mA; $V_{GS(amp)peak}$ = 0.8 V; P_L = 100 W (CW); f = 925 MHz; tested on the Doherty development circuit.

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 240 mA (main); V_{DS} = 28 V; typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [3]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
920	1.15 – j5.18	4.33 + j1.33	66.0	67.8	22.7
940	1.59 – j5.92	4.33 + j1.33	65.0	67.6	23.0
960	2.56 – j6.94	3.93 + j1.22	63.0	64.8	22.8
Maximum drain efficiency load					
920	1.15 – j5.18	3.89 + j4.44	46.8	78.4	25.1
940	1.59 – j5.92	3.09 + j4.94	38.0	78.5	25.8
960	2.56 – j6.94	3.24 + j4.34	41.7	75.7	25.3

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

[3] At 6 dB OBO.

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 480 mA (peak); V_{DS} = 28 V; typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [3]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
920	1.81 – j5.01	2.32 – j0.81	149.0	70.2	22.4
940	2.05 – j5.52	2.40 – j0.27	150.3	73.55	22.88
960	2.78 – j6.29	2.32 – j0.81	141.0	69.5	22.7
Maximum drain efficiency load					
920	1.81 – j5.01	2.30 + j1.69	79.4	84.3	26.2
940	2.05 – j5.52	2.32 + j1.69	97.7	84.5	25.8
960	2.78 – j6.29	2.16 + j1.33	91.2	84.0	25.8

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

[3] At 6 dB OBO.

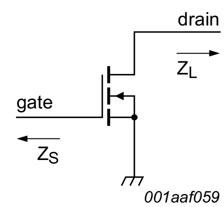
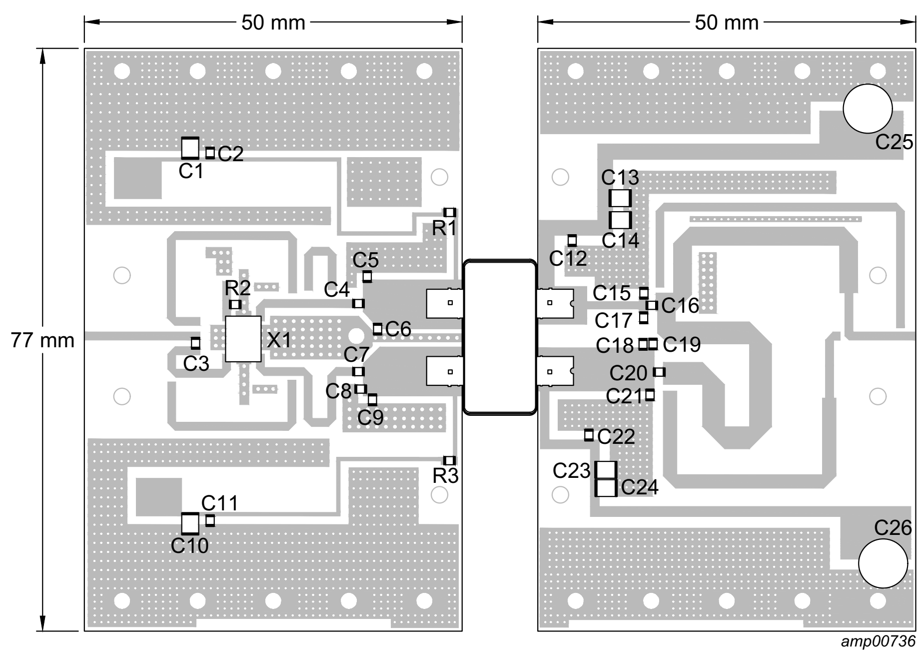


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): RO4350B: ε_r = 3.5; thickness = 0.508 mm; thickness copper plating = 35 μm. See Table 11 for a list of components.

Fig 2. Component layout

Table 11. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C10, C13, C14, C23, C24	multilayer ceramic chip capacitor	4.7 μF, 100 V	Murata 1210
C2, C3, C4, C7, C11, C12, C22	multilayer ceramic chip capacitor	100 pF [1]	ATC600F
C5	multilayer ceramic chip capacitor	6.8 pF [1]	ATC600F
C6	multilayer ceramic chip capacitor	3.6 pF [1]	ATC600F
C8, C15	multilayer ceramic chip capacitor	3.0 pF [1]	ATC600F
C9, C19	multilayer ceramic chip capacitor	4.3 pF [1]	ATC600F
C16	multilayer ceramic chip capacitor	33 pF [1]	ATC600F

Table 11. List of components *...continued*

See Figure 2 for component layout.

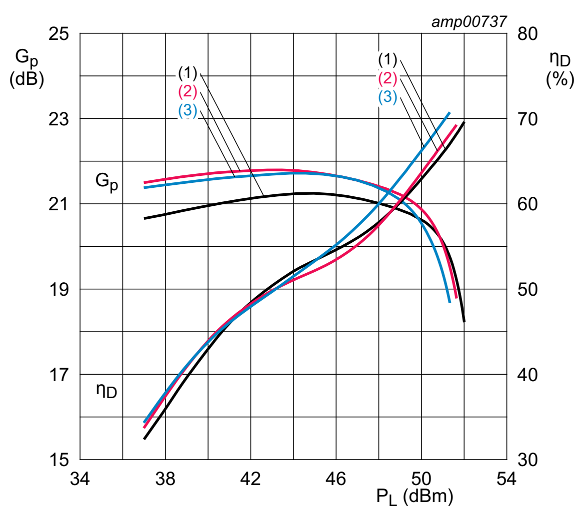
Component	Description	Value	Remarks
C17, C18	multilayer ceramic chip capacitor	3.9 pF [1]	ATC600F
C20	multilayer ceramic chip capacitor	2.0 pF [1]	ATC600F
C21	multilayer ceramic chip capacitor	6.2 pF [1]	ATC600F
C25, C26	electrolytic capacitor	1000 μF, 100 V	
R1, R3	chip resistor	5.1 Ω	SMD 0805
R2	chip resistor	50 Ω	SMD 0805
X1	asymmetric coupler	2 dB	RN2 CMX09Q02

[1] Murata or capacitor of same quality

7.4 Graphical data

All data measured on the Doherty development circuit.

7.4.1 CW



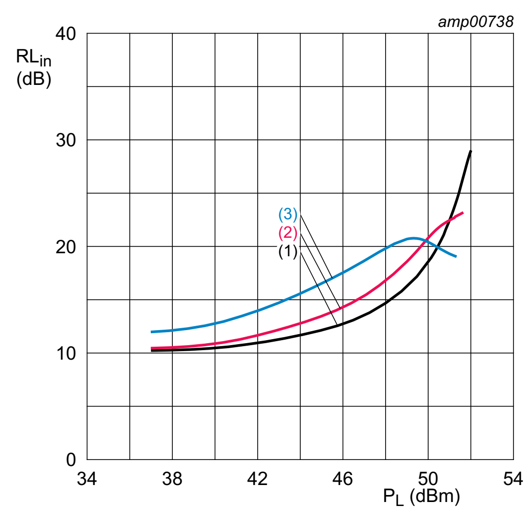
V_{DS} = 28 V; I_{Dq} = 120 mA; $V_{GS(amp)peak}$ = 0.8 V.

(1) f = 925 MHz

(2) f = 943MHz

(3) f = 960 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 120 mA; $V_{GS(amp)peak}$ = 0.8 V; t_p = 100 μs; δ = 10 %.

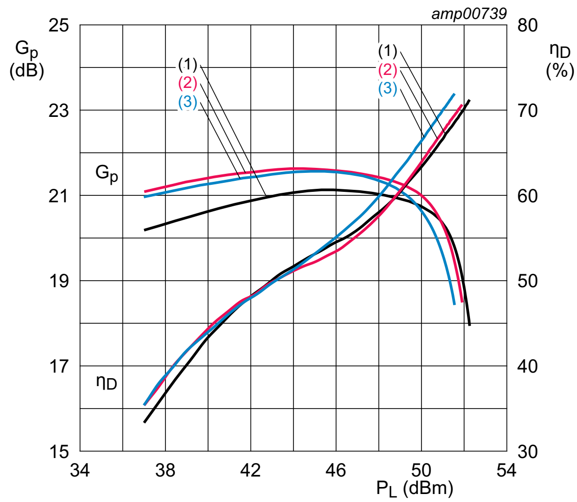
(1) f = 925 MHz

(2) f = 943 MHz

(3) f = 960 MHz

Fig 4. Input return loss as a function of output power; typical values

7.4.2 Pulsed CW



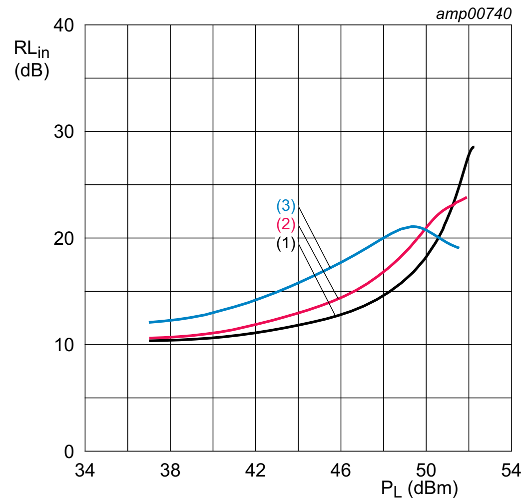
V_{DS} = 28 V; I_{Dq} = 120 mA; $V_{GS(amp)peak}$ = 0.8 V; t_p = 100 μs; δ = 10 %.

(1) f = 925 MHz

(2) f = 943MHz

(3) f = 960 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 120 mA; $V_{GS(amp)peak}$ = 0.8 V; t_p = 100 μs; δ = 10 %.

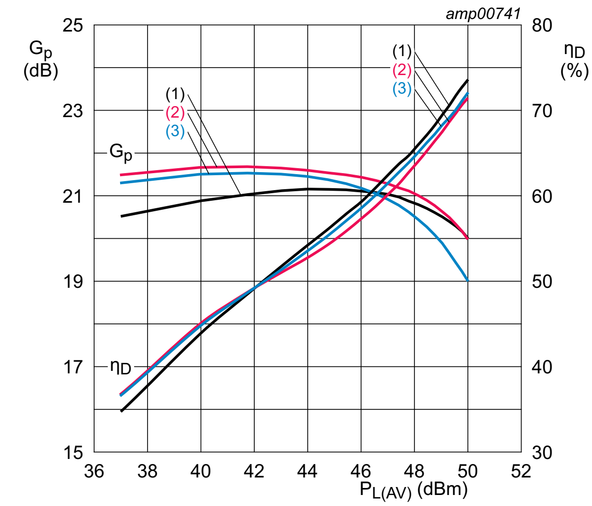
(1) f = 925 MHz

(2) f = 943 MHz

(3) f = 960 MHz

Fig 6. Input return loss as a function of output power; typical values

7.4.3 1-Carrier W-CDMA



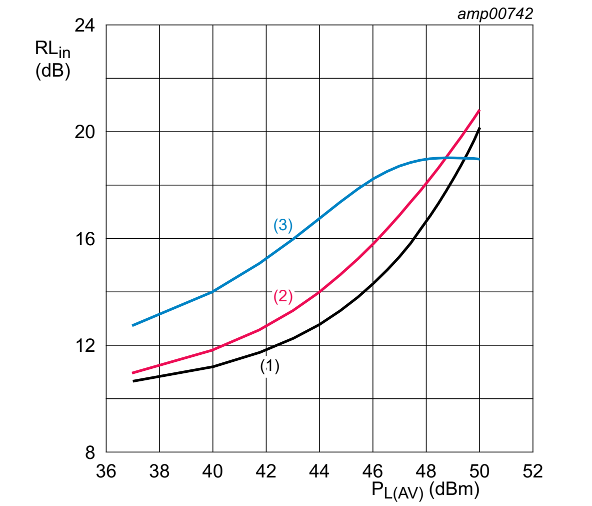
V_{DS} = 28 V; I_{Dq} = 120 mA; $V_{GS(amp)peak}$ = 0.8 V; 46 % clipping.

(1) f = 925 MHz

(2) f = 943 MHz

(3) f = 960 MHz

Fig 7. Power gain and drain efficiency as function of average output power; typical values



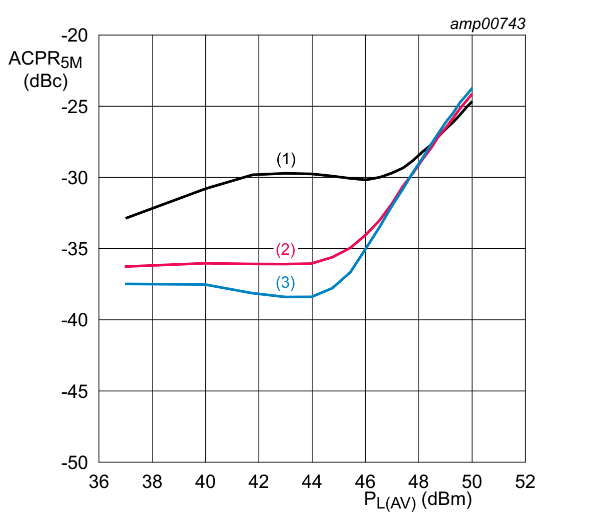
V_{DS} = 28 V; I_{Dq} = 120 mA; $V_{GS(amp)peak}$ = 0.8 V; 46 % clipping.

(1) f = 925 MHz

(2) f = 943MHz

(3) f = 960 MHz

Fig 8. Input return loss as a function of average output power; typical values



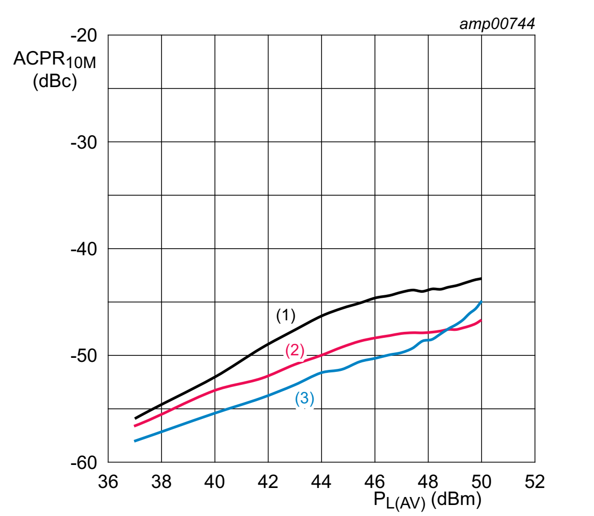
V_{DS} = 28 V; I_{Dq} = 120 mA; $V_{GS(amp)peak}$ = 0.8 V; 46 % clipping.

(1) f = 925 MHz

(2) f = 943 MHz

(3) f = 960 MHz

Fig 9. Adjacent channel power ratio (5 MHz) as a function of average output power; typical values



V_{DS} = 28 V; I_{Dq} = 120 mA; $V_{GS(amp)peak}$ = 0.8 V; 46 % clipping.

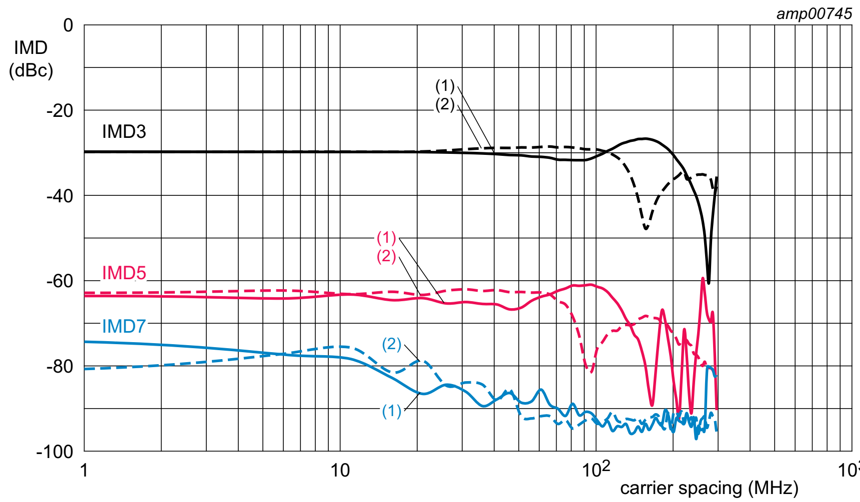
(1) f = 925 MHz

(2) f = 943 MHz

(3) f = 960 MHz

Fig 10. Adjacent channel power ratio (10 MHz) as a function of average output power; typical values

7.4.4 2-Tone VBW



V_{DS} = 28 V; I_{Dq} = 120 mA; $V_{GS(amp)peak}$ = 0.8 V; f_c = 940 MHz.

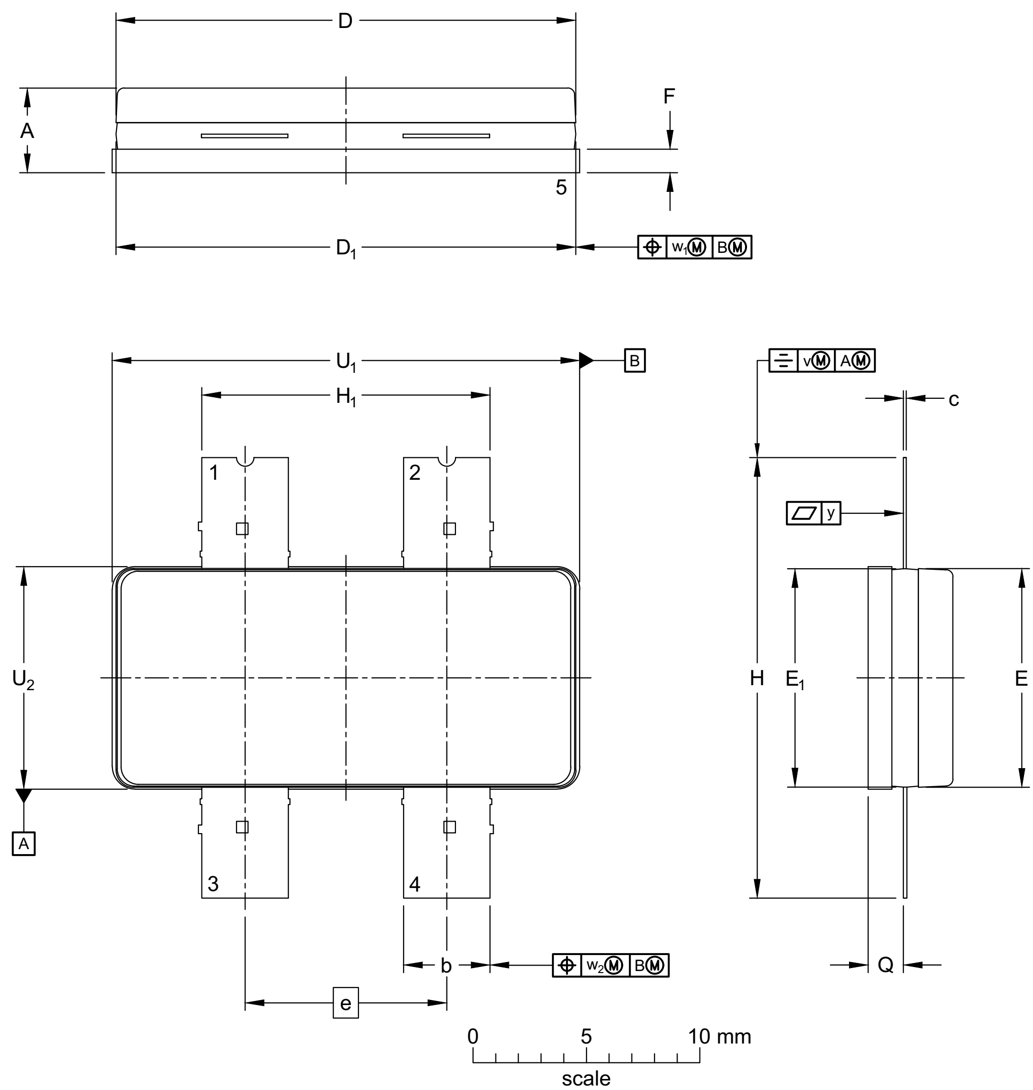
(1) IMD low

(2) IMD high

Fig 11. VBW capability on Doherty development RF test circuit

8. Package outline

Air cavity plastic earless flanged package; 4 leads SOT1273-1



Dimensions

Unit		A	b	c	D	D_1	E	E_1	e	F	H	H_1	Q[1]	U_1	U_2	v	w_1	w_2	y
mm	max	4.01	3.91	0.18	20.42	20.37	9.80	9.75		1.14	19.53	12.83	1.68	20.70	9.91	0.50	0.50	0.50	0.10
	nom								8.89										
	min	3.40	3.71	0.13	20.12	20.17	9.50	9.55		0.94	19.33	12.57	1.45	20.50	9.70				

Note:
1. Dimension Q is measured at 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1273-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1273-1						17-01-12

Fig 12. Package outline SOT1273-1

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 12. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 13. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9G10XS-120A v.1	20181129	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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For more information, please visit: **http://www.ampleon.com**

For sales office addresses, please visit: **http://www.ampleon.com/sales**

14. Contents

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Date of release: 29 November 2018

Document identifier: BLC9G10XS-120A