HMC857LC5

v04.0914

14 Gbps, 2 x 2 CROSSPOINT SWITCH WITH PROGRAMMABLE OUTPUT VOLTAGE

Typical Applications

The HMC857LC5 is ideal for:

- SONET OC-192 and 10 GbE
- 16G Fiber Channel
- Networking & Storage
- Dual 2:1 Selector
- 1:2 Fanout with Input Mux

Features

Supports High Data Rates: up to 14 Gbps

Differential or Single-Ended Inputs / Outputs

Fast Rise and Fall Times: 21 / 21 ps

Low Power Consumption: 345 mW typ.

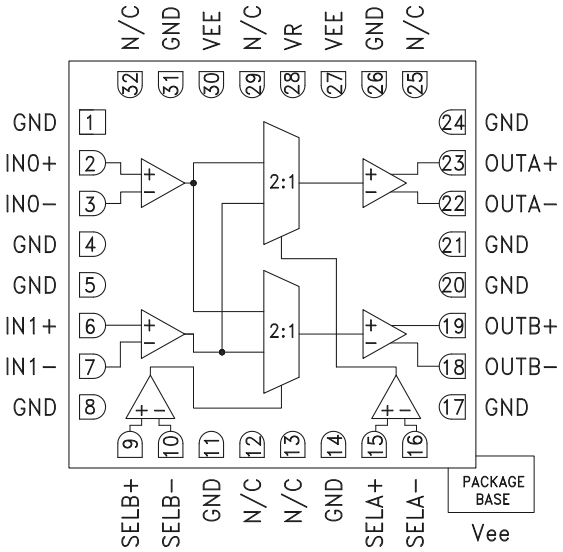
Programmable Differential
Output Voltage Swing: 475 - 1200 mVp-p

Propagation Delay: 117 ps

Single Supply: -3.3 V

32 Lead Ceramic 5 x 5 mm SMT Package: 25 mm^2

Functional Diagram



General Description

The HMC857LC5 is a 2x2 Crosspoint Switch designed to support data transmission rates of up to 14 Gbps and selector port operation up to 14 GHz. The selector routes the differential inputs to either one or both of the desired outputs upon assertion of the appropriately selected port.

All differential inputs to the HMC857LC5 are CML and terminated on-chip with 50 Ohms to the positive supply, GND, and may be DC or AC coupled. Outputs can be connected directly to a 50 Ohm ground-terminated system or drive devices with CML logic input. The HMC857LC5 also features an output level control pin, VR, which allows for loss compensation or signal level optimization. The HMC857LC5 operates from a single -3.3 V supply and is available in ROHS-compliant 3x3 mm SMT package.

Electrical Specifications, T_A = +25 °C, Vee = -3.3 V, Vr = 0 V

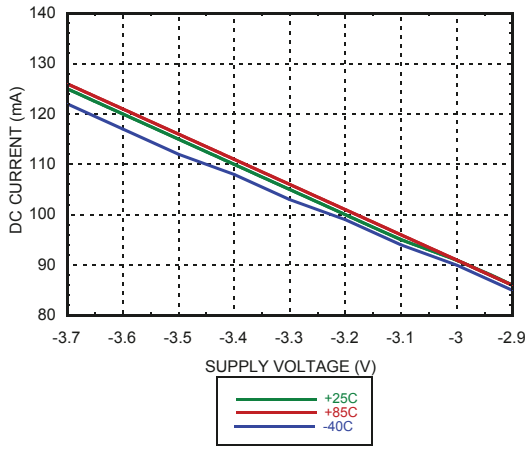
Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		-3.6	-3.3	-3.0	V
Power Supply Current			105		mA
Maximum Data Rate			14		Gbps
Maximum Select Rate			14		GHz
Input Voltage Range		-1.5		0.5	V
Input Differential Range		0.1		2.0	Vp-p
Input Return Loss	Frequency <20 GHz		10		dB
Output Amplitude	Single-Ended, peak-to-peak		500		mVp-p
	Differential, peak-to-peak		1000		mVp-p
Output High Voltage			-10		mV
Output Low Voltage			-510		mV

Electrical Specifications (continued)

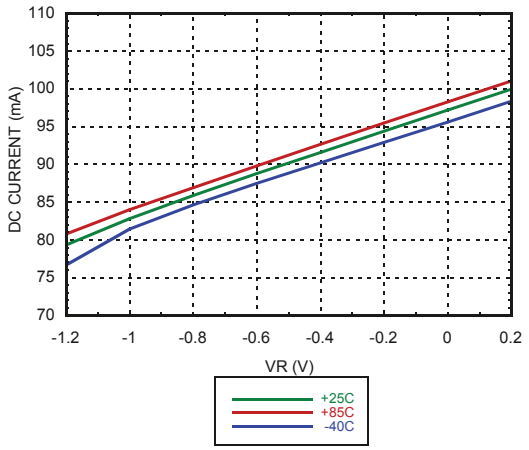
Parameter	Conditions	Min.	Typ.	Max	Units
Output Rise / Fall Time	Differential, 20% - 80%		21		ps
Output Return Loss	Frequency <22 GHz		10		dB
Random Jitter, Jr	rms [1]		0.08	0.11	ps rms
Deterministic Jitter, Jd	peak-to-peak, 2^{15}-1 PRBS input [1]		2		ps, p-p
Propagation Delay, A or B to D_{OUT}, td			117		ps
Propagation Delay Select to Data, tds			114		ps
Set Up & Hold Time, t_{SH}			5		ps

[1] Added jitter calculated by de-embedding the source's jitter at 13 Gbps, 2^{15} -1 PRBS input.

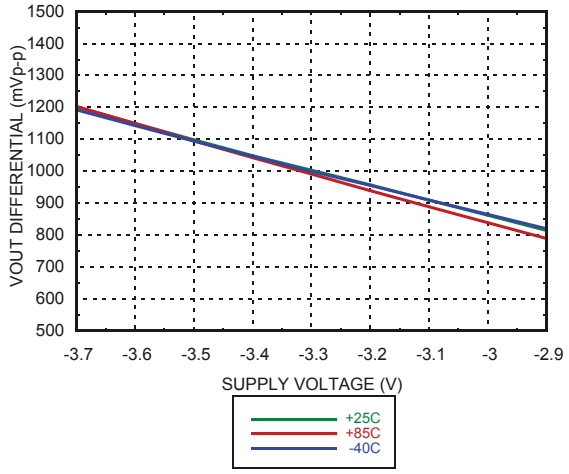
DC Current vs. Supply Voltage [1][2]



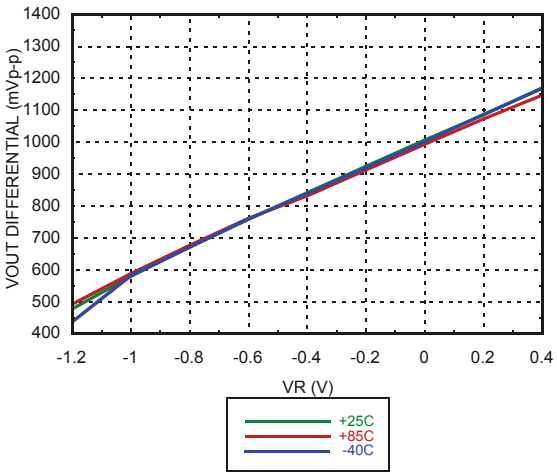
DC Current vs. VR [2][3]



Output Differential Voltage vs. Supply Voltage [1][2]



Output Differential Voltage vs. VR [2][3]



[1] VR = 0.0 V [2] Frequency = 13 GHz [3] Vee = -3.3 V

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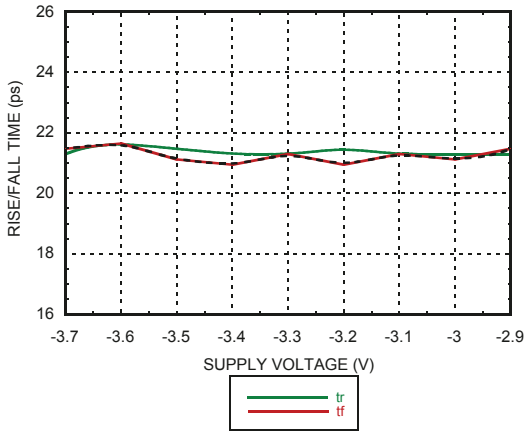
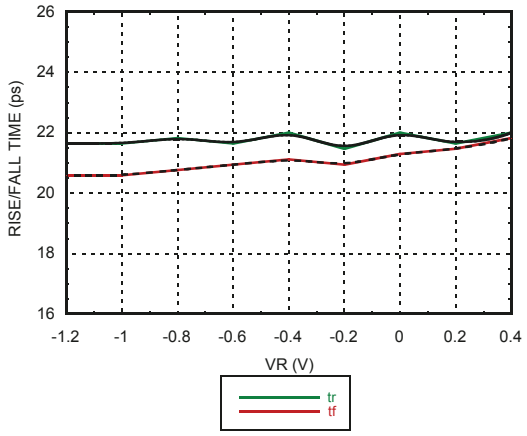
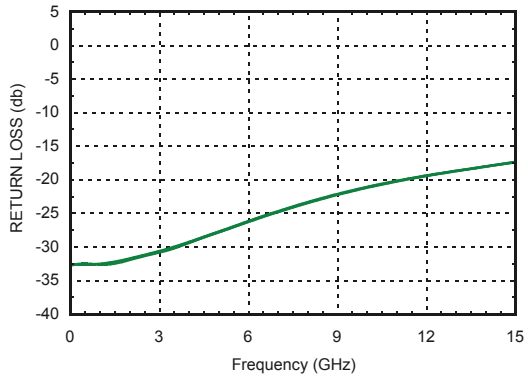
Rise / Fall Time vs. Supply Voltage [1] [2]



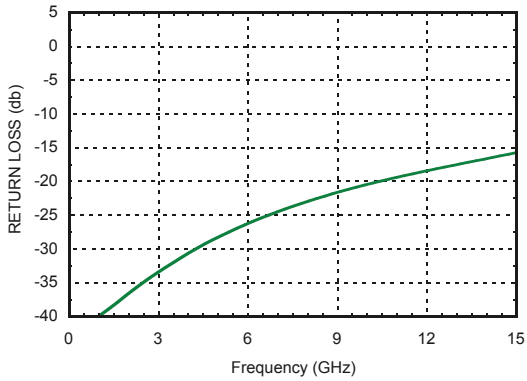
Rise / Fall Time vs. VR [2] [3]



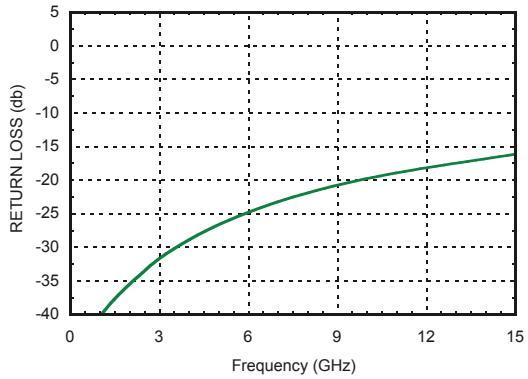
Select Input Return Loss vs. Frequency [1] [3] [4]



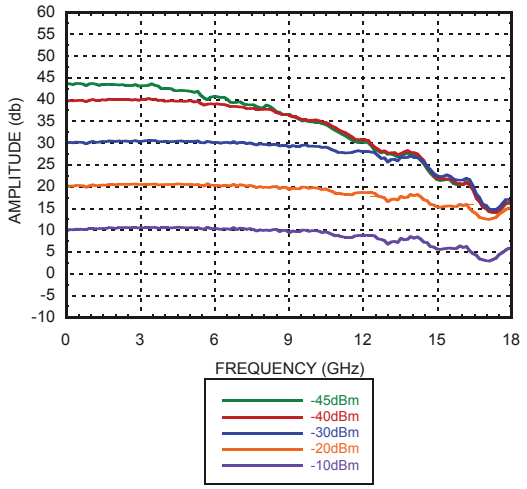
Data Input Return Loss vs. Frequency [1] [3] [4]



Output Return Loss vs. Frequency [1] [3] [4]

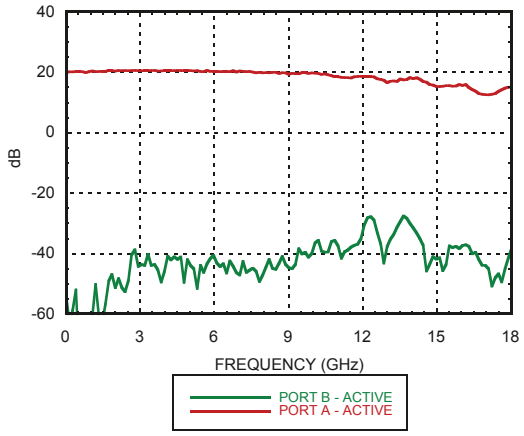


Response vs. Input Power [1] [3] [5]

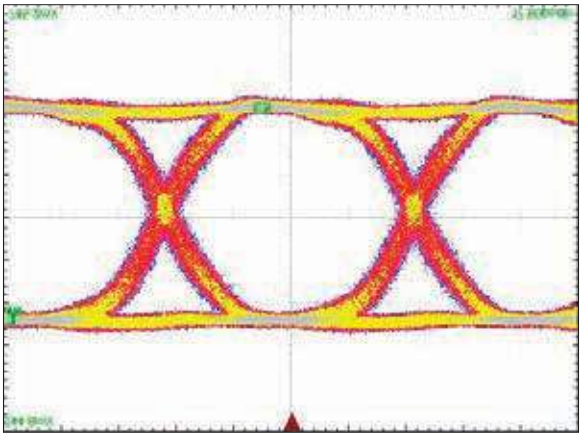


[1] VR = 0.0 V [2] Frequency = 13 GHz [3] Vee = -3.3 V [4] Device measured on evaluation board with gating
[5] Device measured on evaluation board with port extensions

Isolation [1] [2] [3]

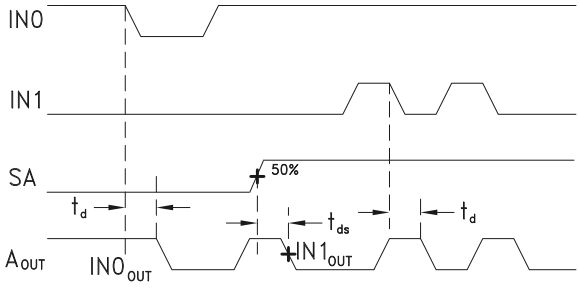


Eye Diagram



[1] Test Conditions:
Waveform generated with a differential 400 mV Agilent N4903A J-Bert with a 13 Gbps PN 2^{15} -1 signal.
Eye Diagram data presented on a Tektronix CSA 8000

Timing Diagram



td = propagation delay, IN to Aout
tds = propagation delay, Select to DataOut

Truth Table

Inputs		Outputs
SB	SA	DP
X	L	IN0 ->A
X	H	IN1 ->A
L	X	IN0 ->B
H	X	IN1 -> B
H = Positive voltage level L = Negative voltage level		
Notes: D = DP - DN IN0 = IN0P - IN0N IN1 = IN1P - IN1N		

[1] VR = 0.0 V [2] Device measured on evaluation board with port extensions [3] Vee = -3.3 V

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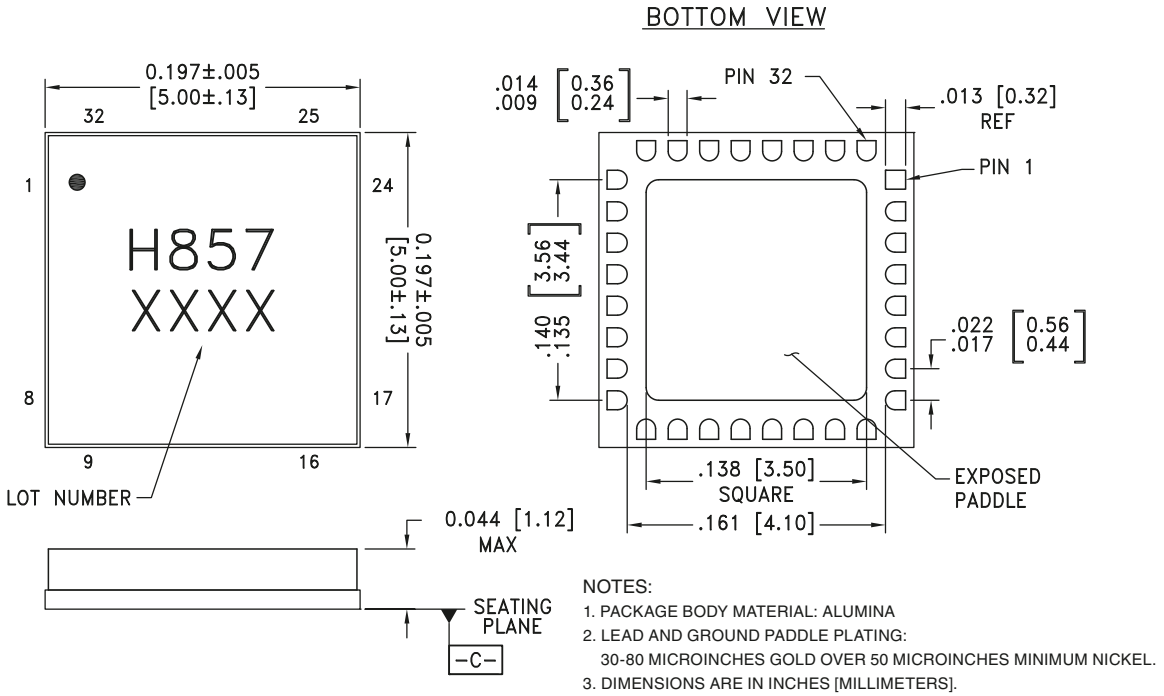
Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.75 V to +0.5 V
Input Signals	-2.0 V to 0.5 V
Output Signals	-1.5 V to 0.5 V
Junction Temperature	125 °C
Continuous Pdiss (T = 85 °C (derate 33.0 mW/°C above 85 °C)	1.33 W
Thermal Resistance ($R_{th\ j\text{-}p}$) Worst case device to package paddle	30 °C/W
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C
ESD Sensitivity (HBM)	Class 1B

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



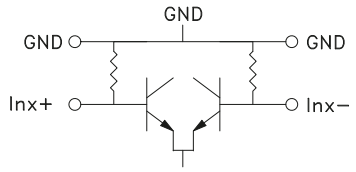
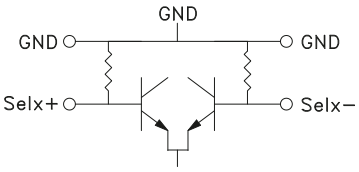
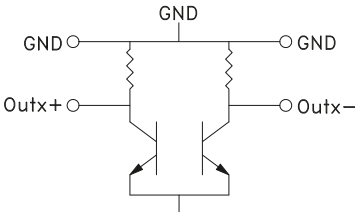
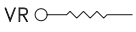
NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO Vee.

Package Information

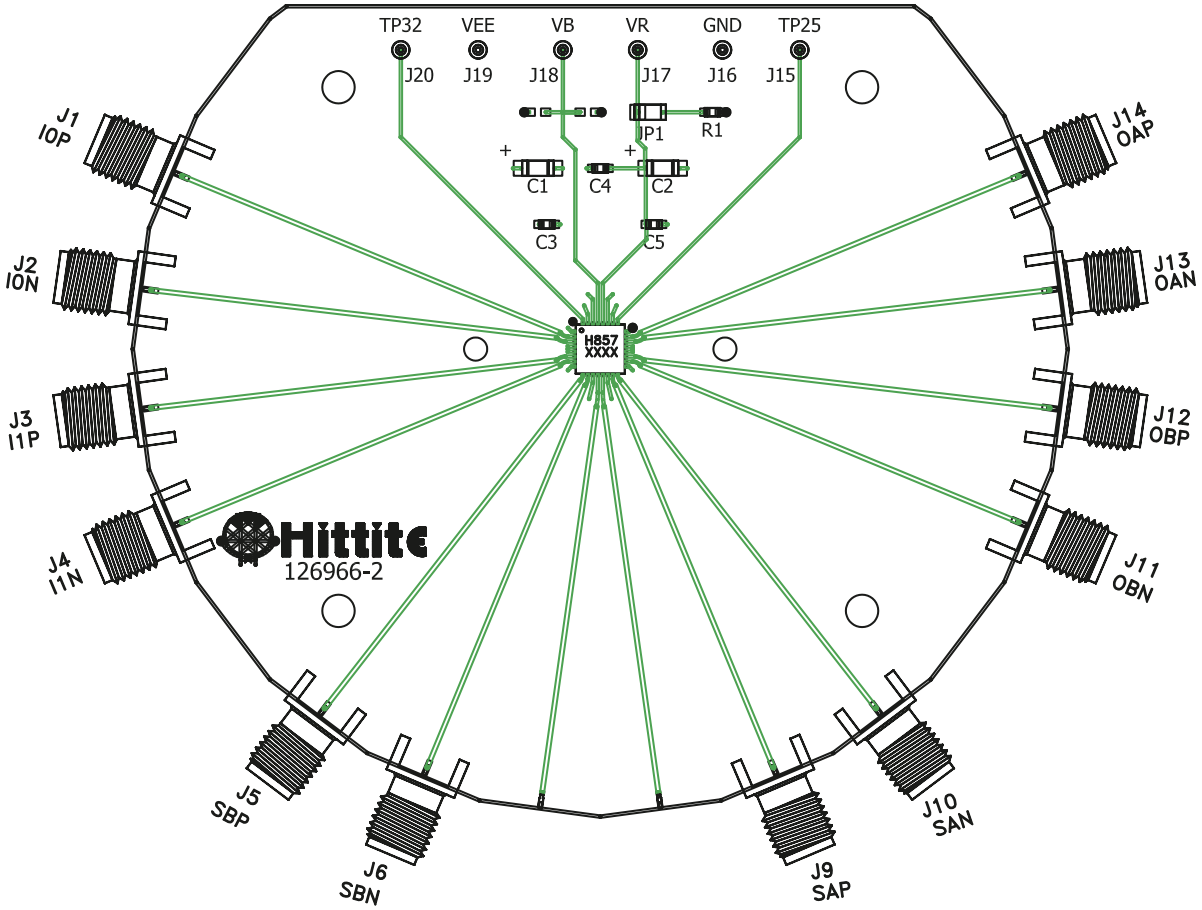
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC857LC5	Alumina, White	Gold over Nickel	MSL3 [1]	H857 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 11, 14, 17, 20, 21, 24	GND	Signal Grounds	
2, 3, 6, 7	In0+, In0-, In1+, In1-	Differential Inputs: Current Mode Logic (CML) referenced to positive supply.	
9, 10, 15, 16	SelB+, SelB-, SelA+, SelA-	Differential Select Inputs: Current Mode Logic (CML) referenced to positive supply.	
12, 13, 25, 29, 32	N/C	No connection necessary. These pins may be connected to RF/DC ground without affecting performance.	
18, 19, 22, 23	OutB-, OutB+, OutA-, OutA+	Differential Outputs: Current Mode Logic (CML) referenced to positive supply.	
26, 31	GND	Supply Ground	
27, 30 Package Base	Vee	These pins and the exposed paddle must be connected to the negative voltage supply.	
28	VR	Output level control. Output level may be increased or decreased by applying a voltage to VR per “Output Differential vs. VR” plot.	

Evaluation PCB



List of Materials for Evaluation PCB 126968 [1]

Item	Description
J1 - J6, J9 - J14	PCB Mount SMA RF Connectors
J15 - J20	DC Pin
JP1	0.1" Header with Shorting Jumper
C1, C2	4.7 µF Capacitor, Tantalum
C3 - C5	330 pF Capacitor, 0402 Pkg.
R1	10 Ohm Resistor, 0603 Pkg.
U1	HMC857LC5 2 x 2 Crossbar Switch
PCB [2]	126966 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed package base should be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to GND for normal operation.

Application Circuit