Introduction

The evaluation board is designed to help the customer evaluate the 5L35023 device, the latest addition to the family of programmable devices in IDT's Timing portfolio. When the board is connected to a PC running IDT Timing Commander™Software through USB, the device can be configured and programmed to generate different combination of frequencies.

Note: Timing Commander ™Software user guide and download can be found in following link.
http://www.idt.com/products/clocks-timing/timing-commander-software-download-resource-guide

Board Overview

Use Figure 1 and Table 1 to identify: USB connector, input and output frequency SMA connectors

.

Figure 1. EVK5L35023 Evaluation board review

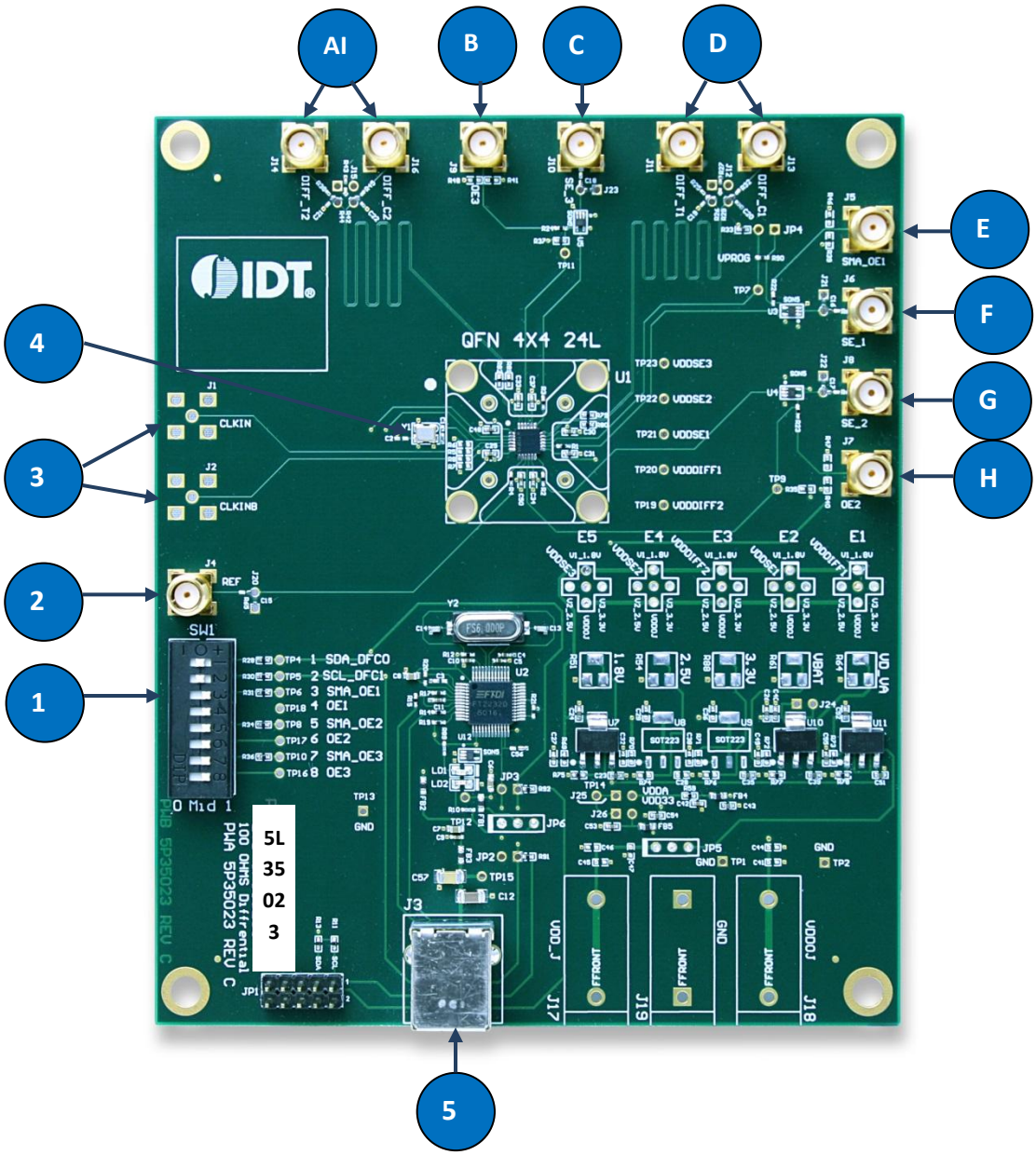


Table 1: Evaluation board Pins and Functions

S.No	Name	On-Board Connector Label	Function
1	DIP switch	SW1	This is used to set outputs enable/disable on the IC and switches DFC in different configurations
2	Reference output	REF	This is the reference or buffered output from the crystal
3	Differential clock input	CLKIN/CLKINB	A differential clock can be connected as source for the device
3 (contd.)	Single-ended clock input	CLKINB	A Single-ended clock can be connected as source for the device using CLKINB only
4	Crystal, 25 MHz		This crystal is used as a reference source for the clock signal
5	USB connector	Y1	Connect this USB to your PC to run IDT Timing Commander
A	Differential output#2	DIFF_T2/C2	This can be a differential pair, or two single-ended outputs. By default, it's an LPHCSL differential output.
B	Output-enable connector	OE3	This port can be used in Pro-active Power Saving(PPS) mode
C	Single-ended output	SE_3	This is the single-ended output. By default it's an LVCMOS single-ended output
D	Differential output#1	DIFF_T1/C1	This can be a differential pair, or two single-ended outputs. By default, it's LPHCSL differential output.
E	Output-enable connector	SMA_OE1	This port can be used in Pro-active Power Saving(PPS) mode
F	Single-ended output	SE_1	This is the single-ended output. By default it's an LVCMOS single-ended output
G	Single-ended output	SE_2	This is the single-ended output. By default it's an LVCMOS single-ended output
H	Output enable connector	OE2	This port can be used in Pro-active Power Saving(PPS) mode

Board Power Supply

Power Supply Options:

The core voltage includes a digital voltage VDD1.8V and an analog voltage VDDA. Both core voltages is powered by USB with 1.8V voltage regulator as default.

- **USB Power Supply only** – When the board is connected to a PC through a USB cable, on-board voltage regulators will generate a 1.8V for the device. USB power source is recommended because it's available right from your laptop.

Output Clock Voltages

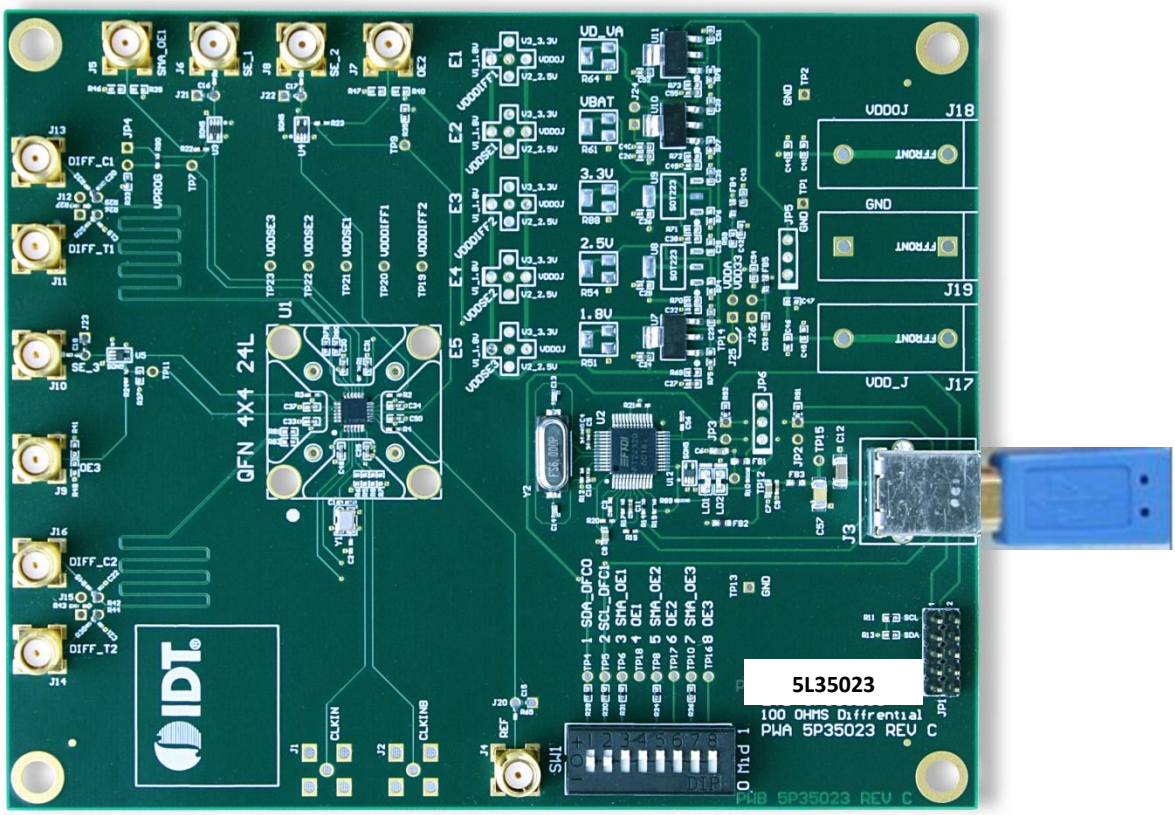
Output clock voltages VDDOx are also been regulated to 1.8V from USB power.

Connecting the Board

The board is connected to a PC through a USB connector for configuring and programming the device, as shown in Figure 2 below. The USB interface will also provide +5V power supply to the board, from which on-board voltage regulators generate various voltages for the core as well as for each output.

Note: The USB port only supports USB 2.0; USB 3.0 is not supported at this time.

Figure 2. Connecting the Board on USB Port for Communication with Timing Commander Software



On-Board Crystal

A 25MHz crystal is installed on the board. It is used as a source for reference frequency.

Board Default Frequency Output

Table 2. Board Default Frequency Output

Serial	Output	Output Frequency
1	SE_1 (Single-ended)	-
2	SE_2 (Single-ended)	48 MHz
3	SE_3 (Single-ended)	60 MHz
4	REF (Single-ended : Reference Output)	25 MHz
5	DIFF_T1/C1 (Differential Output)	100 MHz
6	DIFF_T2/C2 (Differential Output)	100 MHz

DIP Switch (SW1)

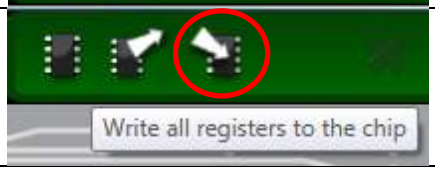
Table 3. DIP Switch (SW1)

Serial	DIP Switch PIN Number	DIP Switch PIN Name	State	Mode
A.	1	SDA_DFCO	Floating/Tristate	-
B.	2	SCL_DFC1	Floating/Tristate	Software I2C
C.	3, 5, 7	SMA_OE1, SMA_OE2, SMA_OE3	High or 1	-
D.	4, 6, 8	OE1, OE2, OE3	High or 1	-

Note. The DIP switch settings are set to default by the Manufacturer, which is same as the table above.

Configuration and Setup from I2C port

Table 4. Configuration and setup from I2C port

Step No.	Steps	Comments
1.	Set SCL_OFC1 Pin (DIP Switch PIN 2)	Set to mid-position on DIP switch
2.	Launch 5L35023 Timing Commander Software	Refer to 5L35023 Timing Commander User Guide
3.	Follow the “Getting Started Steps” – in Timing Commander Software	--
4.	Using the Timing Commander GUI, start a new setting file or open a pre-configured tcs file	Configure the Timing Commander Software for the required sets of outputs.
5.	Connect J3 using the supplied USB cable to a USB port from a PC	An I2C connection is established between GUI software and VC3S Chip
6.	Using GUI, connect to the EVB by clicking on the microchip icon located at the top right corner of the Timing Commander.	
7.	Once configured, new options will be available on a green background indicating that the EVB has successfully connected with	
8	By clicking on the “WRITE” icon, all the setting from the GUI are written to the registers of the VC3s chip	
9.	All intended outputs should be available for measurement.	-

Board Schematics

Evaluation board schematics are shown on the following pages.

Figure 3. Evaluation Board Schematic (I)

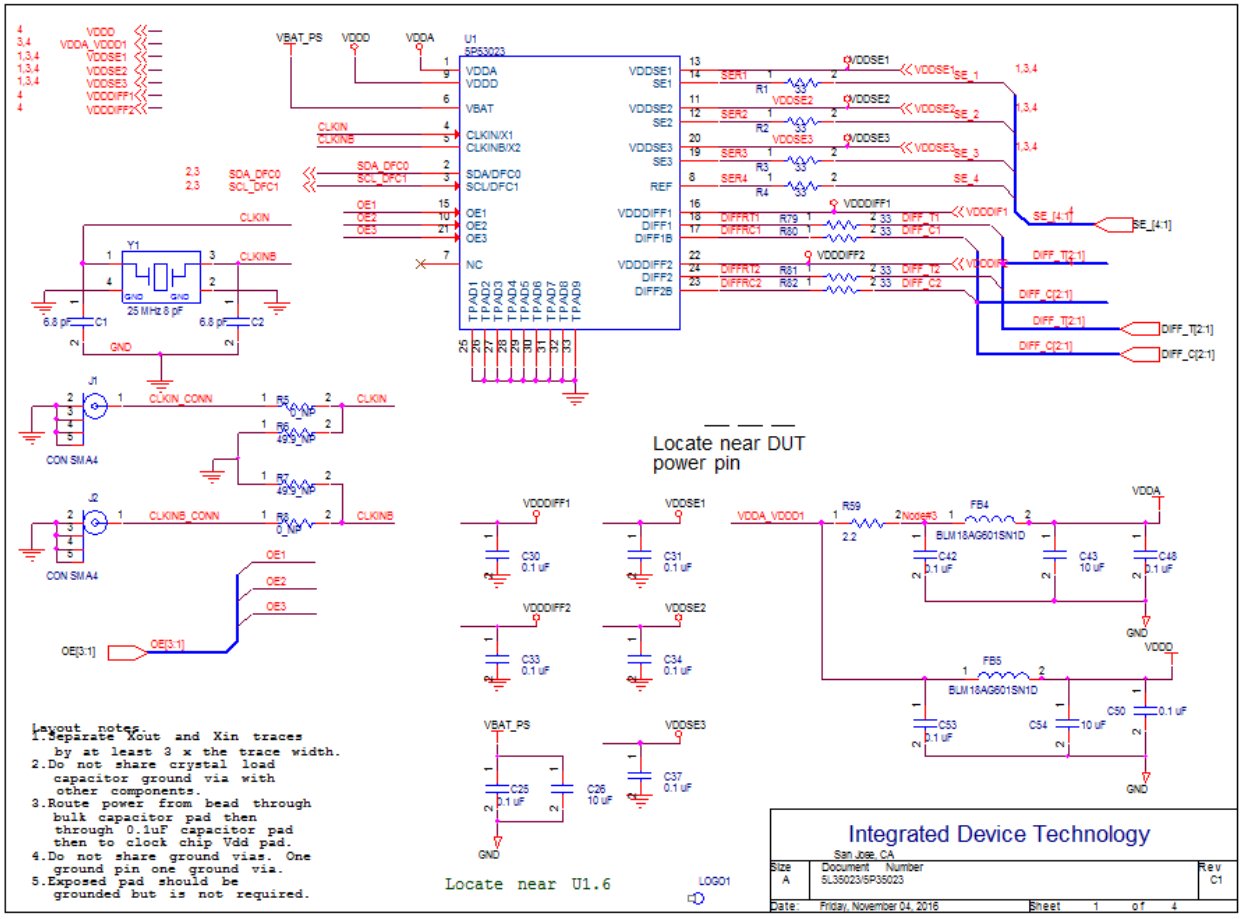
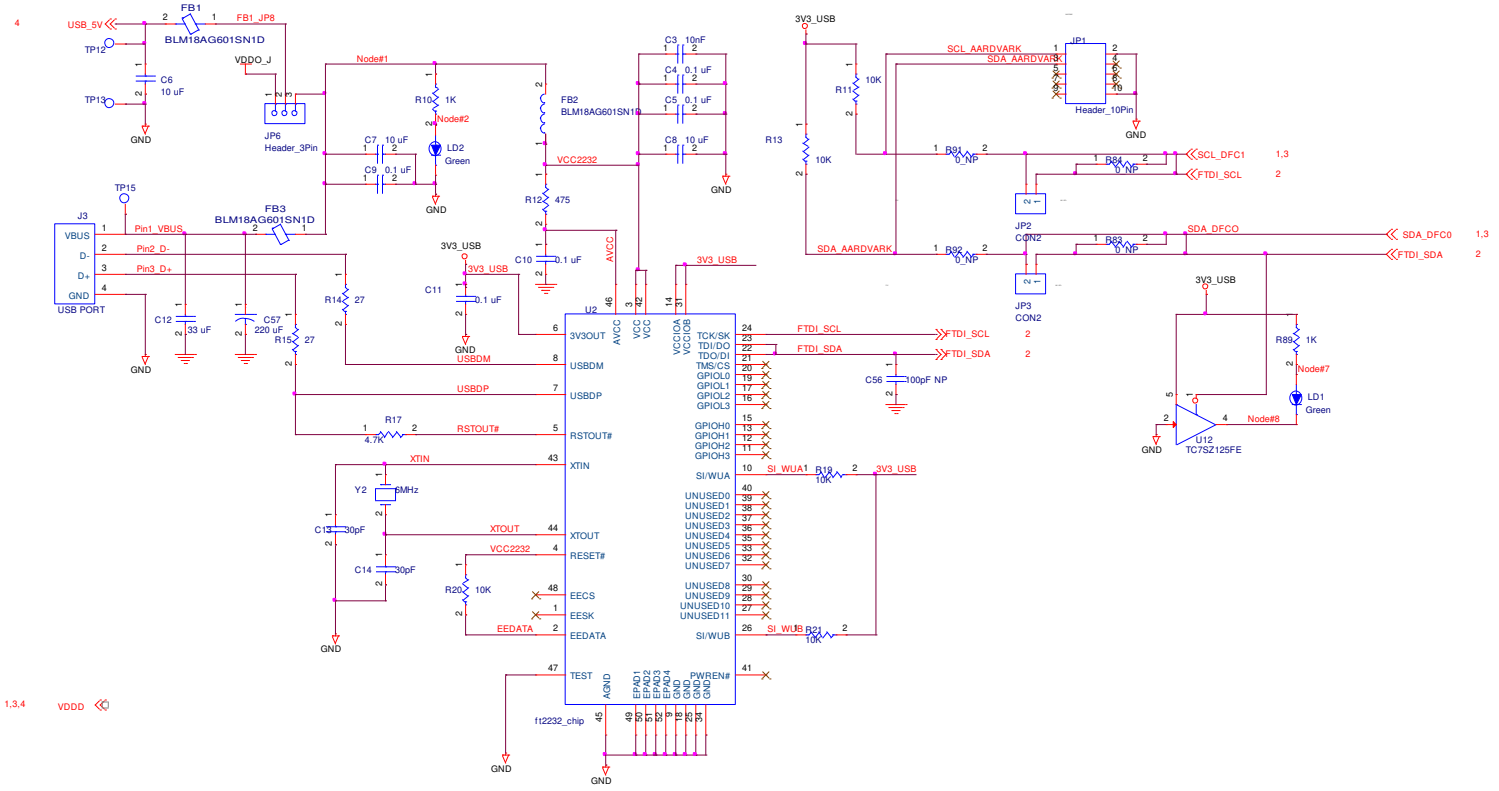


Figure 4. Evaluation Board Schematic (II)



	IDT_5L35023/5P35023 EVB_BOARD_REVC
B	C1
Friday , November 04, 2016	2 4

Figure 5. Evaluation Board Schematic (III)

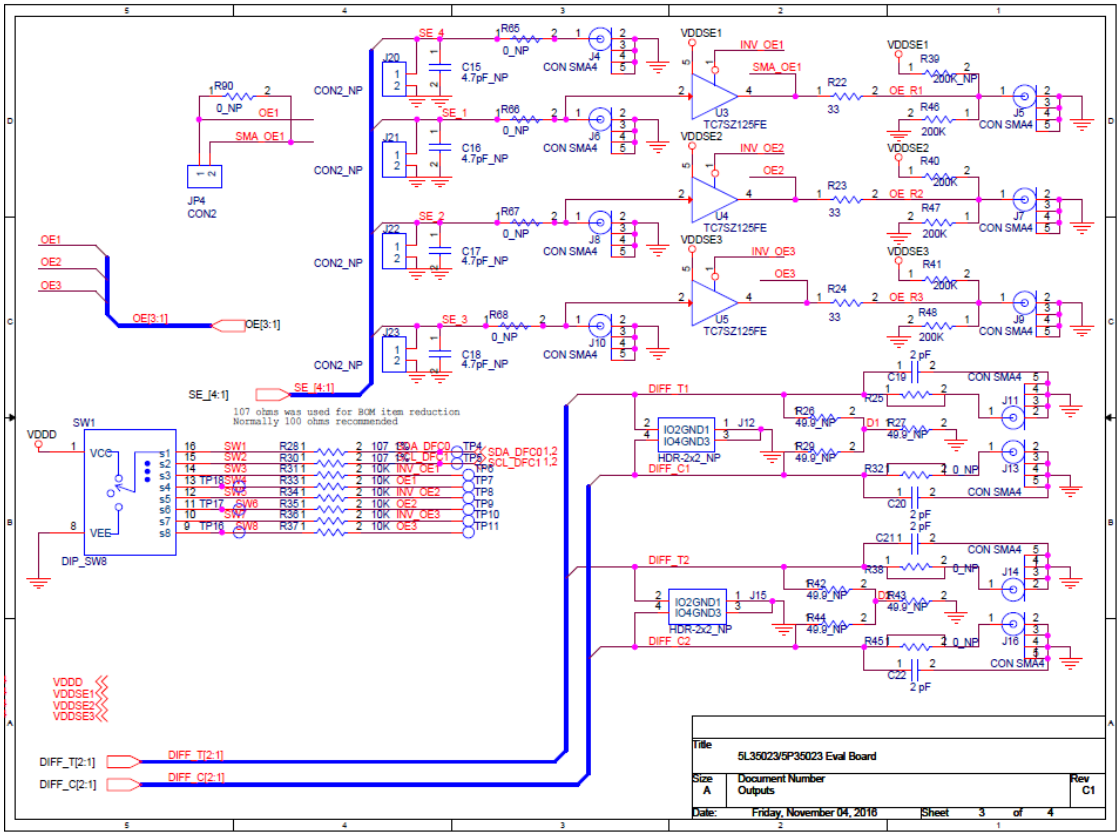
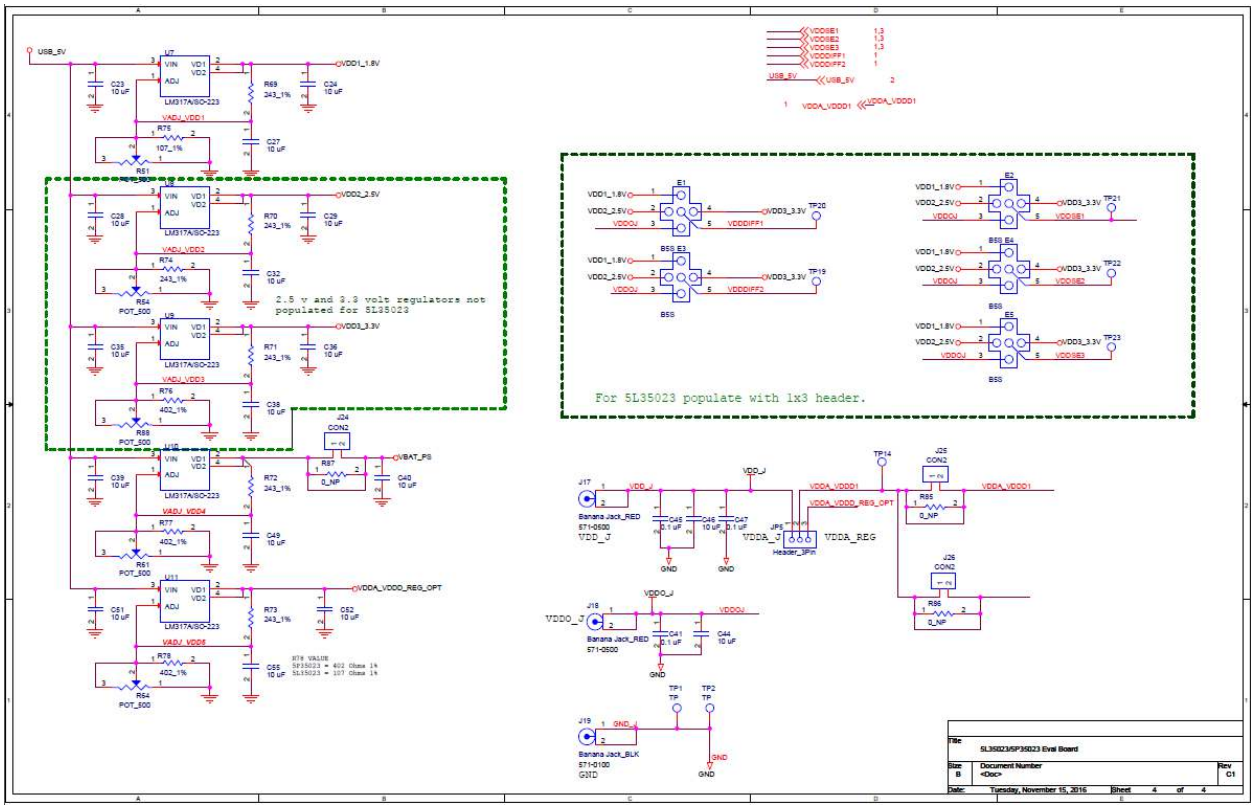


Figure 6. Evaluation Board Schematic (IV)



Signal Termination Options

Termination options for Differential Output 1 – 2 in the evaluation board are displayed in Figure 7. The termination circuits are designed to optionally terminate the output clocks in LVPECL, LVDS, LVCMOS and HCSL signal types by populating (or not-populating) some resistors. DC or AC coupling of these outputs are also supported.

Tables 5 and Table 6, below, tabulates component installations to support LVPECL, LPHCSL, LVCMOS and LVDS signal types for OUTPUT1– 2, respectively. Please note that by doing so, the output signals will be measured and terminated by an oscilloscope with a 50Ω internal termination.

Figure 7. Output Termination Options

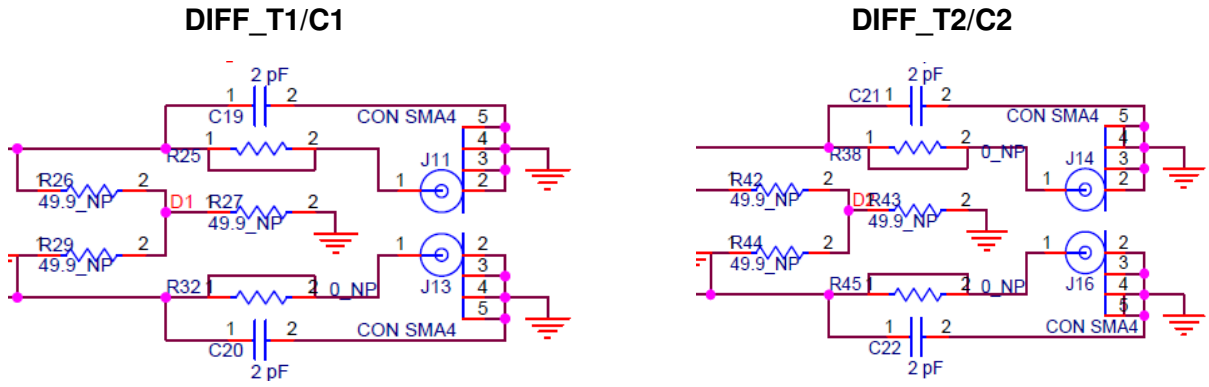


Table 5. Termination Options for Differential Output 1 (DIFF_T1/C1)

Signal Type	Series Resistors: R79, R80	Series Capacitors: C19, C20	Resistor Network: R26, R29	R27	R25, R32
**LPHCSL	33 Ω	2pF	Not Installed	Not Installed	Not Installed

Table 6. Termination Options for Differential Output 2 (DIFF_T2/C2)

Signal Type	Series Resistors: R81, R82	Series Capacitors: C21, C22	Resistor Network: R42, R44	R43	R38, R45
**LPHCSL	33 Ω	2pF	Not Installed	Not Installed	Not Installed

As noted, 4-resistor network is not installed in Table 5 and Table 6 because oscilloscope with internal 50Ω termination is utilized for signal termination and measurement. If an AC-coupled, stand-alone LVPECL output is needed (without oscilloscope connections), the 4-resistor network needs to be installed accordingly.

Table 7. Termination for Single-ended output 1 (SE_1)

Signal Type	Series Resistors: R1	Series Capacitors: C16
*LVCMOS	33 Ω	Not Installed

Table 8. Termination for Single-ended output 2 (SE_2)

Signal Type	Series Resistor: R2	Series Capacitor: C17
*LVCMOS	33 Ω	Not Installed

Table 9. Termination for Single-ended output 3 (SE_3)

Signal Type	Series Resistors: R3	Series Capacitors: C18
*LVCMOS	33 Ω	Not Installed

Table 10. Termination for Single-ended REF output (REF)

Signal Type	Series Resistor: R4	Series Capacitor: C15
*LVCMOS	33 Ω	Not Installed

Table 11. Termination for Differential and Single-ended Clock Input (CLKIN\CLKINB)

Signal Type	Series Resistor: R8	Series Resistor: R15
Differential Clock Input	Not Installed	Not Installed
Single-Ended Clock Input	Not Installed	Not Installed

Note: **The differential output is applicable to LPHCSL which is the default configuration of the board.
*The single-ended output is applicable to LVCMOS which is the default configuration of the board.
Contact IDT if user wants to change termination configuration to support other output signal types.

Orderable Part Numbers

The following evaluation board part numbers are available for order.

Table 12. Orderable Part Numbers

Part Number	Description
EVK5L35023	Evaluation board with all differential outputs terminated as LPHCSL, Single-ended terminated as LVCMOS

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