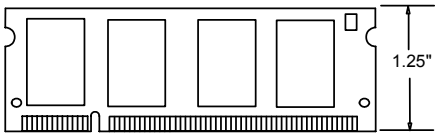
128MB - WD1SN128X808
256MB - WD1SN256X808
512MB - WD1SN512X808
1GB - WD1SN01GX808
2GB - WD1SN02GS808 (Stacked)

Features:

- 200-pin Unbuffered Non-ECC DDR SDRAM SODIMM for DDR-266, DDR-333, DDR-400
- JEDEC standard VDD=2.5V (+/- 0.2V) power supply
- One rank 128MB, 256MB, 512MB, 1GB, and 2GB
- Modules are built with x8 DDR SDRAM devices in **TSOPII-66 Pb-Free** package
- Programmable Read/Write Burst Length of 2, 4 and 8
- It uses 8K refresh cycles in 64ms
- SPD (Serial Presence Detect) with EEPROM
- All input/output are SSTL_2 compatible
- All contacts are gold plated
- **ROHS compliant**

Figure 1: Available profile

Standard:



Description:

The following specification covers the WD1SN128X808, WD1SN256X808, WD1SN512X808, WD1SN01GX808, WD1SN02GX808 family of One-Rank Unbuffered Non-ECC DDR Small-outline modules using x8 TSOPII SDRAMs. Please reference Figure 1 for available layout configurations and the product ordering guide on the final page of this specification for available options including speed grade and silicon manufacturer.

Speed Grades:

Speed Grade	Data Rate (MHz)			Clock/Data Rate	Latency	Module Speed
	CL2	CL2.5	CL3			
-266A	266	-	-	7ns/266MHz	2-3-3	DDR266A
-266B	-	266	-	7.5ns/266MHz	2.5-3-3	DDR266B
-333B	266	333	-	6.0ns/333MHz	2.5-3-3	DDR333
-400C	266	333	400	5.0ns/400MHz	3-3-3	DDR400

Address Summary Table:

	128MB	256MB	512MB	1GB	2GB
Module Configuration	16M x 64	32M x 64	64M x 64	128M x 64	256M x 64
Device Configuration	16M x 8 (8 components)	32M x 8 (8 components)	64M x 8 (8 components)	128M x 8 (8 components)	256M x 8 (8 stacked components)
Refresh	8K	8K	8K	8K	8K
Row Addressing	A0-A11	A0-A12	A0-A12	A0-A13	A0-A13
Column Addressing	A0-A9	A0-A9	A0-A9, A11	A0-A9, A11	A0-A9, A11, A12
Module Rank	1	1	1	1	1

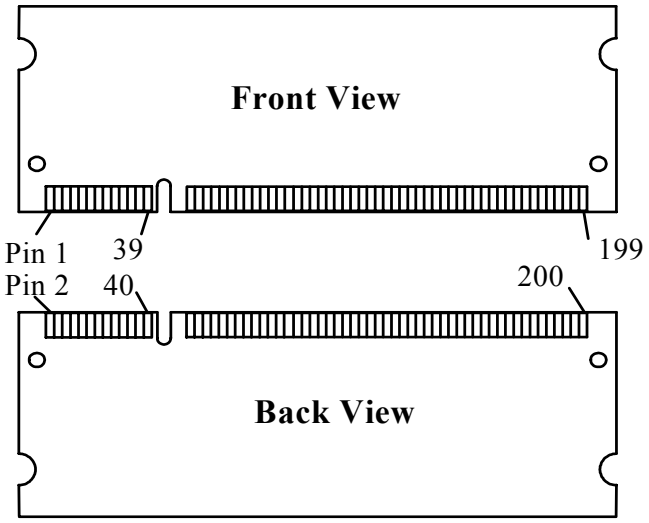
***Specifications are for reference purposes only and are subject to change by Wintec without notice.**

DIMM Pin Configuration:

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	51	VSS	101	A9	151	DQ42	2	VREF	52	VSS	102	A8	152	DQ46
3	VSS	53	DQ19	103	VSS	153	DQ43	4	VSS	54	DQ23	104	VSS	154	DQ47
5	DQ0	55	DQ24	105	A7	155	VDD	6	DQ4	56	DQ28	106	A6	156	VDD
7	DQ1	57	VDD	107	A5	157	VDD	8	DQ5	58	VDD	108	A4	158	CK1#
9	VDD	59	DQ25	109	A3	159	VSS	10	VDD	60	DQ29	110	A2	160	CK1
11	DQS0	61	DQS3	111	A1	161	VSS	12	DM0	62	DM3	112	A0	162	VSS
13	DQ2	63	VSS	113	VDD	163	DQ48	14	DQ6	64	VSS	114	VDD	164	DQ52
15	VSS	65	DQ26	115	A10	165	DQ49	16	VSS	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	VDD	18	DQ7	68	DQ31	118	RAS#	168	VDD
19	DQ8	69	VDD	119	WE#	169	DQS6	20	DQ12	70	VDD	120	CAS#	170	DM6
21	VDD	71	DNU	121	S0#	171	DQ50	22	VDD	72	DNU	122	DNU	172	DQ54
23	DQ9	73	DNU	123	NC	173	VSS	24	DQ13	74	DNU	124	NC	174	VSS
25	DQS1	75	VSS	125	VSS	175	DQ51	26	DM1	76	VSS	126	VSS	176	DQ55
27	VSS	77	DNU	127	DQ32	177	DQ56	28	VSS	78	DNU	128	DQ36	178	DQ60
29	DQ10	79	DNU	129	DQ33	179	VDD	30	DQ14	80	DNU	130	DQ37	180	VDD
31	DQ11	81	VDD	131	VDD	181	DQ57	32	DQ15	82	VDD	132	VDD	182	DQ61
33	VDD	83	DNU	133	DQS4	183	DQS7	34	VDD	84	DNU	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	VSS	36	VDD	86	NC	136	DQ38	186	VSS
37	CK0#	87	VSS	137	VSS	187	DQ58	38	VSS	88	VSS	138	VSS	188	DQ62
39	VSS	89	DNU	139	DQ35	189	DQ59	40	VSS	90	VSS	140	DQ39	190	DQ63
41	DQ16	91	DNU	141	DQ40	191	VDD	42	DQ20	92	VDD	142	DQ44	192	VDD
43	DQ17	93	VDD	143	VDD	193	SDA	44	DQ21	94	VDD	144	VDD	194	SA0
45	VDD	95	DNU	145	DQ41	195	SCL	46	VDD	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	VDDSPD	48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	NC/A12	149	VSS	199	NC	50	DQ22	100	A11	150	VSS	200	NC

NC - No Connect; DNU – Do Not Use
Note: Pin 99 is No Connect for 128MB, A12 for 256MB and 512MB

Pin Locations:



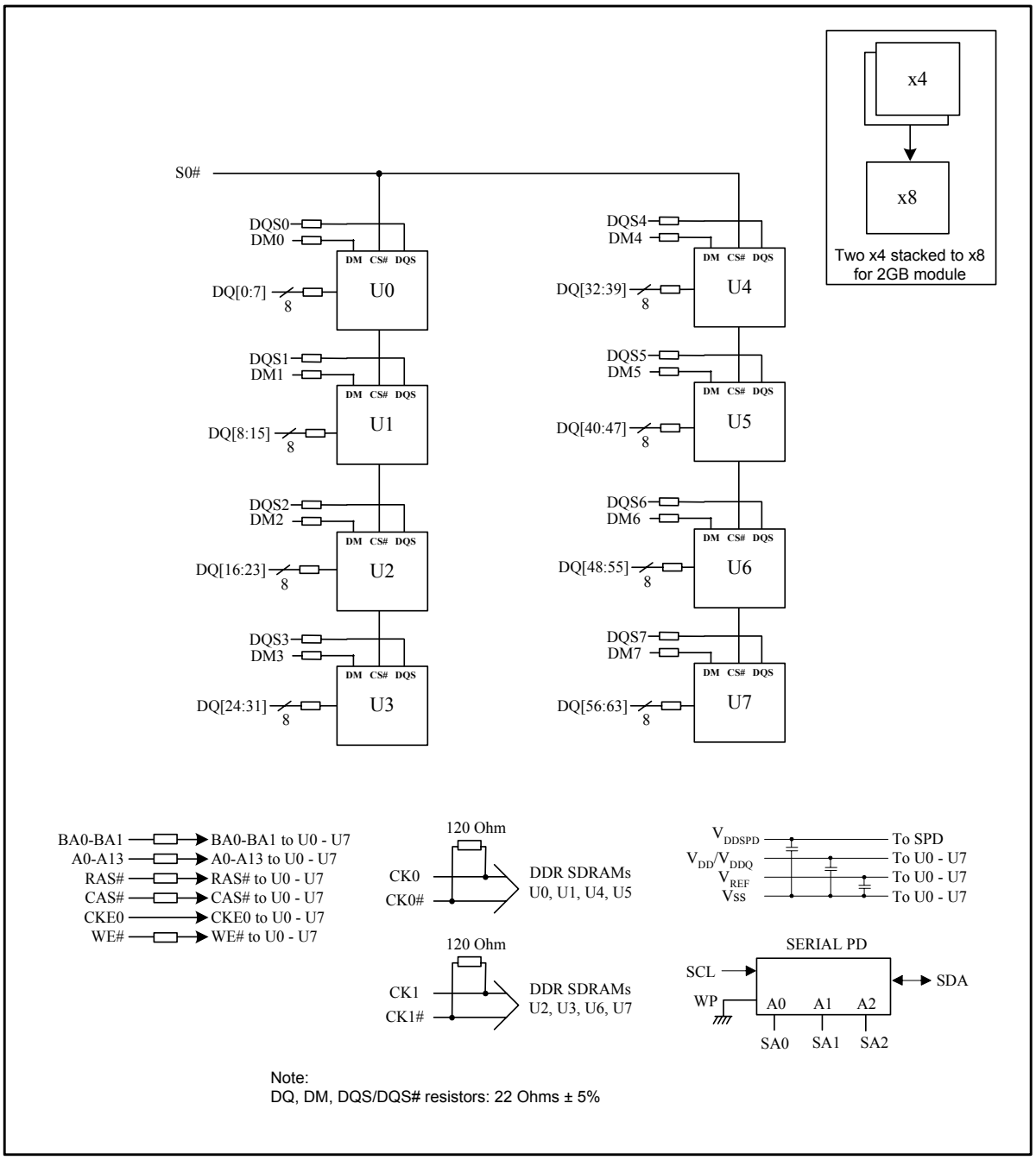
200-pin SODIMM

Pin Description:

Pin Name	Description	Pin Name	Description
A0-A13	Address input (Multiplexed)	CK0, CK0#, CK1, CK1#	Clock input
BA0, BA1	Bank select address	S0#	Chip Select
RAS#	Row address strobe	SCL	Serial clock
CAS#	Column address strobe	SDA	Serial Data I/O
WE#	Write enable	SA0-SA2	Address in EEPROM
CKE0	Clock Enable	VDD	Power supply
DQ0 – DQ63	Data input/output	VREF	Power supply for reference
DQS0 – DQS7	Data strobe input/output	VSS	Ground
DM0 – DM7	Data mask	VDDSPD	Serial EEPROM power supply
DNU	Do Not Use	NC	No connection

Functional Block Diagram:

One Rank 16M x 64 (128MB), 32M x 64 (256MB), 64M x 64 (512MB), 128M x 64 (1GB), and 256M x 64 (2GB) DDR Unbuffered Non-ECC SODIMM (x8 organization)



Absolute Maximum Ratings:

Exposure to stresses greater than these absolute maximum rating conditions for extended periods may affect reliability of the module.

Symbol	Parameter	Min	Max	Units
V_{DD}, $V_{DD}Q$	V_{DD} and $V_{DD}Q$ supply voltage relative to V_{SS}	-1.0	3.6	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.5	3.6	V
T_{STG}	Storage temperature (T_{case})	-55	+150	°C
T_{OPR}	Operating Temperature (ambient)	0	+70	°C
I_{OS}	Short circuit current	-	50	mA

DC Operating Conditions:

Parameter	Symbol	Min	Typical	Max	Units
Supply Voltage	V_{DD}	2.3	2.5	2.7	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	V_{REF} + 0.31	-	-	V
Input Low Voltage	V_{IL}	-	-	V_{REF} - 0.31	V

Electrical Characteristics and AC Timings:

V_{DD} = +2.5V ± 0.2V, $V_{DD}Q$ = +2.5V ± 0.2V, V_{SS} = 0V

Parameter	Symbol	-5 DDR-400		-6 DDR-333		-7 DDR-266		-7.5 DDR-266B		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
DQ output access time from $CK/\overline{CK}$	tAC	-0.5	+0.5	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	1,2,3,4
DQS output access time from $CK/\overline{CK}$	tDQSCK	-0.6	+0.6	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	ns	1,2,3,4
CK high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	1,2,3,4
CK low-level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	1,2,3,4
CK half period	tHP	min (tCL, tCH)	-	min (tCL, tCH)	-	min (tCL, tCH)	-	min (tCL, tCH)	-	ns	1,2,3,4
Clock cycle time	tCK3	5	8	6	12	7	12	7	12	ns	
	tCK2.5	6	12	6	12	7	12	7.5	12	ns	
	tCK2	7.5	12	7.5	12	7.5	12	7.5	12	ns	
Active to Precharge command	tRAS	40	70,000	42	70,000	45	120,000	45	120,000	ns	1,2,3,4
Active to Active command period	tRC	55	-	60	-	60	-	65	-	ns	1,2,3,4
Refresh to Refresh command interval	tRFC	70	-	72	-	75	-	75	-	ns	1,2,3,4
Active to Read/Write delay	tRCD	15	-	18	-	15	-	20	-	ns	1,2,3,4
Precharge command period	tRP	15	-	18	-	15	-	20	-	ns	1,2,3,4
DQ and DM input hold time	tDH	0.4	-	0.45	-	0.5	-	0.5	-	ns	1,2,3,4
DQ and DM input setup time	tDS	0.4	-	0.45	-	0.5	-	0.5	-	ns	1,2,3,4
Control & Address input pulse width for each input	tIPW	2.2	-	2.2	-	2.2	-	2.2	-	ns	1,2,3,4,6
DQ and DM input pulse width for each input	tDIPW	1.75	-	1.75	-	1.75	-	1.75	-	ns	1,2,3,4,6
Data-out high-impedance time from $CK/\overline{CK}$	tHZ	-0.7	+0.7	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	1,2,3,4,7
Data-out low-impedance time from $CK/\overline{CK}$	tLZ	-0.7	+0.7	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	1,2,3,4,7
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	+0.4	-	+0.45	-	+0.5	-	+0.8	ns	1,2,3,4
Write command to 1st DQS latching transition	tDQSS	0.72	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK	1,2,3,4
Data hold skew factor	tQHS	-	+0.5	-	+0.55	-	+0.75	-	+0.75	ns	1,2,3,4
Data output hold time from DQS	tQH	tHP-tQHS	-	tHP-tQHS	-	tHP-tQHS	-	tHP-tQHS	-	ns	1,2,3,4
DQS input low/high pulse width	tDQSL,H	0.35	-	0.35	-	0.35	-	0.35	-	tCK	1,2,3,4
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	0.2	-	0.2	-	tCK	1,2,3,4
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	0.2	-	0.2	-	tCK	1,2,3,4
Mode register set command cycle time	tMRD	2	-	2	-	2	-	2	-	tCK	1,2,3,4
Write postamble	tWPST	0.40	0.60	0.40	0.60	0.40	0.60	0.40	0.60	tCK	1,2,3,4,11
Write preamble	tWPRE	0.25	-	0.25	-	0.25	-	0.25	-	tCK	1,2,3,4
Write preamble setup time	tWPRES	0	-	0	-	0	-	0	-	tCK	1,2,3,4,10

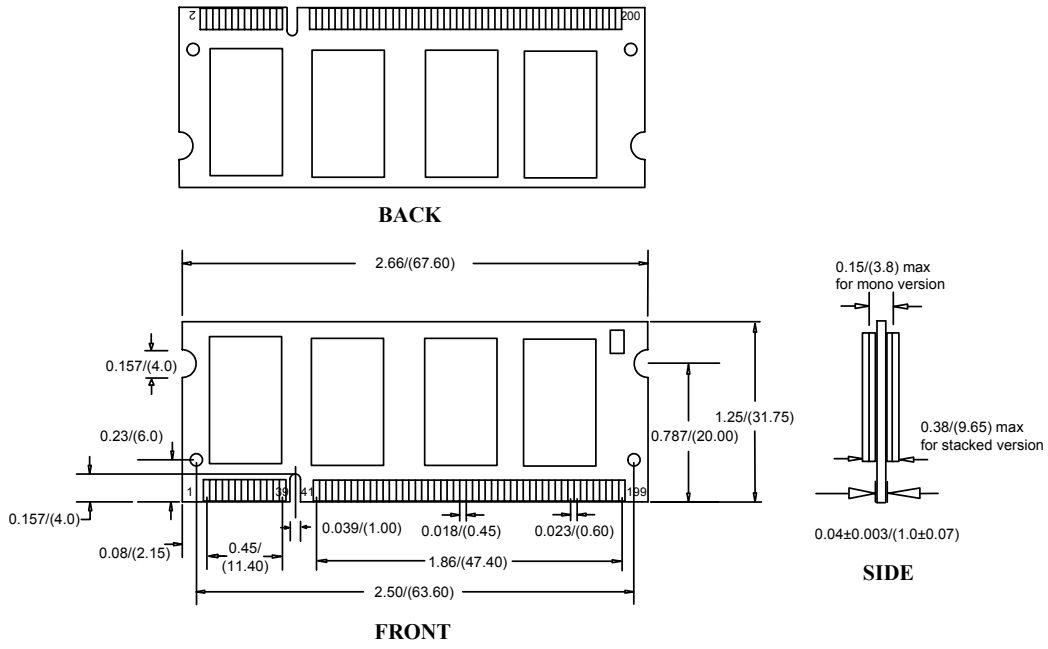
V_{DD} = +2.5V ± 0.2V, $V_{DD}Q$ = +2.5V ± 0.2V, V_{SS} = 0V

Parameter	Symbol	-5 DDR-400		-6 DDR-333		-7 DDR-266		-7.5 DDR-266B		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Address and control input hold time	tIH	0.6	-	0.75	-	0.9	-	0.9	-	ns	Fast slew rate 2,3,4,5,8
		0.7	-	0.8	-	1.0	-	1.0	-	ns	Slow slew rate 2,3,4,5,8
Address and control input setup time	tIS	0.6	-	0.75	-	0.9	-	0.9	-	ns	Fast slew rate 2,3,4,5,8
		0.7	-	0.8	-	1.0	-	1.0	-	ns	Slow slew rate 2,3,4,5,8
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	1,2,3,4
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	1,2,3,4
Active bank A to Active bank B command	tRRD	10	-	12	-	15	-	15	-	ns	1,2,3,4
Write recovery time	tWR	15	-	15	-	15	-	15	-	ns	1,2,3,4
Auto Precharge write recovery + Precharge time	tDAL	(tWR/tCK)+ (tRP/tCK)								tCK	1,2,3,4,5
Internal Write to Read command delay	tWTR	2	-	1	-	1	-	1	-	tCK	1,2,3,4
Exit Self-Refresh to non-Read command	tXSNR	75	-	75	-	75	-	75	-	ns	1,2,3,4
Exit Self-Refresh to Read command	tXSRD	200	-	200	-	200	-	200	-	tCK	1,2,3,4
Average periodic refresh interval	tREFI	-	7.8	-	7.8	-	7.8	-	7.8	µs	1,2,3,4,9

Note:

1. Input slew rate ≥ 1 V/ns for DDR400 and DDR333
2. The *CK*/$\overline{CK}$ input reference level (for timing reference to *CK*/$\overline{CK}$) is the point at which *CK* and $\overline{CK}$ cross: the input reference level for signals other than *CK*/$\overline{CK}$, is V_{REF}. *CK*/$\overline{CK}$ slew rate are ≥ 1 V/ns.
3. Inputs are not recognized as valid until V_{REF} stabilizes.
4. The output timing reference level, as measured at the timing reference point indicated in AC Characteristics is V_{TT}.
5. For each of the terms, if not already an interger, round to the next highest interger. tCK is equal to the actual system clock cycle time.
6. These parameters guarantee device timing, but they are not necessarily tested on each device.
7. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
8. Fast slew rate ≥ 1.0 V/ns, slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and *CK* and $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{IH(ac)}$ and $V_{IL(ac)}$.
9. A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.
10. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
11. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

Physical Dimensions – Standard:



Note:
1. Dimensions are in inches/(mm)
2. Tolerances:+/- 0.005"/(0.13mm) unless otherwise specified

Ordering Guide:

DDR-266, 333, 400MHz, One-Rank x8, Unbuffered SODIMM

WD1SN128X808
WD1SN256X808
WD1SN512X808
WD1SN01GX808
WD1SN02GS808

$x - yyyy(j) - Zz$

Naming Guide:

x: **Profile**	(Blank)	=	Std. (1.2")
yyyy: **Speed**	266A	=	DDR-266@CL2
	266B	=	DDR-266@CL2.5
	333B	=	DDR-333@CL2.5
	400C	=	DDR-400@CL3
(j): **Option**	(Blank)	=	Std.
Zz: **DRAM/Die**	Q	=	Infineon
	P	=	Samsung
	H	=	Micron

(Call for additional DRAM options and latest die-revision)

Configuration/Availability:

Density	PT #	Profile		Speed		DRAM/Die
128MB	WD1SN128X808	(Std)	-	266A, 266B, 333B, 400C	-	*Zz*
256MB	WD1SN256X808	(Std)		266A, 266B, 333B, 400C		
512MB	WD1SN512X808	(Std)		266A, 266B, 333B, 400C		
1GB	WD1SN01GX808	(Std)		266A, 266B, 333B, 400C		
2GB	WD1SN02GS808	(Std)		266A, 266B, 333B, 400C		

Example: WD1SN512X808-400C-QB
1GB DDR-400 Unbuffered Non-ECC SODIMM 1.25" using Infineon 64Mx8 B-Die

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http://www.wintecind.com/oem

Revision History:

Revision 1.0 (January 2006)
- Initial Release

Revision 1.1 (March 2006)
- Added stacked version