AN-1452 LM4985 Evaluation Board

1 Quick Start Guide

1. Connect the I^2C signal generation and interface board to a computer's parallel port.
2. Install LM4985 control software: "LM4985_Software_ver1-52."
3. Amplifier output mode:
   - For OCL (Output CapacitorLess) mode, place a jumper across the pins of JP10 and JP11 and across pins 1 and 2 on JP8.
   - For C-CUPL (Capacitor Coupled) mode, place a jumper across pins 2 and 3 on JP8. Leave JP10 and JP11 open.
4. Apply a 2.3V to 5.0V power supply's positive voltage output to the "+" pin on jumpers JP1 and JP2. Apply the power supply's ground return to the "-" on JP1 and JP2.
5. Connect the supplied 5-wire cable between the I^2C signal generation and interface board and the 5-pin connector (JP7 and JP9) on the LM4985 demonstration board.
6. Apply a stereo audio signal to jumpers JP3 and JP5. Apply the source's signal and ground to the "+" pin and the "-" pin, respectively.
7. Connect a load (≥ 16Ω) to JP4 and another load to JP6. JP4's "+" pin and JP6's "+" pin carries the output signals from the two amplifiers found on pins OUT1 and OUT2, respectively.
8. Apply power. Make measurements. Plug in a pair of headphones. Enjoy.

2 Introduction

To help the user investigate and evaluate the LM4985's performance and capabilities, a fully populated demonstration board is available. This board is shown in Figure 1. Connected to an external power supply (2.3V to 5V), a signal source and an I^2C controller (or signal source), the LM4985 demonstration board easily demonstrates the amplifier's features.

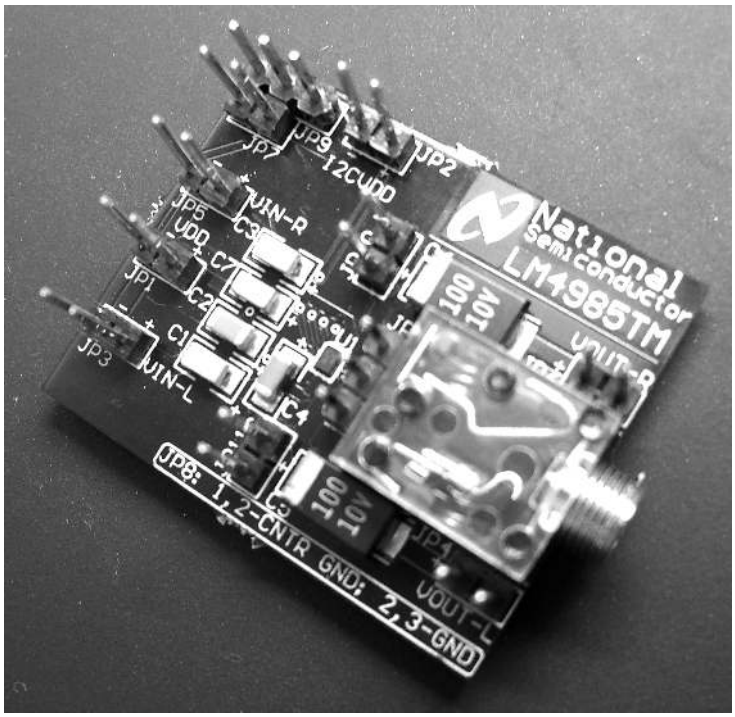

Figure 1. LM4985 Demonstration Board

3 General Description

The LM4985 is a stereo headphone audio amplifier with an internal digitally controlled volume control. The LM4985 is optimized to operate over a power supply voltage range of 2.5V to 5.0V. This amplifier is capable of delivering 40mW$_{RMS}$ per channel into a 32Ω load at 1% THD when powered by a 3.6V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. To that end, the LM4985 features two functions that optimize system cost and minimize PCB area: an integrated, digitally controlled (I^2C bus) volume control and, for maximum flexibility, an operational mode that eliminates output signal-coupling capacitors (OCL mode). Since the LM4985 does not require bootstrap capacitors, snubber networks, or output coupling capacitors, it is optimally suited for low-power, battery powered potable systems. For added design flexibility, the LM4985 can also be configured for single-ended capacitively coupled outputs.

The LM4985 includes an internal input MUX that allows the signal on either input to appear on either amplifier output and separate shutdown controls for each stereo channel.

The LM4985 features a shutdown mode for micropower dissipation, an internal thermal shutdown protection mechanism, and is unity gain stable.

4 Operating Conditions

- Temperature Range –40°C ≤ T_A ≤ 85°C
- Amplifier Power Supply Voltage 2.3V ≤ V_{DD} ≤ 5.0V

5 Schematic

Figure 2 shows the LM4985 Demonstration Board schematic. Refer to Table 1 for a list of the connections and their functions.

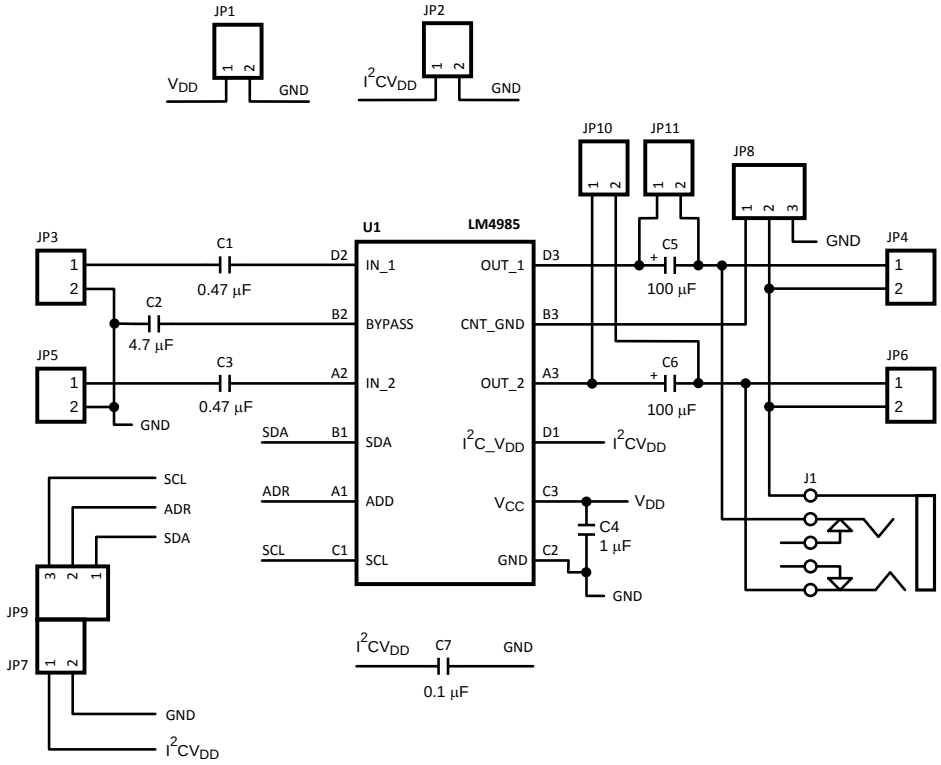

Figure 2. LM4985 Demonstration Board Schematic

6 Board Features

The LM4985 demonstration board has all of the necessary connections, using 100mil headers, to apply the power supply voltage, the audio input signals, and the I^2C signal inputs. The amplified audio signal is available on both a stereo headphone jack and auxiliary output connections. Jumpers are included to allow the use of either capacitively coupled or directly coupled amplifier outputs.

Also included with the demonstration board is an I^2C signal generation board and software. With this board and the software, the user can easily control the LM4985's input multiplexer, shutdown function, adjustable turn-on time, and stereo volume control. Figure 3 shows the software's graphical user interface.

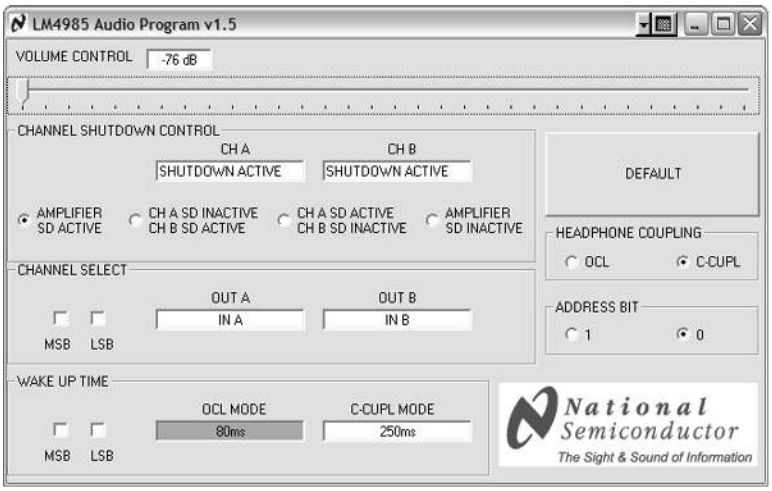

Figure 3. LM4985 Demonstration Board Graphical User Interface

7 Connections

Connecting to the world is accomplished through the 100mil headers on the LM4985 demonstration board. The functions of the different headers are detailed in Table 1.

Table 1. LM4985 Demonstration Board Connections

Jumper Designation	Function or Use
JP1	Power supply connection. Connect an external power supply's positive voltage source to the JP1 pin labeled "+" and the supply's ground source to the pin labeled "-."
JP2	If an external I^2C power supply voltage is used, connect this supply's positive voltage source to the JP2 pin labeled "+" and the supply's ground source to the pin labeled "-." If no external supply is used, leave this jumper's pins unconnected.
JP3	This is the connection to the amplifier's input A (labeled as the "left" input on the demonstration board). Apply an external signal source's positive voltage to the JP3 pin labeled "+" and the signal source's ground reference to the pin labeled "-."
JP4	This is the connection to the amplifier's output A (labeled as the "left" output on the demonstration board). Connect the JP4 pin labeled "+" to the positive input of an external signal measurement device. Connect the JP4 pin labeled "-" to the ground input of an external signal measurement device. JP4's pin labeled "+" corresponds to the headphone jack's "tip" connection. JP4's pin labeled "-" corresponds to the headphone jack's "sleeve" (or ground) connection.
JP5	This is the connection to the amplifier's input B (labeled as the "right" input on the demonstration board). Apply an external signal source's positive voltage to the JP5 pin labeled "+" and the signal source's ground reference to the pin labeled "-."
JP6	This is the connection to the amplifier's output B (labeled as the "right" output on the demonstration board). Connect the JP6 pin labeled "+" to the positive input of an external signal measurement device. Connect the JP6 pin labeled "-" to the ground input of an external signal measurement device. JP6's pin labeled "+" corresponds to the headphone jack's "sleeve" connection. JP6's pin labeled "-"corresponds to the headphone jack's "sleeve" (or ground) connection.
JP7 and JP9	Combined, these jumpers are used for the I^2C signal inputs. JP9-pin 1 is for the SDA signal, JP9-pin 2 is for the ADR signal, and JP9-pin 3 is for the SCL signal. JP7-pin 1 is for an I^2CV_{DD} supply voltage supplied by the I2C signal source and JP7-pin 2 is for ground.
JP8	This three-pin jumper is used when either OCL or C-CUPL modes are used. Short pins 1 and 2 together when the OCL mode is selected. Short pins 2 and 3 together when the C-CUPL mode is selected.
JP10	This jumper is used to short the right channel output capacitor C6 when the OCL mode is selected through the I^2C digital interface. When the LM4985 is used in the C–CUPL mode, leave this jumper open.
JP11	This jumper is used to short the left channel output capacitor C5 when the OCL mode is selected through the I^2C digital interface. When the LM4985 is used in the C–CUPL mode, leave this jumper open.

8 Power Supply Sequencing

The LM4985 uses two power supply voltages: V_{DD} for the analog circuitry and I^2CV_{DD} for the digital controls (volume, shutdown, and so on). To ensure proper functionality, apply V_{DD} first, followed by I^2CV_{DD}. If one power supply is used, V_{DD} and I^2CV_{DD} can be connected together. The part will power-up with shutdown active, the volume control set to minimum, and the input MUX set so that IN1 and IN2 correspond to OUT1 and OUT2, respectfully (normal stereo).

9 I²C Signal Generation Board and Software

The I^2C signal generation and interface board, along with the LM4985 software, will generate the address byte and the data byte used in the I^2C control data transaction. To use the I^2C signal generation and interface board, please plug it into a PC's parallel port (on either a notebook or a desktop computer).

The software comes with an installer. To install, unzip the file titled "LM4985_Software_ver1-52." After the file unzips, double-click the "setup.exe" file. After it launches, please follow the installer's instructions. Setup will create a folder named "LM4985" in the "Program" folder on the "C" disk (if the default is used) along with a shortcut of the same name in the "Programs" folder in the "Start" menu.

The LM4985 program includes controls for the amplifier's volume control, shutdown, input MUX, selectable wake-up time, amplifier output coupling and the I^2C address bit. The control program's on-screen user interface is shown in Figure 3.

The Default button is used to return the LM4985 to its power-on reset state (minimum volume setting, shutdown on both amplifiers active, standard stereo mode, capacitively coupled output, and minimum wake-up time.

The LM4985's stereo **VOLUME CONTROL** has 32 steps and a gain range of –76dB to 18dB. It is controlled using the slider located at the top of the program's window. Each time the slider is moved from one tick mark to another, the program updates the amplifier's volume control.

The **CHANNEL SHUTDOWN CONTROL** has four radio buttons. From left to right, the first button controls the shutdown function of both amplifiers. When selected, both amplifiers are placed in shutdown mode. The middle pair of buttons places a single amplifier channel in shutdown mode. The first of the pair deactivates channel A's shutdown and activates channel B's shutdown. The second in the pair activates channel A's shutdown and deactivates channel B's shutdown. The last shutdown button deactivates both channels' shutdown, allowing full, two-channel amplifier operation.

There is a protocol that one must follow when placing an individual amplifier channel in shutdown while the other channel remains active. The protocol requires activating both channel's shutdown simultaneously, then deactivating the shutdown of the channel whose output is desired (or leaving the desired channel in shutdown mode). This protocol is required whether using this software or a user-created routine. Further, when operating in the C-CUPL mode, a short delay time is required before activating one channel after placing both channels in shutdown. If the user finds that both channels activate when only one was chosen, increase the delay.

The next section, **CHANNEL SELECT**, is used to choose which input signal is internally routed to which amplifier channel. The power-on or reset state is standard stereo: the signal applied to input IN A is routed to the OUT A amplifier and the signal applied to input IN B is routed to the OUT B amplifier. The other three modes are the signal applied to IN A is routed to both channels, the signal applied to IN B is routed to both channels, and reverse stereo (the signal applied to IN A is routed to amplifier B and the signal applied to IN B is routed to amplifier A).

Use the **WAKE UP TIME** section to select one of four different wake-up times available in both OCL and C-CUPL modes. The time shown is typical. The actual observed wake-up time may be different.

Either of the two amplifier output-coupling modes is selected using the two radio buttons in the **HEADPHONE COUPLING** section. Select the output capacitorless (OCL) operational mode by clicking the "OCL" button. Select the capacitor-coupled (C-CUPL) operational mode by clicking the "C-CUPL" button. Ensure that shorting clips are installed correctly on jumpers JP8, JP10, and JP11. Refer to Table 2 and Table 3.

Table 2. OCL Operation

JP8	Short pins 1 and 2 together when the OCL mode is selected.
JP10	Short this jumper when the OCL is selected through the I^2C digital interface.
JP11	Short this jumper when the OCL is selected through the I^2C digital interface.

Table 3. C-CUPL Operation

JP8	Short pins 2 and 3 together when the C-CUPL mode is selected.
JP10	Open this jumper when the C-CUPL is selected through the I^2C digital interface.
JP11	Open this jumper when the C-CUPL is selected through the I^2C digital interface.

The last section of the software's interface (Figure 3) is the **ADDRESS BIT**. This bit can be set to 1 or 0. The software will force the I^2C interface board to apply a logic low or logic high to the LM4985's ADR pin according to the radio button that is selected. The LM4985 will respond to either of the addresses selected in the software's Address Bit control.

10 PCB Layout Guidelines

This section provides general practical guidelines for PCB layouts that use various power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results are predicated on the final layout.

10.1 Power and Ground Circuits

Star trace routing techniques (returning individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major positive impact on low-level signal performance. Star trace routing refers to using individual traces that radiate from a signal point to feed power and ground to each circuit or even device. This technique may require greater design time, but should not increase the final price of the board.

10.2 Avoiding Typical Design/Layout Problems

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other, do so at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and crosstalk.

11 Bill of Materials

Designator	Description	Package	Value (µF)	Notes
C1	Capacitor	C3216-1206 (Surface Mount)	0.47	10V, Tantalum
C2	Capacitor	C3216-1206 (Surface Mount)	4.7	50V, Ceramic
C3	Capacitor	C3216-1206 (Surface Mount)	0.47	10V, Tantalum
C4	Capacitor	C3216-1206 (Surface Mount)	1	50V, Ceramic
C5	Polarized Capacitor	TC7343-2917 (Surface Mount)	100	10V, Tantalum
C6	Polarized Capacitor	TC7343-2917 (Surface Mount)	100	10V, Tantalum
C7	Capacitor	C3216-1206 (Surface Mount)	0.1	50V, Ceramic
J1	3–Conductor Headphone Jack	Stereo Headphone Jack (3.5MM)		

12 Demonstration Board PCB Layout

Figure 4 through Figure 7 show the different layers used to create the LM4985 four-layer demonstration board. Figure 4 is the silkscreen that shows parts location, Figure 5 is the top layer, Figure 6 is the upper middle layer, and Figure 7 is the bottom layer. The lower middle layer was not routed in this PCB layout.

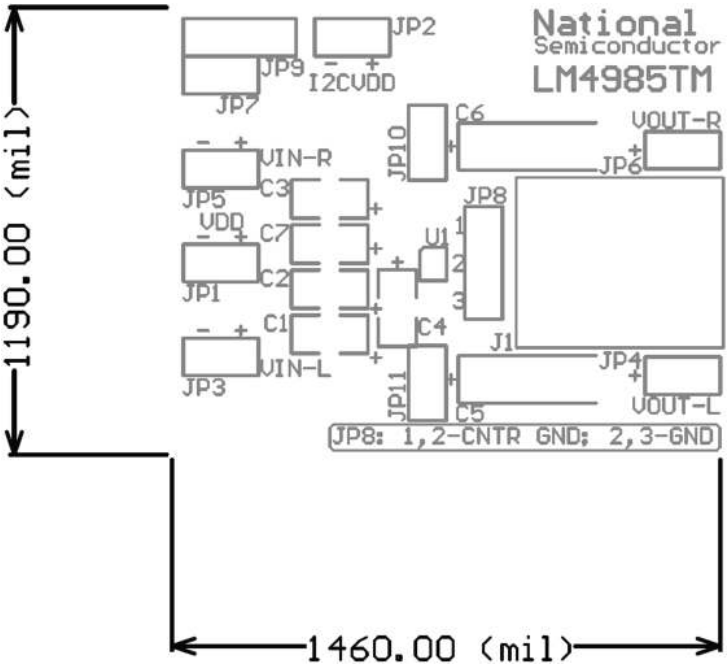

Figure 4. Top Silkscreen (Shown 2.6X actual size)

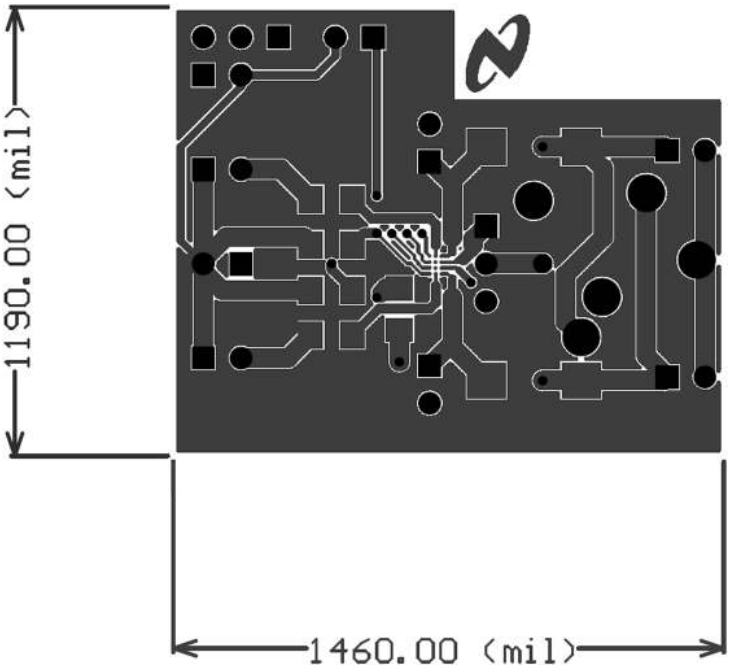

Figure 5. Top Layer (Shown 2.6X actual size)

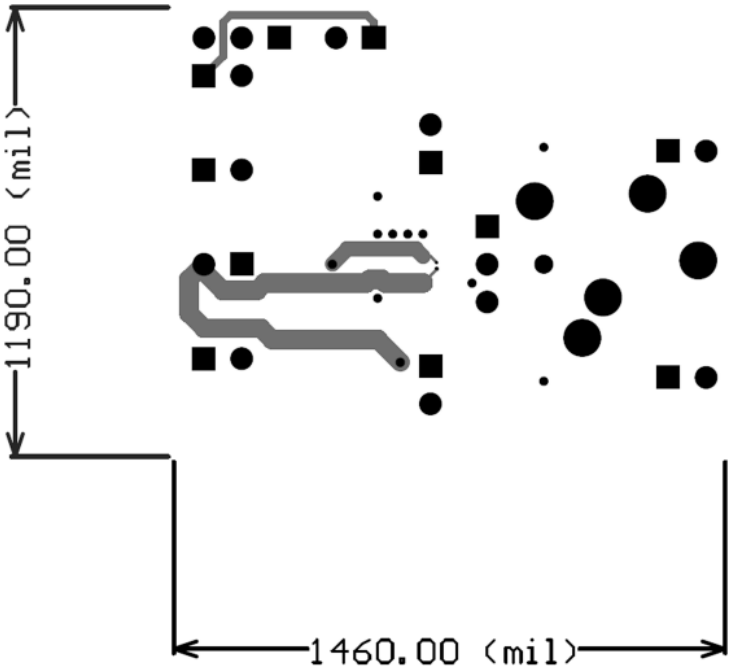

Figure 6. Upper Middle Layer (Shown 2.6X actual size)

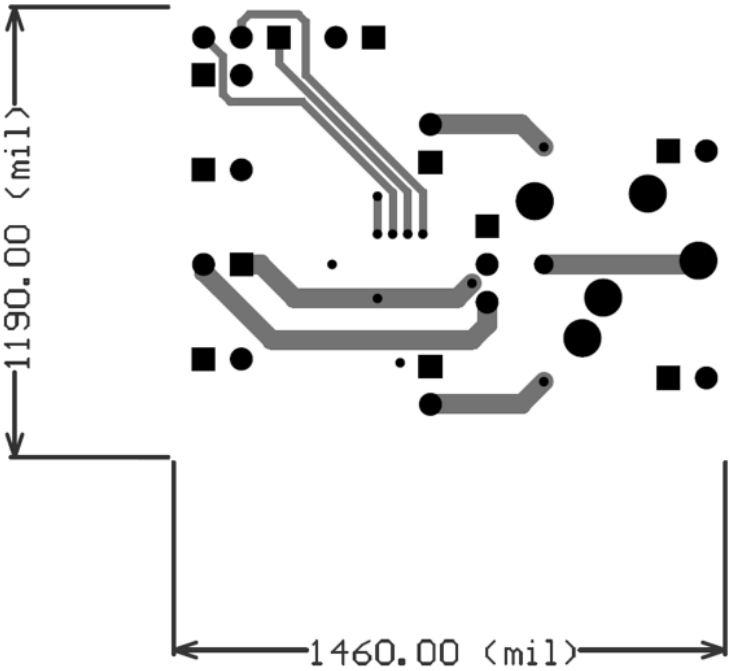

Figure 7. Bottom Layer (Shown 2.6X actual size)

13 Typical Demonstration Board Audio Performance (C-CUPL Mode)

Typical C-CUPL mode THD + N versus Output Power performance curves for 16Ω and 32Ω are shown in Figure 8 and Figure 9, respectively. Typical C-CUPL mode THD + N versus Frequency performance curves for 16Ω and 32Ω are shown in Figure 10 and Figure 11, respectively.

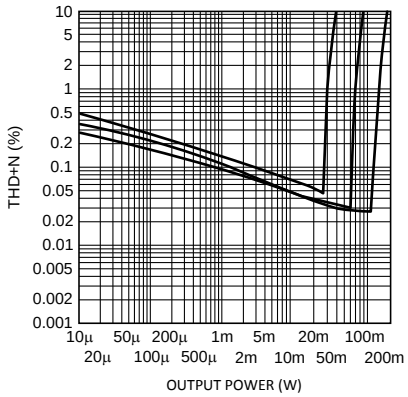

Figure 8. R_L = 16Ω, f_{IN} = 1kHz, at (from left to right at 1% THD+N): V_{DD} = 2.5V, V_{DD} = 3.6V, V_{DD} = 5.0V C-CUPL mode THD+N vs Output Power

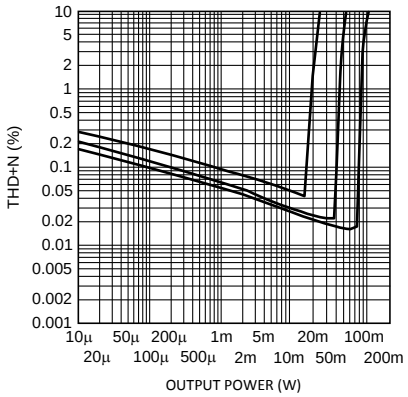

Figure 9. R_L = 32Ω, f_{IN} = 1kHz, at (from left to right at 1% THD+N): V_{DD} = 2.5V, V_{DD} = 3.6V, V_{DD} = 5.0V C-CUPL mode THD+N vs Output Power

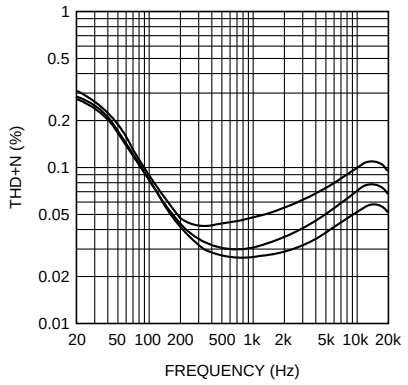

Figure 10. R_L = 16Ω, f_{IN} = 1kHz, at (from top to bottom at 1kHz): V_{DD} = 2.5V, P_{OUT} = 20mW, V_{DD} = 3.6V, P_{OUT} = 50mW, V_{DD} = 5.0V, P_{OUT} = 50mW C-CUPL mode THD+N vs Frequency

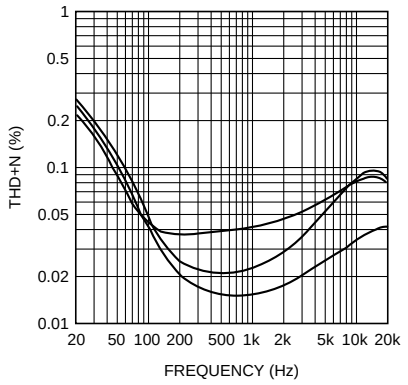

Figure 11. R_L = 32Ω, f_{IN} = 1kHz, at (from top to bottom at 1kHz): V_{DD} = 2.5V, P_{OUT} = 16mW, V_{DD} = 3.6V, P_{OUT} = 38mW, V_{DD} = 5.0V, P_{OUT} = 60mW C-CUPL mode THD+N vs Frequency

14 Typical Demonstration Board Audio Performance (OCL Mode)

Typical OCL mode THD + N versus Output Power performance curves for 16Ω and 32Ω are shown in Figure 12 and Figure 13, respectively. Typical OCL mode THD + N versus Frequency performance curves for 16Ω and 32Ω are shown in Figure 14 and Figure 15, respectively.

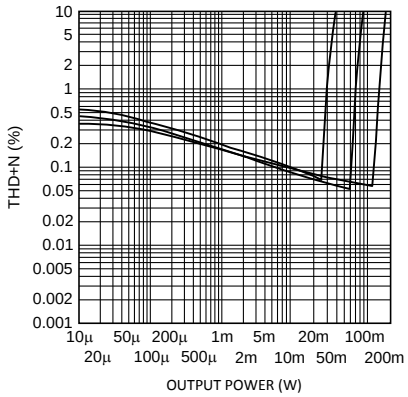

Figure 12. R_L = 16Ω, f_{IN} = 1kHz, at (from left to right at 1% THD+N): V_{DD} = 2.5V, V_{DD} = 3.6V, V_{DD}= 5.0V OCL mode THD+N vs Output Power

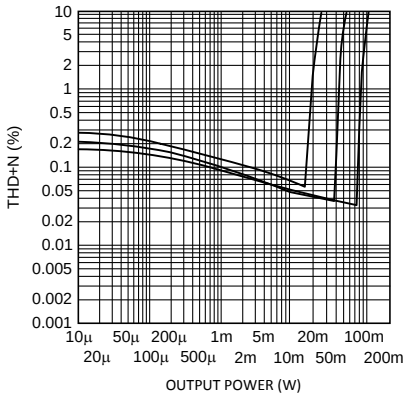

Figure 13. R_L = 32Ω, f_{IN} = 1kHz, at (from left to right at 1% THD+N): V_{DD} = 2.5V, V_{DD} = 3.6V, V_{DD}= 5.0V OCL mode THD+N vs Output Power

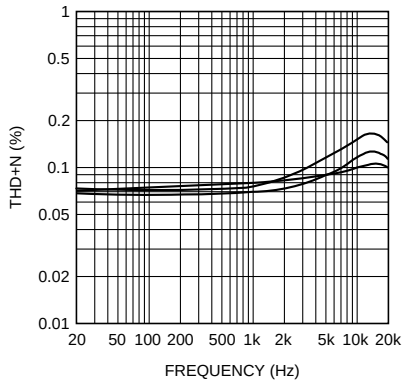

Figure 14. R_L = 16Ω, f_{IN} = 1kHz, at (from top to bottom at 2kHz): V_{DD} = 2.5V, P_{OUT} = 20mW, V_{DD} = 3.6V, P_{OUT} = 35mW, V_{DD}= 5.0V, P_{OUT} = 110mW OCL mode THD+N vs Frequency

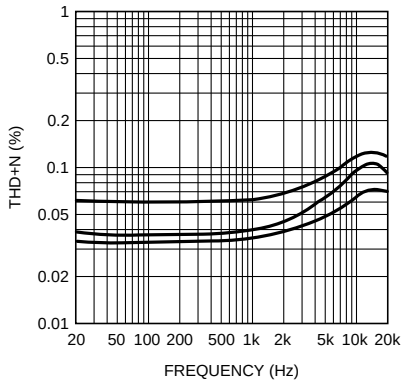

Figure 15. R_L = 32Ω, f_{IN} = 1kHz, at (from top to bottom at 2kHz): V_{DD} = 2.5V, P_{OUT} = 15mW, V_{DD} = 3.6V, P_{OUT} = 35mW, V_{DD}= 5.0V, P_{OUT} = 70mW OCL mode THD+N vs Frequency

Appendix A Minimizing Output Transient Magnitude

Although barely audible, very low magnitude output transients may occur when the LM4985's shutdown mode is deactivated. To ensure that they are silenced, the two slowest turn-on times are recommended when using the C-CUPL mode and the all but the fastest turn-on time when using the OCL mode.

Appendix B LM4985 I²C Control Register

Table 4 shows the actions that are implemented by manipulating the bits within the two internal I²C control registers.

Table 4. LM4985 I²C Control Register Addressing and Data Format Chart

	LM4985 I2C Contol Register Addressing and Data Chart								
I2C Address		A6	A5	A4	A3	A2	A1	A0	**Function**
		1	1	0	0	1	1	A0	
Register Select	D7	D6	D5	D4	D3	D2	RS1	RS0	
	0	0	0	0	0	0	0	0	Read and write the mode control register
	0	0	0	0	0	0	0	1	Read and write the volume control register
Mode Control Register	D7	D6	D5	D4	D3	D2	D1	D0	
		WT1	WT0	PHG	SDCH1	SDCH2	CHSEL1	CHSEL2	
	0	X	X	X	X	X	X	X	D7 must always be set to 0
	–	0	0	X	X	X	X	X	Wake-up time: 80ms (OCL), 250ms (C-CUPL)
	–	0	1	X	X	X	X	X	Wake-up time: 110ms (OCL), 450ms (C-CUPL)
	–	1	0	X	X	X	X	X	Wake-up time: 170ms (OCL), 850ms (C-CUPL)
	–	1	1	X	X	X	X	X	Wake-up time: 290ms (OCL), 1650ms (C-CUPL)
	–	X	X	1	X	X	X	X	Output capacitor-less mode **active**
	–	X	X	0	X	X	X	X	Output capacitor-less mode **inactive**
	–	X	X	X	0	0	X	X	Amplifier's SHUTDOWN mode **active**
	–	X	X	X	0	1	X	X	Illegal mode
	–	X	X	X	1	0	X	X	Illegal mode
	–	X	X	X	1	1	X	X	Amplifier's SHUTDOWN mode **inactive**
	–	X	X	X	X	X	0	02	Amplifier's Chan. 1 is **Input 1**, Chan 2. is **Input 2**
	–	X	X	X	X	X	0	1	Amplifier's Chan. 1 is **Input 1**, Chan 2. is **Input 1**
	–	X	X	X	X	X	1	0	Amplifier's Chan. 1 is **Input 2**, Chan 2. is **Input 2**
	–	X	X	X	X	X	1	1	Amplifier's Chan. 1 is **Input 2**, Chan 2. is **Input 1**

Appendix C Volume Control Settings Binary Values

The minimum volume setting is set to –76dB when 00000 is loaded into the volume control register. Incrementing the volume control register in binary fashion increases the volume control setting, reaching full scale at 11111. Table 5 shows the value of the gain for each of the 32 binary volume control settings.

Table 5. Binary Values for the Different Volume Control Gain Settings

Gain	B4	B3	B2	B1	B0
18	1	1	1	1	1
17	1	1	1	1	0
16	1	1	1	0	1
15	1	1	1	0	0
14	1	1	0	1	1
13	1	1	0	1	0
12	1	1	0	0	1
10	1	1	0	0	0
8	1	0	1	1	1
6	1	0	1	1	0
4	1	0	1	0	1
2	1	0	1	0	0
0	1	0	0	1	1
–2	1	0	0	1	0
–4	1	0	0	0	1
–6	1	0	0	0	0
–8	0	1	1	1	1
–10	0	1	1	1	0
–12	0	1	1	0	1
–14	0	1	1	0	0
–16	0	1	0	1	1
–18	0	1	0	1	0
–21	0	1	0	0	1
–24	0	1	0	0	0
–27	0	0	1	1	1
–30	0	0	1	1	0
–34	0	0	1	0	1
–38	0	0	1	0	0
–44	0	0	0	1	1
–52	0	0	0	1	0
–62	0	0	0	0	1
–76	0	0	0	0	0

Appendix D Micro SMD Wafer Level Chip Scale Package, PCB, Layout, and Mounting Considerations

Please refer to *AN-1112 DSBGA Wafer Level Chip Scale Package* (SNVA009) for possible updates to the µSMD package information.

Appendix E Maximizing OCL Mode Channel-to-Channel Separation

The OCL mode AC ground return (CNT_GND pin) is shared by both amplifiers. As such, any resistance between the CNT_GND pin and the load will create a voltage divider with respect to the load resistance. In a typical circuit, the amount of CNT_GND resistance can be very small, but still significant. It is significant because of the relatively low load impedances for which the LM4985 was designed to drive: 16Ω to 32Ω. The ratio of this voltage divider will determine the magnitude of any residual signal present at the CNT_GND pin. It is this residual signal that leads to channel-to-channel separation (crosstalk) degradation.

For example, for a 60dB channel-to-channel separation while driving a 16Ω load, the resistance between the LM4985's CNT_GND pin and the load must be less than 16mΩ. This is achieved by ensuring that the trace that connects the CNT_GND pin to the headphone jack sleeve should be as short and massive as possible, given the physical constraints of any specific printed circuit board layout and design.

Appendix F Revision History

Rev	Date	Description
1.0	04/21/06	Initial release.
1.1	05/18/06	Added Appendix E.
1.2	05/26/06	Re-released to the WEB.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265