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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

May 2015

FDS86267P

P-Channel Shielded Gate PowerTrench® MOSFET

-150 V, -2.2 A, 255 mΩ

Features

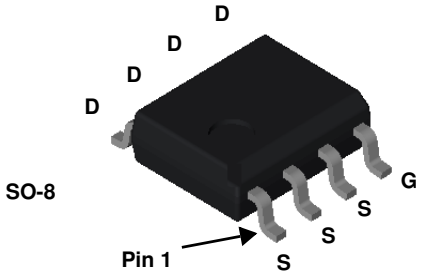
- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 255 mΩ at V_{GS} = -10 V, I_D = -2.2 A
- Max $r_{DS(on)}$ = 290 mΩ at V_{GS} = -6 V, I_D = -2 A
- Very Low $r_{DS(on)}$ Mid Voltage P-channel Silicon Technology Optimised for Low Qg
- This Product is Optimised for Fast Switching Applications as well as Load Switch Applications
- 100% UIL Tested
- RoHS Compliant

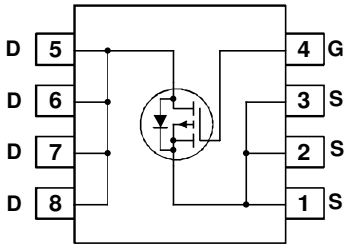
General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates shielded gate technology. The process has been optimized for the on-state resistance and yet maintain superior switching performance.

Applications

- Active Clamp Switch
- Load Switch





MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted.

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			-150	V
V_{GS}	Gate to Source Voltage			±25	V
I_D	Drain Current -Continuous		(Note 1a)	-2.2	A
	-Pulsed		(Note 4)	-34	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	54	mJ
P_D	Power Dissipation	T_A = 25 °C	(Note 1a)	2.5	W
	Power Dissipation	T_A = 25 °C	(Note 1b)	1.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	125	

Package Marking and Ordering Information

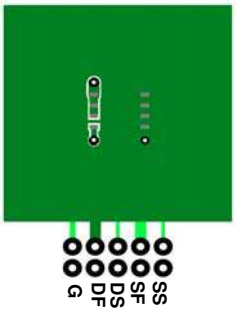
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS86267P	FDS86267P	SO-8	13 ”	12 mm	2500 units

Electrical Characteristics T_J = 25 °C unless otherwise noted.

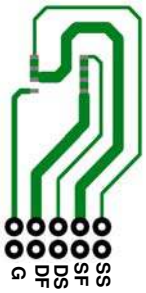
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0 V	-150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		-121		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -120 V, V_{GS} = 0 V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±25 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 μA	-2	-3	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -10 V, I_D = -2.2 A		191	255	mΩ
		V_{GS} = -6 V, I_D = -2 A		214	290	
		V_{GS} = -10 V, I_D = -2.2 A, T_J = 125 °C		342	448	
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -2.2 A		6.8		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -75 V, V_{GS} = 0 V, f = 1 MHz		806	1130	pF
C_{oss}	Output Capacitance			54	75	pF
C_{rss}	Reverse Transfer Capacitance			1.6	2.3	pF
R_g	Gate Resistance		0.1	3	6	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -75 V, I_D = -2.2 A, V_{GS} = -10 V, R_{GEN} = 6 Ω		9.7	20	ns
t_r	Rise Time			2.5	10	ns
$t_{d(off)}$	Turn-Off Delay Time			17	30	ns
t_f	Fall Time			5.7	12	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to -10 V; V_{DD} = -75 V, I_D = -2.2 A		11	16	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to -6 V; V_{DD} = -75 V, I_D = -2.2 A		7	10	nC
Q_{gs}	Gate to Source Charge	V_{DD} = -75 V, I_D = -2.2 A		3.2		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = -75 V, I_D = -2.2 A		1.9		nC
Drain-Source Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.2 A (Note 2)		-0.8	-1.3	V
		V_{GS} = 0 V, I_S = -2 A (Note 2)		-0.8	-1.2	
t_{rr}	Reverse Recovery Time	I_F = -2.2 A, di/dt = 100 A/μs		65	104	ns
Q_{rr}	Reverse Recovery Charge			157	251	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 125 °C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25 °C, L = 3 mH, I_{AS} = -6 A, V_{DD} = -150 V, V_{GS} = -10 V. 100% tested at L = 0.3 mH, I_{AS} = -13 A.
4. Pulsed Id please refer to Fig 11 SOA graph for more details.

Typical Characteristics T_J = 25 °C unless otherwise noted

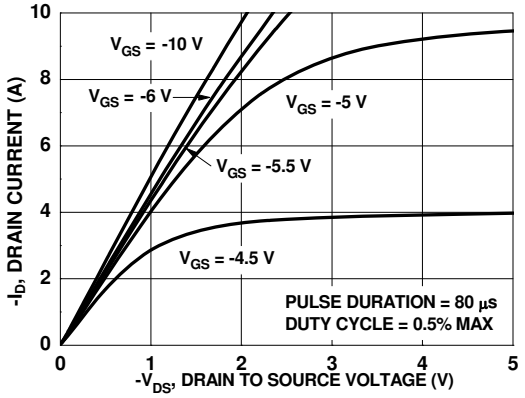


Figure 1. On Region Characteristics

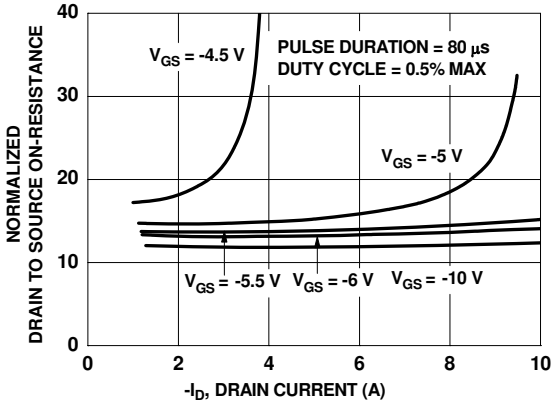


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

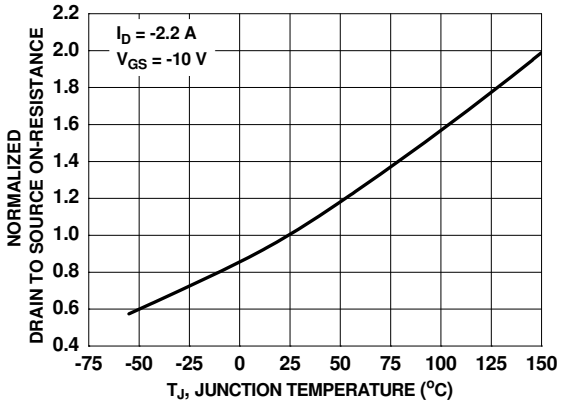


Figure 3. Normalized On Resistance vs Junction Temperature

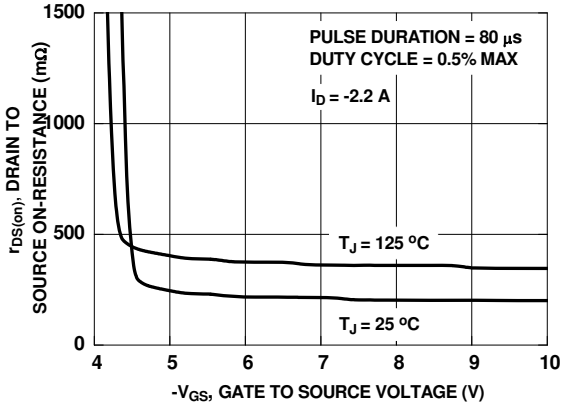


Figure 4. On-Resistance vs Gate to Source Voltage

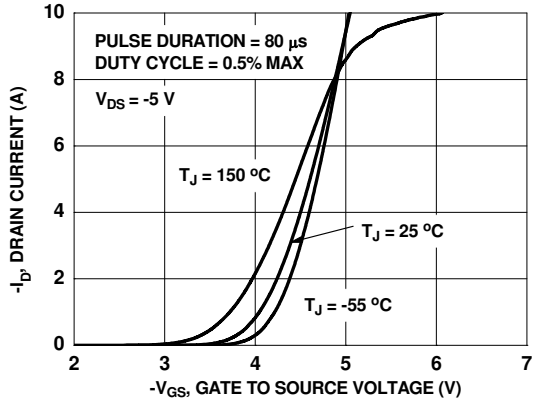


Figure 5. Transfer Characteristics

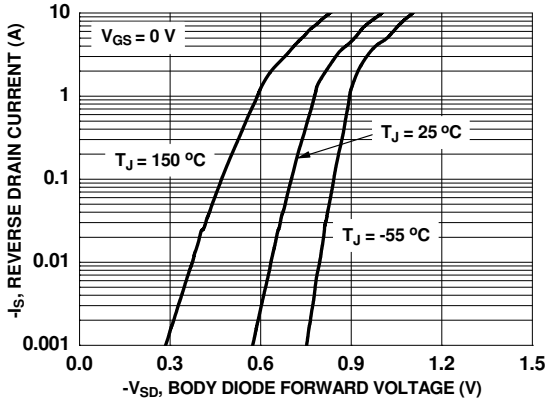


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

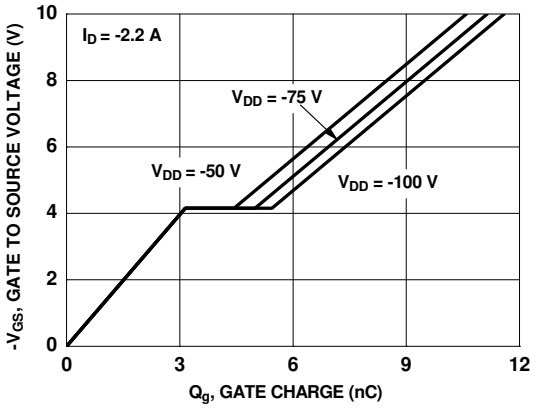


Figure 7. Gate Charge Characteristics

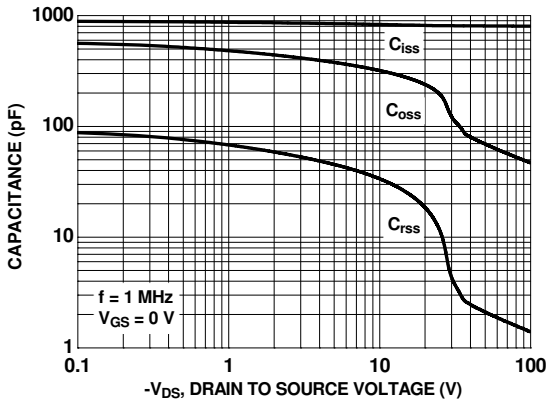


Figure 8. Capacitance vs Drain to Source Voltage

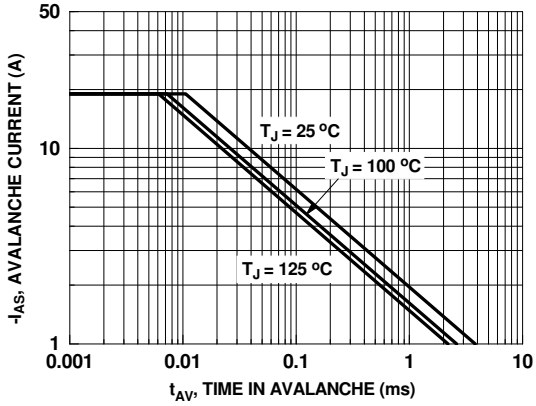


Figure 9. Unclamped Inductive Switching Capability

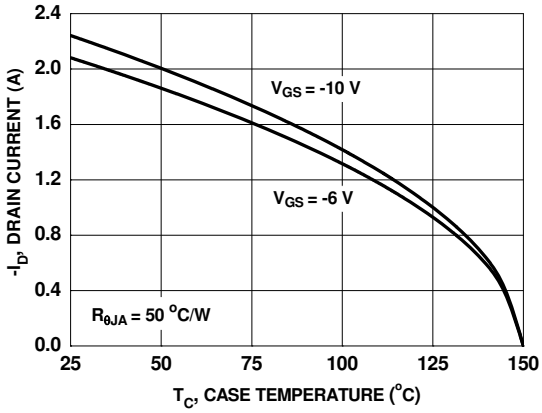


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

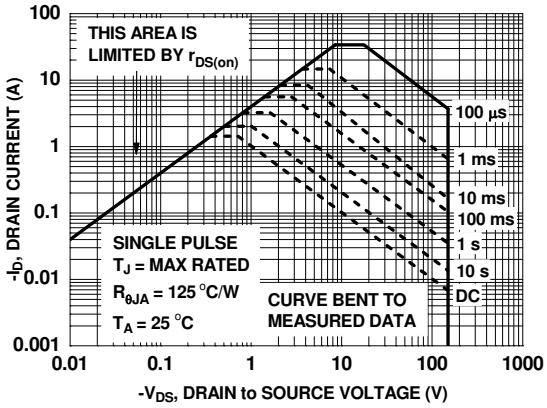


Figure 11. Forward Bias Safe Operating Area

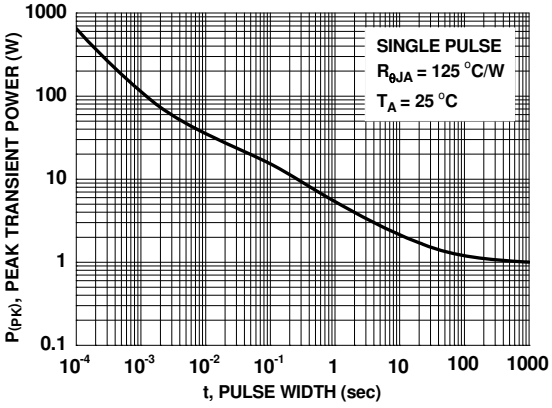
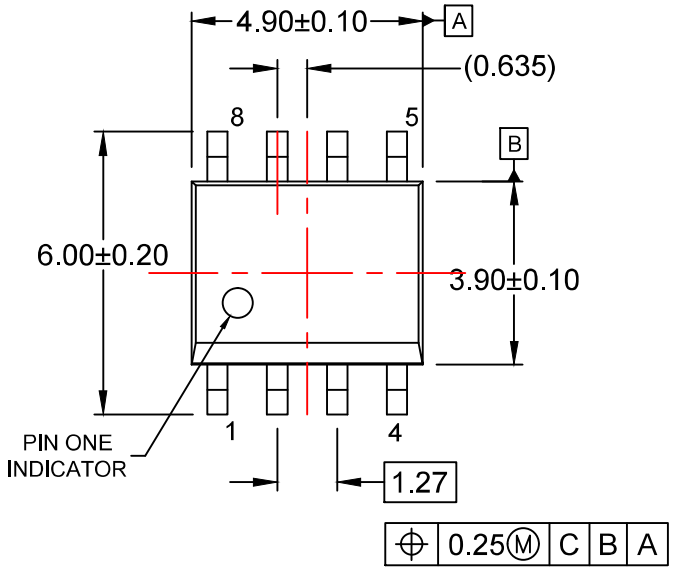
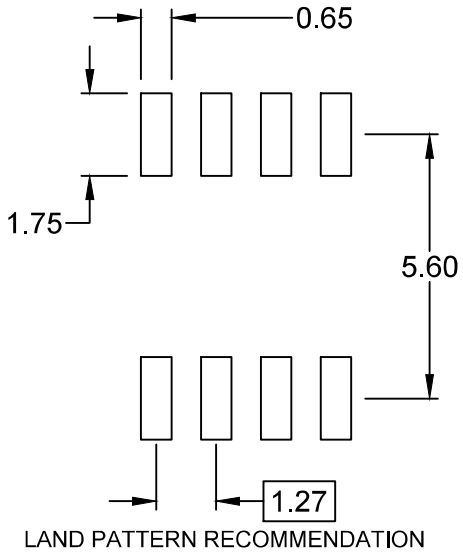
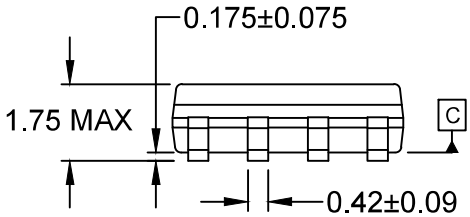


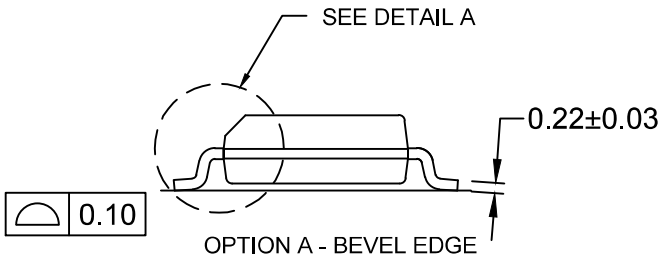
Figure 12. Single Pulse Maximum Power Dissipation



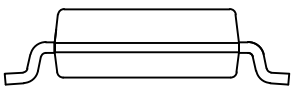


LAND PATTERN RECOMMENDATION

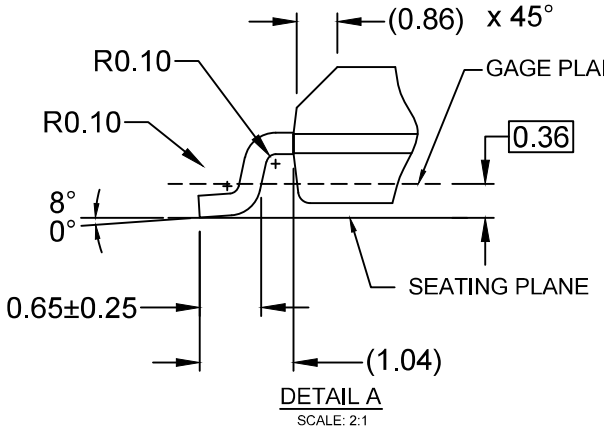




OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE



DETAIL A
SCALE: 2:1

NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M
E) DRAWING FILENAME: M08Arev16

FAIRCHILD.

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