16-Bit, 500 kSPS PulSAR ADC in MSOP

Data Sheet **AD7686**

FEATURES

- 16-bit resolution with no missing codes
- Throughput: 500 kSPS
- INL: ±0.6 LSB typical, ±2 LSB maximum (±0.003% of FSR)
- SINAD: 92.5 dB at 20 kHz
- THD: −110 dB at 20 kHz
- Pseudo differential analog input range
  - 0 V to V_{REF} with V_{REF} up to VDD
- No pipeline delay
- Single-supply 5 V operation with
  - 1.8 V/2.5 V/3 V/5 V logic interface
- Proprietary serial interface: SPI-/QSPI™-/MICROWIRE™-/DSP-compatible
- Daisy-chain multiple ADCs and busy indicator
- Power dissipation
  - 3.75 µW at 5 V/100 SPS
  - 3.75 mW at 5 V/100 kSPS
- Standby current: 1 nA
- 10-lead MSOP (MSOP-8 size) and
  - 3 mm × 3 mm, 10-lead LFCSP (SOT-23 size)
- Pin-for-pin-compatible with 10-lead MSOP/PulSAR® ADCs

APPLICATIONS

- Battery-powered equipment
- Data acquisitions
- Instrumentation
- Medical instruments
- Process controls

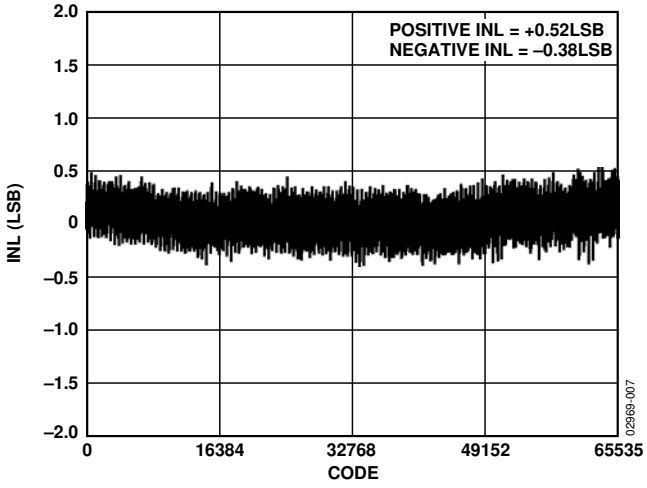

Figure 1. Integral Nonlinearity vs. Code

[1] Protected by U.S. Patent 6,703,961.

FUNCTIONAL BLOCK DIAGRAM

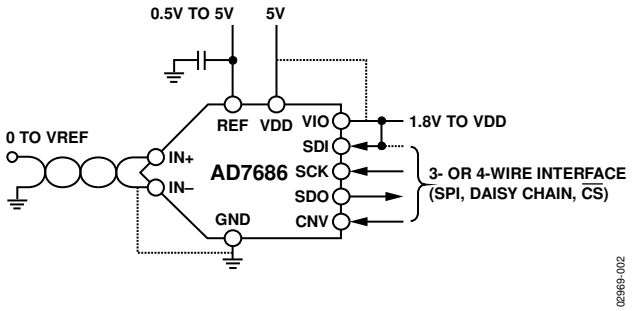

Figure 2.

Table 1. MSOP, LFCSP/SOT-23 14-/16-/18-Bit PulSAR ADC

Type	100 kSPS	250 kSPS	400 kSPS to 500 kSPS	1000 kSPS	ADC Driver
18-Bit True		AD7691	AD7690	AD7982	ADA4941
Differential			AD7982		ADA4941
16-Bit True	AD7684	AD7687	AD7688		ADA4941
Differential			AD7693		ADA4841
16-Bit Pseudo	AD7680	AD7685	AD7686	AD7980	ADA4941
Differential	AD7683	AD7694			
14-Bit Pseudo Differential	AD7940	AD7942	AD7946		ADA4941

GENERAL DESCRIPTION

The AD7686[1] is a 16-bit, charge redistribution, successive approximation, analog-to-digital converter (ADC) that operates from a single 5 V power supply, VDD. It contains a low power, high speed, 16-bit sampling ADC with no missing codes, an internal conversion clock, and a versatile serial interface port. The part also contains a low noise, wide bandwidth, short aperture delay track-and-hold circuit. On the CNV rising edge, the AD7686 samples an analog input IN+ between 0 V to REF with respect to a ground sense IN−. The reference voltage, REF, is applied externally and can be set up to the supply voltage.

Power dissipation scales linearly with throughput.

The SPI-compatible serial interface also features the ability, using the SDI input, to daisy-chain several ADCs on a single, 3-wire bus or provides an optional busy indicator. This device is compatible with 1.8 V, 2.5 V, 3 V, or 5 V logic, using the separate supply VIO.

The AD7686 is housed in a 10-lead MSOP or a 10-lead LFCSP with operation specified from −40°C to +85°C.

Rev. C Document Feedback

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4/06—Rev. 0 to Rev. A

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4/05—Revision 0: Initial Version

SPECIFICATIONS

VDD = 4.5 V to 5.5 V, VIO = 2.3 V to VDD, V_{REF} = VDD, T_A = −40°C to +85°C, unless otherwise noted.

Table 2.

		B Grade			C Grade			
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		16			16			Bits
ANALOG INPUT								
Voltage Range	IN+ − IN−	0		V_{REF}	0		V_{REF}	V
Absolute Input Voltage	IN+	−0.1		VDD + 0.1	−0.1		VDD + 0.1	V
	IN−	−0.1		+0.1	−0.1		+0.1	V
Analog Input CMRR	f_{IN} = 200 kHz		65			65		dB
Leakage Current at 25°	Acquisition phase		1			1		nA
C Input Impedance		See the Analog Input section			See the Analog Input section			
ACCURACY								
No Missing Codes		16			16			Bits
Differential Linearity Error		−1	±0.7		−1	±0.5	+1.5	LSB[1]
Integral Linearity Error		−3	±1	+3	−2	±0.6	+2	LSB[1]
Transition Noise	REF = VDD = 5 V		0.5			0.45		LSB[1]
Gain Error[2], T_{MIN} to T_{MAX}			±2	±8		±2	±6	LSB[1]
Gain Error Temperature Drift			±0.3			±0.3		ppm/°C
Offset Error[2], T_{MIN} to T_{MAX}			±0.1	±1.6		±0.1	±1.6	mV
Offset Temperature Drift			±0.3			±0.3		ppm/°C
Power Supply Sensitivity	VDD = 5 V ± 5%		±0.05			±0.05		LSB[1]
THROUGHPUT								
Conversion Rate		0		500	0		500	kSPS
Transient Response	Full-scale step			400			400	ns
AC ACCURACY								
Signal-to-Noise Ratio	f_{IN} = 20 kHz, V_{REF} = 5 V	89	92		91	92.7		dB[3]
	f_{IN} = 20 kHz, V_{REF} = 2.5 V		87.5			88		dB[2]
Spurious-Free Dynamic Range	f_{IN} = 20 kHz		−106			−110		dB[2]
Total Harmonic Distortion	f_{IN} = 20 kHz		−106			−110		dB[2]
Signal-to-(Noise + Distortion)	f_{IN} = 20 kHz, V_{REF} = 5 V	89	92		91	92.5		dB[2]
	f_{IN} = 20 kHz, V_{REF} = 5 V, −60 dB input		32			33.5		dB[2]
Intermodulation Distortion[4]			−110			−115		dB[2]

[1] LSB means least significant bit. With the 5 V input range, 1 LSB is 76.3 µV.
[2] See the Terminology section. These specifications do include full temperature range variation, but do not include the error contribution from the external reference.
[3] All specifications in dB are referred to a full-scale input FSR. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[4] f_{IN1} = 21.4 kHz, f_{IN2} = 18.9 kHz, each tone at −7 dB below full scale.

VDD = 4.5 V to 5.5 V, VIO = 2.3 V to VDD, V_{REF} = VDD, T_A = −40°C to +85°C, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE					
Voltage Range		0.5		VDD + 0.3	V
Load Current	500 kSPS, REF = 5 V		100		µA
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			9		MHz
Aperture Delay	VDD = 5 V		2.5		ns
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.3 × VIO	V
V_{IH}		0.7 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format		Serial 16 bits straight binary			
Pipeline Delay		Conversion results available immediately after completed conversion			
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD	Specified performance	4.5		5.5	V
VIO	Specified performance	2.3		VDD + 0.3	V
VIO Range		1.8		VDD + 0.3	V
Standby Current[1, 2]	VDD and VIO = 5 V, 25°C		1	50	nA
Power Dissipation	VDD = 5 V, 100 SPS throughput		3.75		µW
	VDD = 5 V, 100 kSPS throughput		3.75	4.3	mW
	VDD = 5 V, 500 kSPS throughput		15	21.5	mW
TEMPERATURE RANGE[3]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] With all digital inputs forced to VIO or GND as required.
[2] During acquisition phase.
[3] Contact sales for extended temperature range.

TIMING SPECIFICATIONS

−40°C to +85°C, VDD = 4.5 V to 5.5 V, VIO = 2.3 V to 5.5 V or VDD + 0.3 V, whichever is the lowest, unless otherwise stated. See Figure 3 and Figure 4 for load conditions.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	0.5		1.6	µs
Acquisition Time	t_{ACQ}	400			ns
Time Between Conversions	t_{CYC}	2			µs
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	10			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}	15			ns
SCK Period (Chain Mode)	t_{SCK}				
VIO Above 4.5 V		17			ns
VIO Above 3 V		18			ns
VIO Above 2.7 V		19			ns
VIO Above 2.3 V		20			ns
SCK Low Time	t_{SCKL}	7			ns
SCK High Time	t_{SCKH}	7			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 4.5 V				14	ns
VIO Above 3 V				15	ns
VIO Above 2.7 V				16	ns
VIO Above 2.3 V				17	ns
CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}				
VIO Above 4.5 V				15	ns
VIO Above 2.7 V				18	ns
VIO Above 2.3 V				22	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			25	ns
SDI Valid Setup Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{SSDICNV}$	15			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	5			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	3			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	4			ns
SDI High to SDO High (Chain Mode with Busy Indicator)	$t_{DSDOSDI}$				
VIO Above 4.5 V				15	ns
VIO Above 2.3 V				26	ns

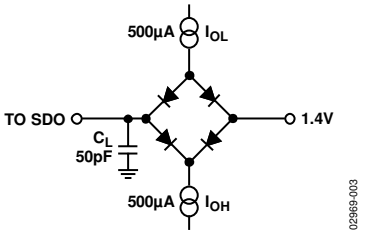


Figure 3. Load Circuit for Digital Interface Timing

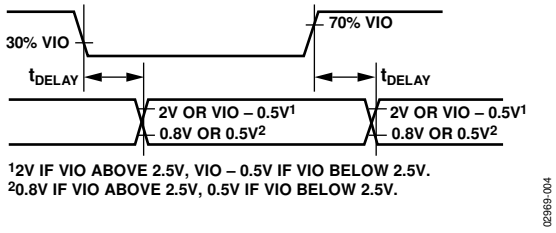


Figure 4. Voltage Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Inputs	
IN+[1], IN−[1]	GND − 0.3 V to VDD + 0.3 V or ±130 mA
REF	GND − 0.3 V to VDD + 0.3 V
Supply Voltages	
VDD, VIO to GND	−0.3 V to +7 V
VDD to VIO	±7 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	200°C/W (MSOP-10)
θ_{JC} Thermal Impedance	44°C/W (MSOP-10)
Lead Temperature	JEDEC J-STD-20

[1] See the Analog Input section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

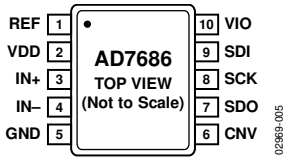


Figure 5. 10-Lead MSOP Pin Configuration

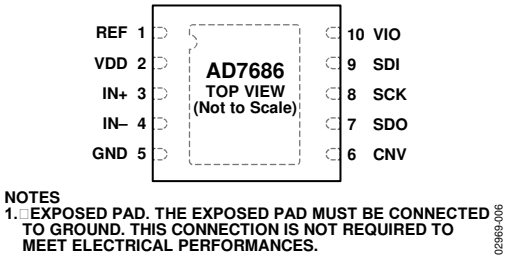


Figure 6. 10-Lead LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	REF	AI	Reference Input Voltage. The REF range is from 0.5 V to VDD. It is referred to the GND pin. This pin should be decoupled closely to the pin with a 10 µF capacitor.
2	VDD	P	Power Supply.
3	IN+	AI	Analog Input. It is referred to IN–. The voltage range, that is, the difference between IN+ and IN–, is 0 V to V_{REF}.
4	IN–	AI	Analog Input Ground Sense. It is connected to the analog ground plane or to a remote sense ground.
5	GND	P	Power Supply Ground.
6	CNV	DI	Convert Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode, chain, or $\overline{CS}$. In $\overline{CS}$ mode, it enables the SDO pin when low. In chain mode, the data should be read when CNV is high.
7	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
8	SCK	DI	Serial Data Clock Input. When the part is selected, the conversion result is shifted out by this clock.
9	SDI	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows: Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low. If SDI or CNV is low when the conversion is completed, the busy indicator feature is enabled.
10	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).
	EPAD	N/A	Exposed Pad. The exposed pad must be connected to ground. This connection is not required to meet electrical performances.

[1]AI = analog input, DI = digital input, DO = digital output, and P = power.

TERMINOLOGY

Integral Nonlinearity Error (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 25).

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error
The first transition should occur at a level ½ LSB above analog ground (38.1 μV for the 0 V to 5 V range). The offset error is the deviation of the actual transition from that point.

Gain Error
The last transition (from 111 . . . 10 to 111 . . . 11) should occur for an analog voltage 1½ LSB below the nominal full scale (4.999886 V for the 0 V to 5 V range). The gain error is the deviation of the actual level of the last transition from the ideal level after the offset is adjusted out.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

and is expressed in bits.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in dB.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in dB.

Signal-to-(Noise + Distortion), SINAD
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in dB.

Aperture Delay
It is the measure of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response
Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

TYPICAL PERFORMANCE CHARACTERISTICS

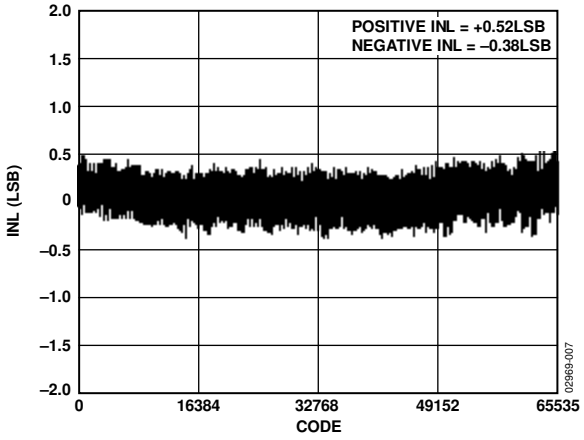


Figure 7. Integral Nonlinearity vs. Code

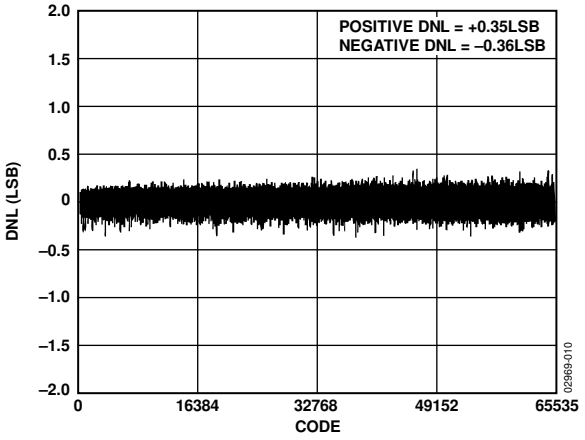


Figure 10. Differential Nonlinearity vs. Code

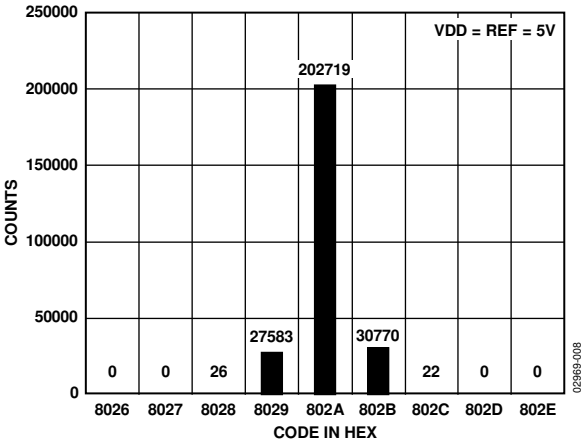


Figure 8. Histogram of a DC Input at the Code Center

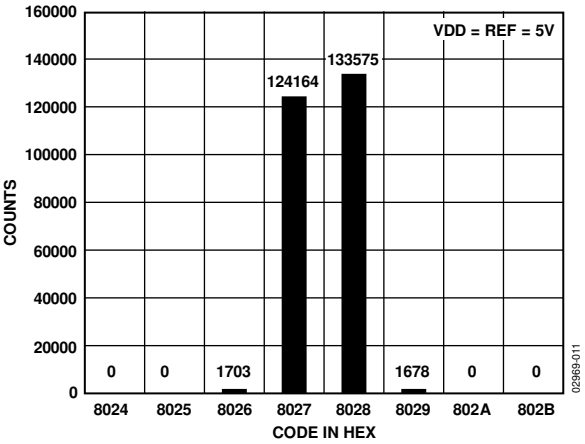


Figure 11. Histogram of a DC Input at the Code Transition

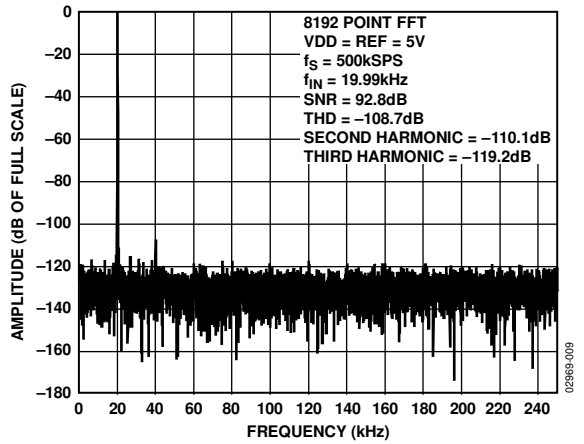


Figure 9. FFT Plot

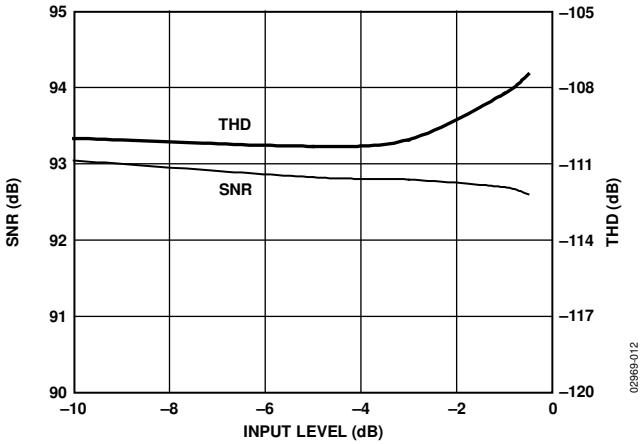


Figure 12. SNR and THD vs. Input Level

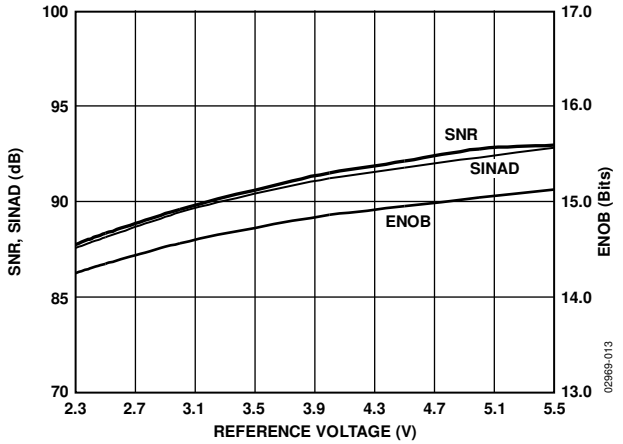


Figure 13. SNR, SINAD, and ENOB vs. Reference Voltage

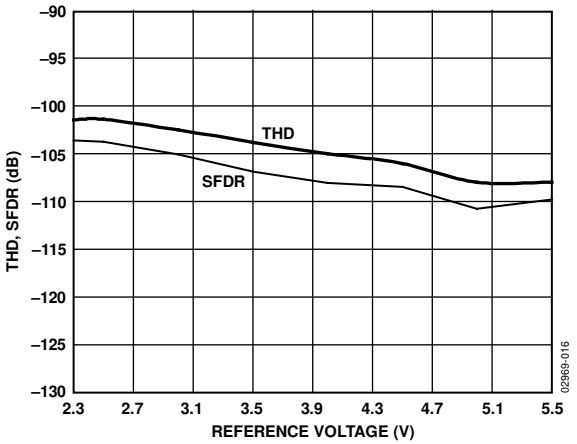


Figure 16. THD, SFDR vs. Reference Voltage

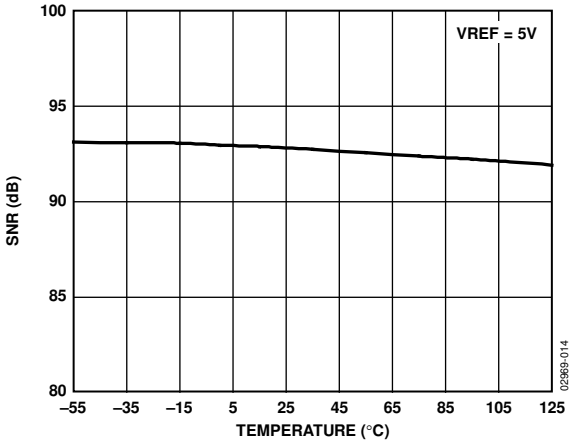


Figure 14. SNR vs. Temperature

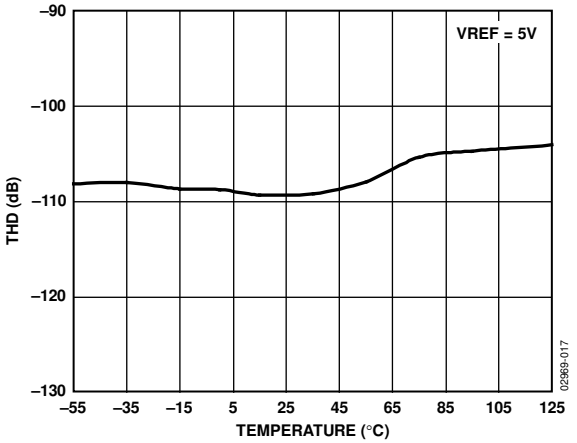


Figure 17. THD vs. Temperature

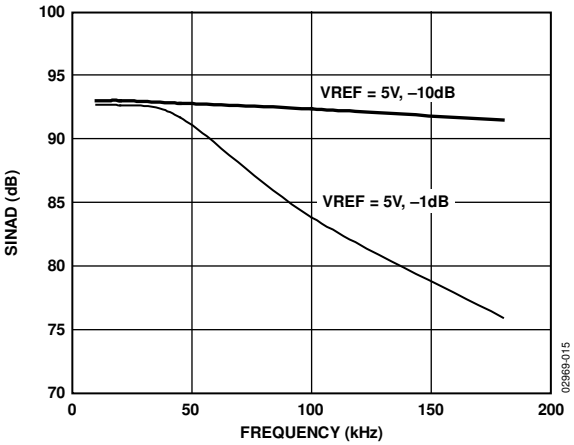


Figure 15. SINAD vs. Frequency

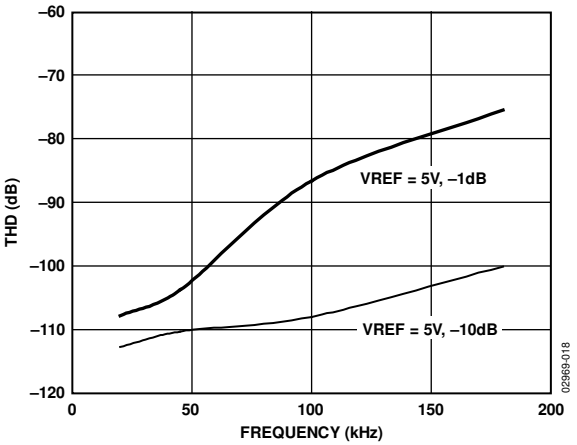


Figure 18. THD vs. Frequency

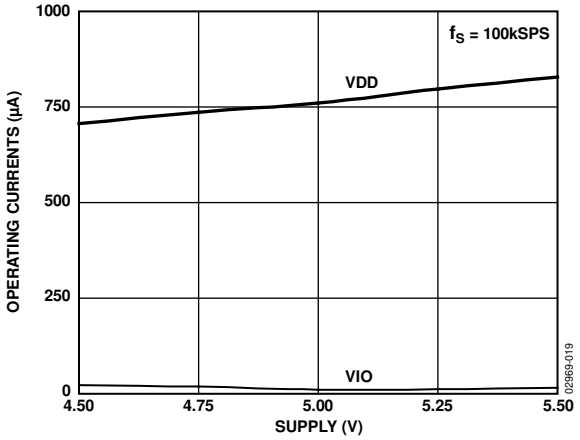


Figure 19. Operating Currents vs. Supply

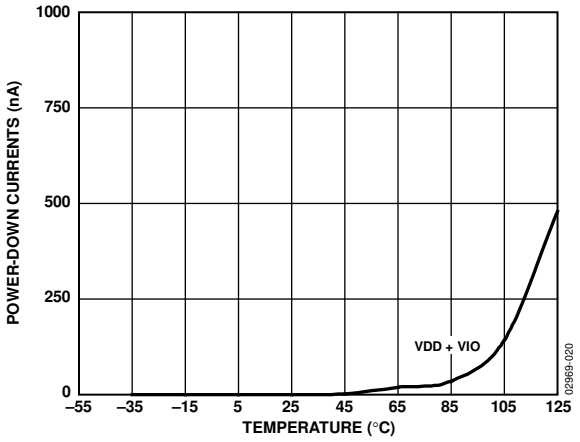


Figure 20. Power-Down Currents vs. Temperature

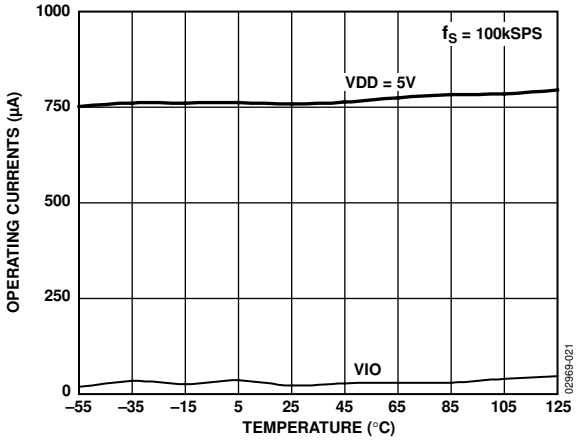


Figure 21. Operating Currents vs. Temperature

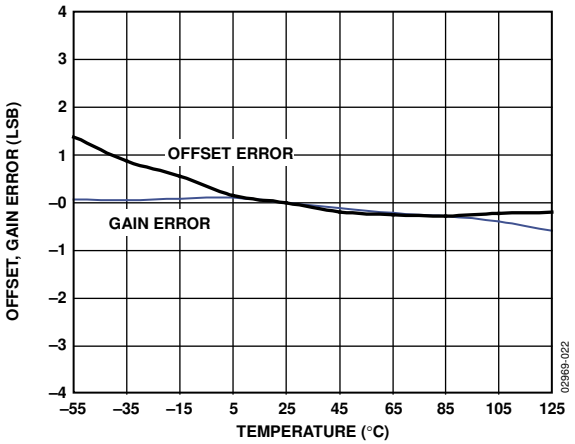


Figure 22. Offset and Gain Error vs. Temperature

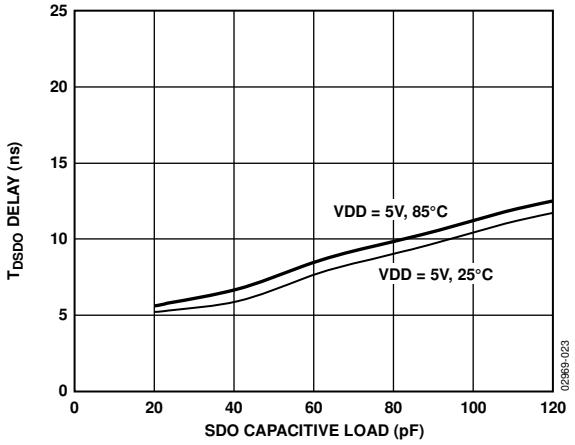


Figure 23. t_{DSDO} Delay vs. Capacitance Load and Supply

THEORY OF OPERATION

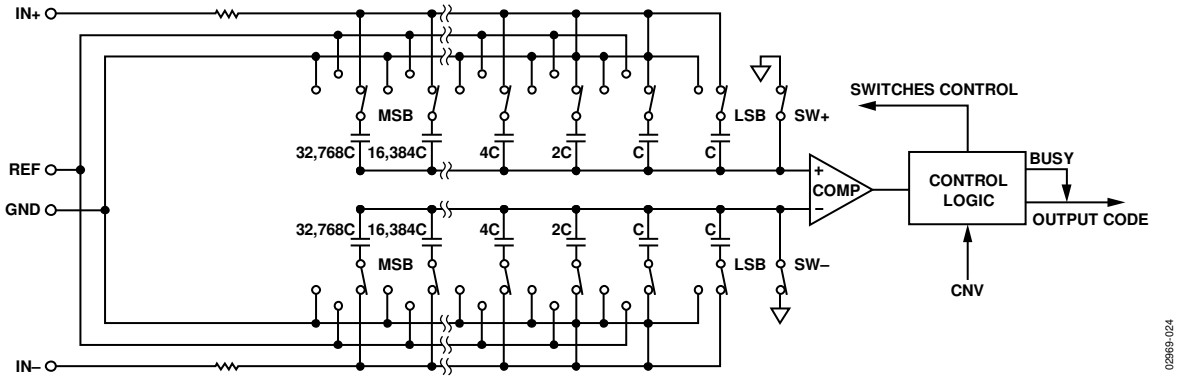


Figure 24. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7686 is a fast, low power, single-supply, precise 16-bit ADC using a successive approximation architecture.

The AD7686 is capable of converting 500,000 samples per second (500 kSPS) and powers down between conversions. For example, when operating at 100 SPS, the device consumes 3.75 µW typically, which is ideal for battery-powered applications.

The AD7686 provides the user with on-chip, track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multiple, multiplexed channel applications.

The AD7686 is specified from 4.5 V to 5.5 V and can be interfaced to any of the 1.8 V to 5 V digital logic family. It is housed in a 10-lead MSOP or a tiny 10-lead LFCSP that combines space savings and allows flexible configurations.

This device is pin-for-pin-compatible with the AD7685, AD7687, and AD7688.

CONVERTER OPERATION

The AD7686 is a successive approximation ADC based on a charge redistribution DAC. Figure 24 shows a simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors, which are connected to two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator input are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs. Therefore, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase initiates. When the conversion phase begins, SW+ and SW− are opened first.

The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs IN+ and IN−, captured at the end of the acquisition phase, is applied to the comparator inputs, causing the comparator to become unbalanced.

By switching each element of the capacitor array between GND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ . . . $V_{REF}/65536$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the part returns to the acquisition phase and the control logic generates the ADC output code and a busy signal indicator. Because the AD7686 has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

Transfer Functions

The ideal transfer characteristic for the AD7686 is shown in Figure 25 and Table 7.

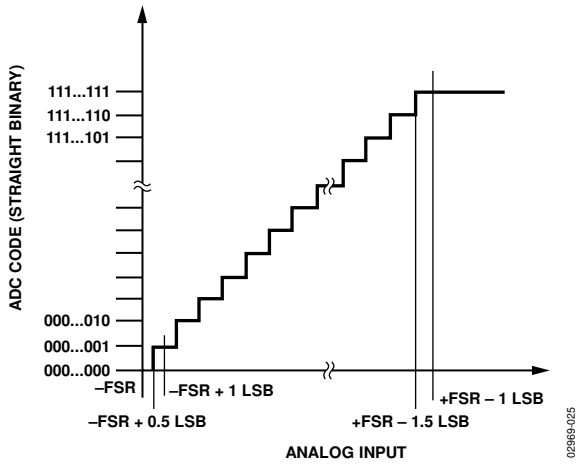


Figure 25. ADC Ideal Transfer Function

Table 7. Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 5 V	Digital Output Code Hexadecimal
FSR – 1 LSB	4.999924 V	FFFF[1]
Midscale + 1 LSB	2.500076 V	8001
Midscale	2.5 V	8000
Midscale – 1 LSB	2.499924 V	7FFF
–FSR + 1 LSB	76.3 µV	0001
–FSR	0 V	0000[2]

TYPICAL CONNECTION DIAGRAM

Figure 26 shows an example of the recommended connection diagram for the AD7686 when multiple supplies are available.

[1] This is also the code for an overranged analog input (V_{IN+} – V_{IN-} above V_{REF} – V_{GND}).
[2] This is also the code for an underranged analog input (V_{IN+} – V_{IN-} below V_{GND}).

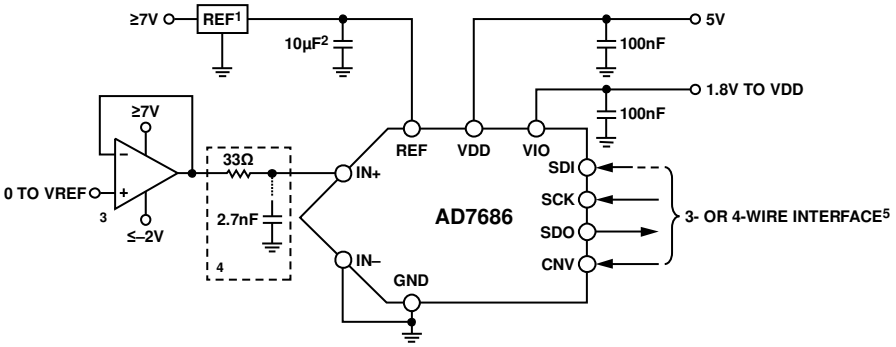


Figure 26. Typical Application Diagram with Multiple Supplies

ANALOG INPUT

Figure 27 shows an equivalent circuit of the input structure of the AD7686. The two diodes, D1 and D2, provide ESD protection for the analog inputs IN+ and IN−. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V because this causes these diodes to begin to forward-bias and start conducting current. These diodes can handle a forward-biased current of 130 mA maximum. For instance, these conditions could eventually occur when the input buffer's (U1) supplies are different from VDD. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part.

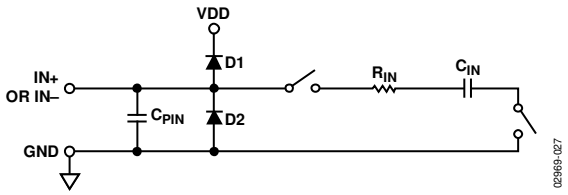


Figure 27. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the differential signal between IN+ and IN−. By using this differential input, small signals common to both inputs are rejected, as shown in Figure 28, which represents the typical CMRR over frequency. For instance, by using IN− to sense a remote signal ground, ground potential differences between the sensor and the local ADC ground are eliminated.

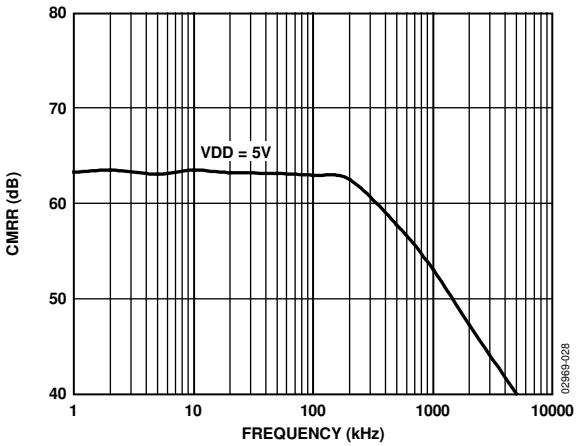


Figure 28. Analog Input CMRR vs. Frequency

During the acquisition phase, the impedance of the analog inputs (IN+ or IN−) can be modeled as a parallel combination of capacitor, C_{PIN}, and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 600 Ω and is a lumped component made up of some serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor. During the conversion phase, where the switches are opened, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a 1-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise.

When the source impedance of the driving circuit is low, the AD7686 can be driven directly. Large source impedances significantly affect the ac performance, especially THD. The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency, as shown in Figure 29.

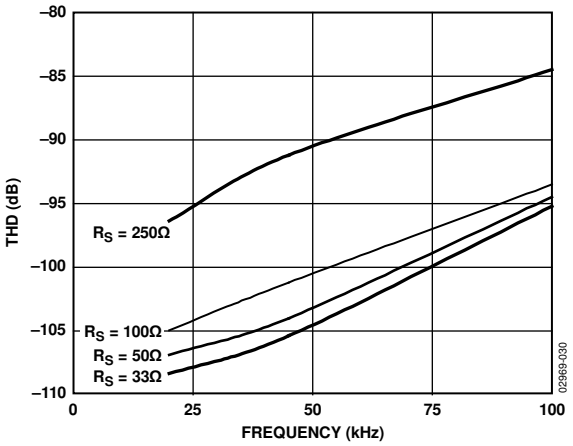


Figure 29. THD vs. Analog Input Frequency and Source Resistance

DRIVER AMPLIFIER CHOICE

Although the AD7686 is easy to drive, the driver amplifier should meet the following requirements:

- The noise generated by the driver amplifier needs to be kept as low as possible to preserve the SNR and transition noise performance of the AD7686. Note that the AD7686 has a noise much lower than most of the other 16-bit ADCs and, therefore, can be driven by a noisier amplifier to meet a given system noise specification. The noise coming from the amplifier is filtered by the AD7686 analog input circuit 1-pole, low-pass filter made by R_{IN} and C_{IN} or by the external filter, if one is used. Because the typical noise of the AD7686 is 37 µV rms, the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20\log\left(\frac{37}{\sqrt{37^2 + \frac{\pi}{2} f_{-3dB} (Ne_N)^2}}\right)$$

  where:

  f_{-3dB} is the input bandwidth in MHz of the AD7686 (9 MHz) or the cutoff frequency of the input filter, if one is used.

  N is the noise gain of the amplifier (for example, 1 in buffer configuration).

  e_N is the equivalent input noise voltage of the op amp, in nV/√Hz.

- For ac applications, the driver should have a THD performance commensurate with the AD7686. Figure 18 shows the THD vs. frequency that the driver should exceed.
- For multichannel multiplexed applications, the driver amplifier and the AD7686 analog input circuit must settle a full-scale step onto the capacitor array at a 16-bit level (0.0015%). In the data sheet for the amplifier, settling at 0.1% to 0.01% is more commonly specified. This could differ significantly from the settling time at a 16-bit level and should be verified prior to driver selection.

Table 8. Recommended Driver Amplifiers

Amplifier	Typical Application
ADA4841-x	Very low noise and low power
AD8605, AD8615	5 V single-supply, low power
AD8655	5 V single-supply, low power
OP184	Low power, low noise, and low frequency
AD8021	Very low noise and high frequency
AD8022	Very low noise and high frequency
AD8519	Small, low power and low frequency
AD8031	High frequency and low power

VOLTAGE REFERENCE INPUT

The AD7686 voltage reference input, REF, has a dynamic input impedance and should, therefore, be driven by a low impedance source with efficient decoupling between the REF and GND pins, as explained in the Layout section.

When REF is driven by a very low impedance source, such as a reference buffer using the AD8031 or the AD8605, a 10 µF (X5R, 0805 size) ceramic chip capacitor is appropriate for optimum performance.

If an unbuffered reference voltage is used, the decoupling value depends on the reference used. For instance, a 22 µF (X5R, 1206 size) ceramic chip capacitor is appropriate for optimum performance using a low temperature drift ADR43x reference.

If desired, smaller reference decoupling capacitor values down to 2.2 µF can be used with a minimal impact on performance, especially DNL.

Regardless, there is no need for an additional lower value ceramic decoupling capacitor, such as 100 nF, between the REF and GND pins.

POWER SUPPLY

The AD7686 is specified at 4.5 V to 5.5 V. The device uses two power supply pins: a core supply VDD and a digital input/output interface supply VIO. VIO allows direct interface with any logic between 1.8 V and VDD. To reduce the supplies needed, the VIO and VDD can be tied together.

The AD7686 is independent of power supply sequencing between VIO and VDD. Additionally, it is very insensitive to power supply variations over a wide frequency range, as shown in Figure 30, which represents PSRR over frequency.

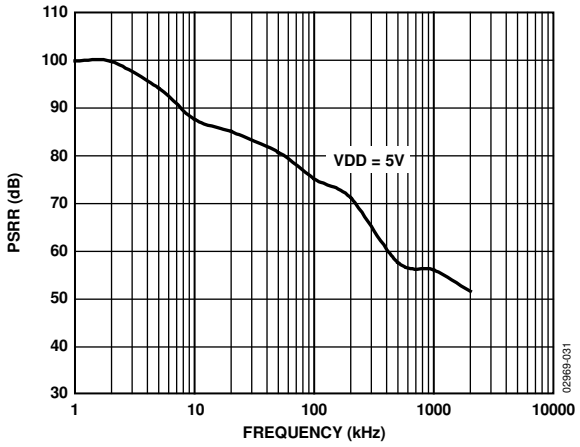


Figure 30. PSRR vs. Frequency

The AD7686 powers down automatically at the end of each conversion phase and, therefore, the power scales linearly with the sampling rate, as shown in Figure 31. This makes the part ideal for low sampling rates (even a few Hz) and low battery-powered applications.

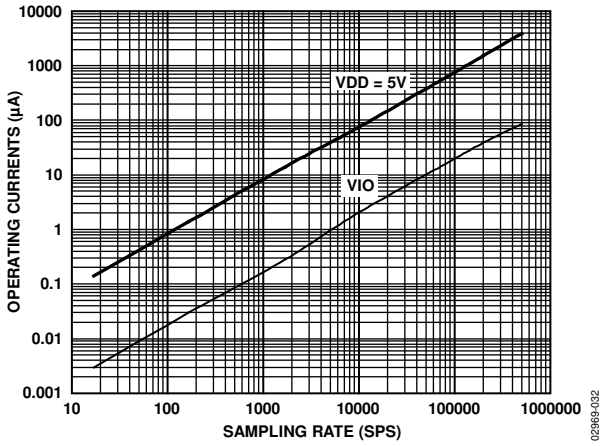
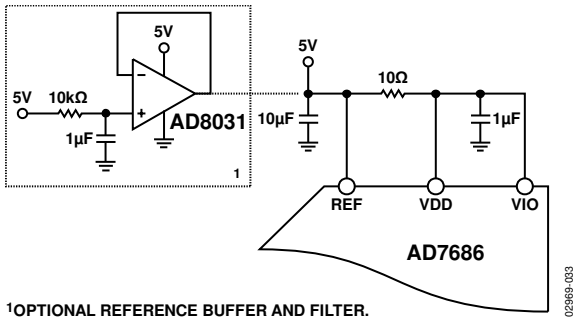


Figure 31. Operating Currents vs. Sampling Rate

SUPPLYING THE ADC FROM THE REFERENCE

For simplified applications, the AD7686, with its low operating current, can be supplied directly using the reference circuit shown in Figure 32. The reference line can be driven by either:

- The system power supply directly.
- A reference voltage with enough current output capability, such as the ADR43x.
- A reference buffer, such as the AD8031, which can also filter the system power supply, as shown in Figure 32.



[1]OPTIONAL REFERENCE BUFFER AND FILTER.

Figure 32. Example of Application Circuit

DIGITAL INTERFACE

Though the AD7686 has a reduced number of pins, it offers flexibility in its serial interface modes.

The AD7686, when in $\overline{CS}$ mode, is compatible with SPI, QSPI, digital hosts, and DSPs, such as Blackfin® ADSP-BF53x or ADSP-219x. This interface can use either 3-wire or 4-wire. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections useful, for instance, in isolated applications. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates the conversions, to be independent of the readback timing (SDI). This is useful in low jitter sampling or simultaneous sampling applications.

The AD7686, when in chain mode, provides a daisy-chain feature using the SDI input for cascading multiple ADCs on a single data line similar to a shift register.

The mode in which the part operates depends on the SDI level when the CNV rising edge occurs. The $\overline{CS}$ mode is selected if SDI is high, and the chain mode is selected if SDI is low. The SDI hold time is such that when SDI and CNV are connected together, the chain mode is always selected.

In either mode, the AD7686 offers the flexibility to optionally force a start bit in front of the data bits. This start bit can be used as a busy signal indicator to interrupt the digital host and trigger the data reading. Otherwise, without a busy indicator, the user must timeout the maximum conversion time prior to readback.

The busy indicator feature is enabled as follows:

- In $\overline{CS}$ mode, if CNV or SDI is low when the ADC conversion ends (see Figure 36 and Figure 40).
- In chain mode, if SCK is high during the CNV rising edge (see Figure 44).

$\overline{CS}$ MODE 3-WIRE, NO BUSY INDICATOR

This mode is most often used when a single AD7686 is connected to an SPI-compatible digital host. The connection diagram is shown in Figure 33, and the corresponding timing is provided in Figure 34.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. Once a conversion is initiated, it continues to completion irrespective of the state of CNV. For instance, it could be useful to bring CNV low to select other SPI devices, such as analog multiplexers. However, CNV must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid generating the busy signal indicator. When the conversion is complete, the AD7686 enters the acquisition phase and powers down. When CNV goes low, the MSB is output onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges.

The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate provided it has an acceptable hold time. After the 16th SCK falling edge, or when CNV goes high, whichever occurs first, SDO returns to high impedance.

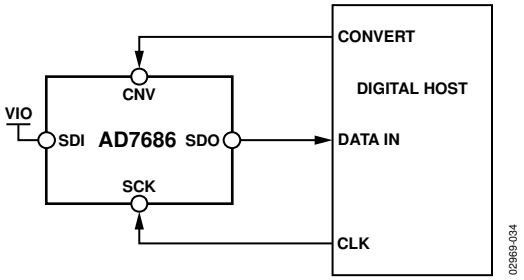


Figure 33. $\overline{CS}$ Mode 3-Wire, No Busy Indicator Connection Diagram (SDI High)

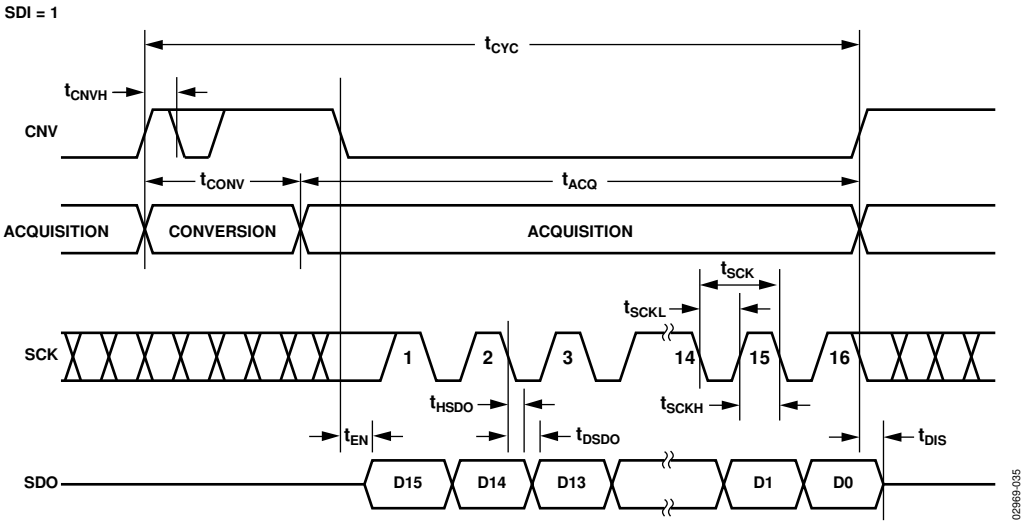


Figure 34. $\overline{CS}$ Mode 3-Wire, No Busy Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE 3-WIRE WITH BUSY INDICATOR

This mode is generally used when a single AD7686 is connected to an SPI-compatible digital host having an interrupt input. The connection diagram is shown in Figure 35, and the corresponding timing is provided in Figure 36.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. SDO is maintained in high impedance until the completion of the conversion, irrespective of the state of CNV. Prior to the minimum conversion time, CNV can be used to select other SPI devices, such as analog multiplexers. However, CNV must be returned low before the minimum conversion time and held low until the maximum conversion time to guarantee the generation of the busy signal indicator. When the conversion is complete, SDO goes from high impedance to low. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. The AD7686 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges.

Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 17th SCK falling edge or when CNV goes high, whichever occurs first, SDO returns to high impedance.

If multiple AD7686s are selected at the same time, the SDO output pin handles this connection without damage or induced latch-up. Meanwhile, it is recommended to keep this connection as short as possible to limit extra power dissipation.

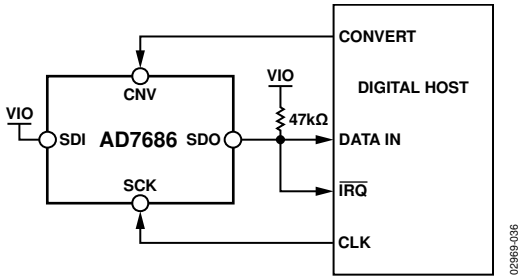


Figure 35. $\overline{CS}$ Mode 3-Wire with Busy Indicator Connection Diagram (SDI High)

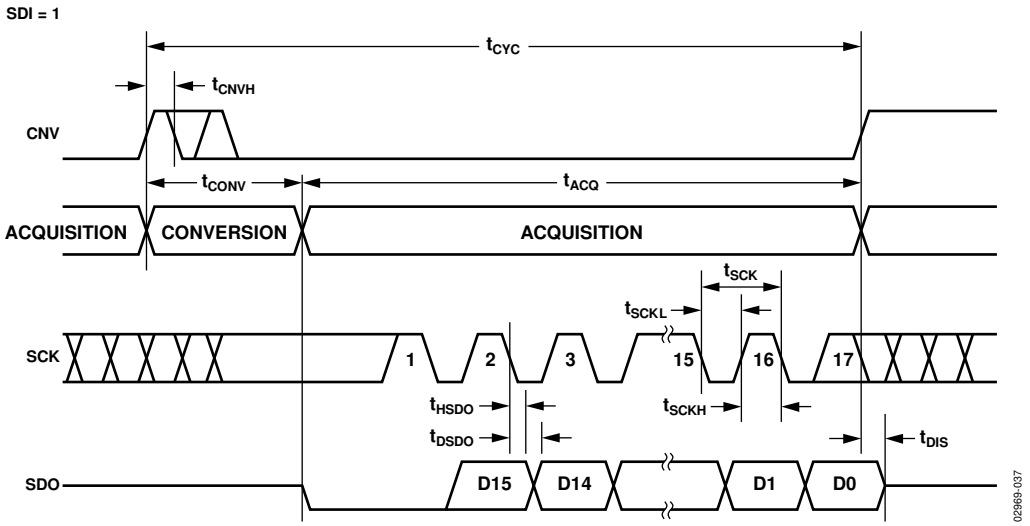


Figure 36. $\overline{CS}$ Mode 3-Wire with Busy Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE 4-WIRE, NO BUSY INDICATOR

This mode is generally used when multiple AD7686s are connected to an SPI-compatible digital host. A connection diagram example using two AD7686 devices is shown in Figure 37, and the corresponding timing is given in Figure 38.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI could be used to select other SPI devices, such as analog multiplexers. but SDI must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid the generation of the busy signal indicator. When the conversion is complete, the AD7686 enters the acquisition phase and powers down. Each ADC result can be read by bringing its SDI input low, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 16th SCK falling edge or when SDI goes high, whichever occurs first, SDO returns to high impedance and another AD7686 can be read.

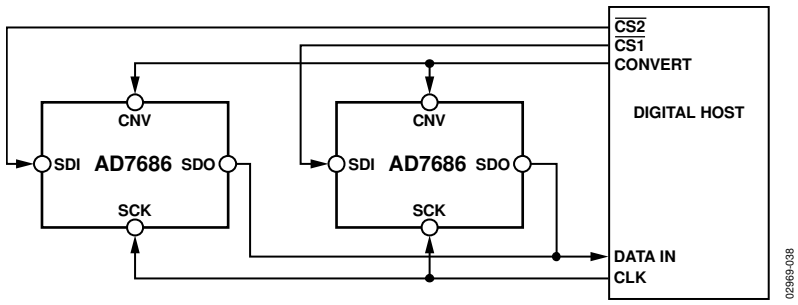


Figure 37. $\overline{CS}$ Mode 4-Wire, No Busy Indicator Connection Diagram

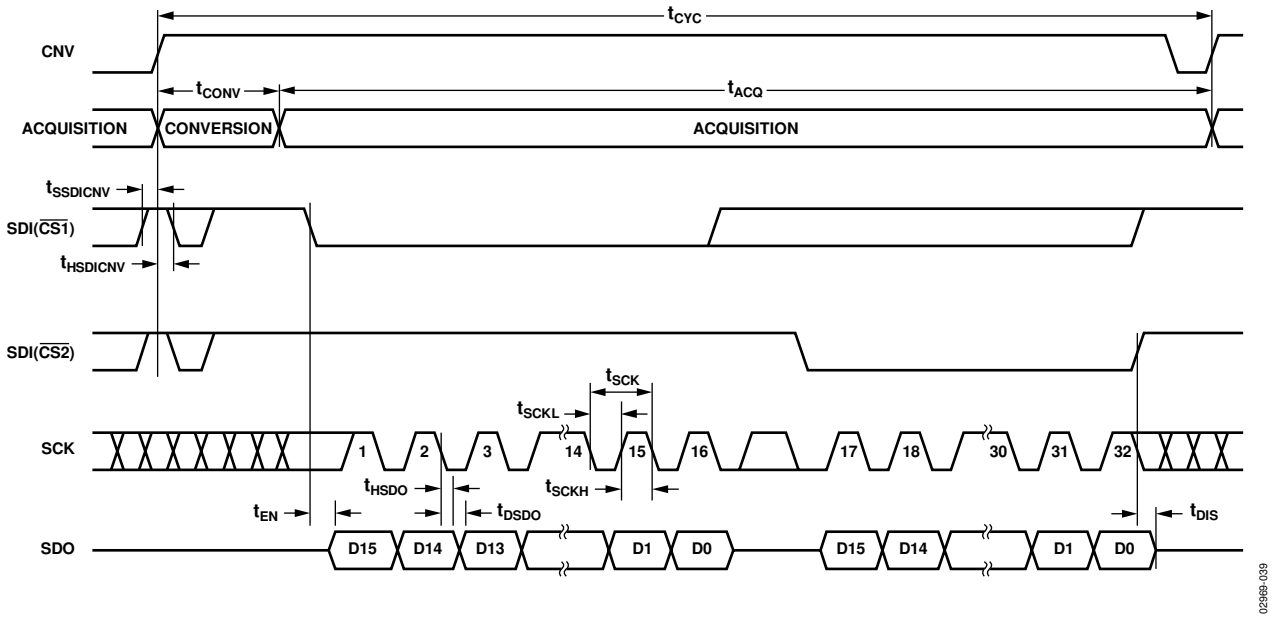


Figure 38. $\overline{CS}$ Mode 4-Wire, No Busy Indicator Serial Interface Timing

$\overline{CS}$ MODE 4-WIRE WITH BUSY INDICATOR

This mode is usually used when a single AD7686 is connected to an SPI-compatible digital host, which has an interrupt input, and when it is desired to keep CNV, which is used to sample the analog input, independent of the signal used to select the data reading. This requirement is particularly important in applications where low jitter on CNV is desired. The connection diagram is shown in Figure 39, and the corresponding timing is provided in Figure 40.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI can be used to select other SPI devices, such as analog multiplexers, but SDI must be returned low before the minimum conversion time and held low until the maximum conversion time to guarantee the generation of the busy signal indicator. When conversion is complete, SDO goes from high impedance to low.

With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data readback controlled by the digital host. The AD7686 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 17th SCK falling edge or SDI going high, whichever occurs first, the SDO returns to high impedance.

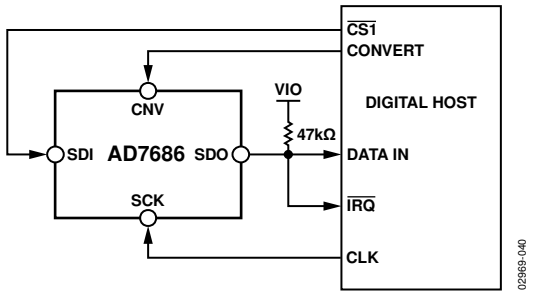


Figure 39. $\overline{CS}$ Mode 4-Wire with Busy Indicator Connection Diagram

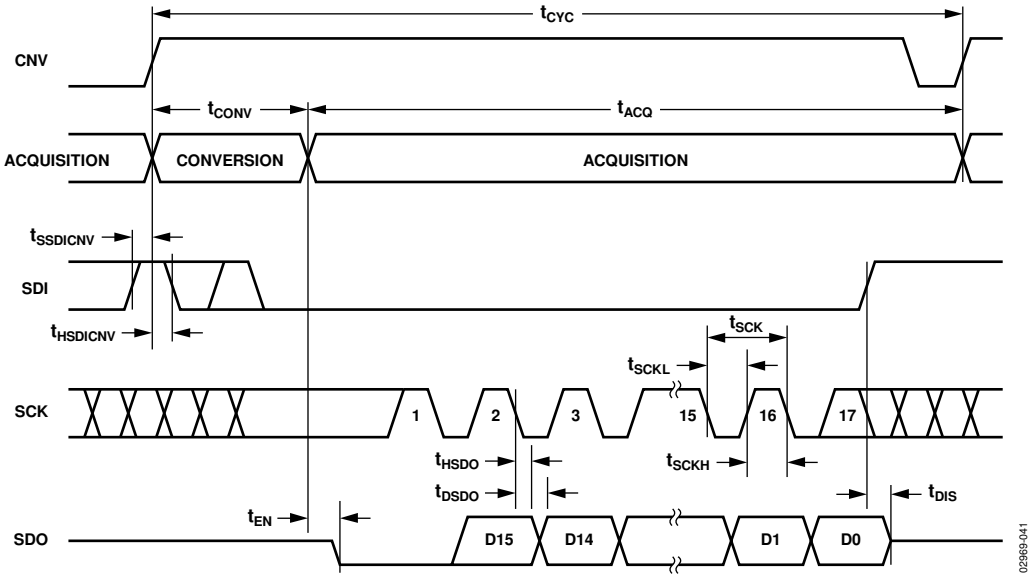


Figure 40. $\overline{CS}$ Mode 4-Wire with Busy Indicator Serial Interface Timing

CHAIN MODE, NO BUSY INDICATOR

This mode can be used to daisy-chain multiple AD7686s on a 3-wire serial interface. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using two AD7686s is shown in Figure 41, and the corresponding timing is given in Figure 42.

When SDI and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion, selects the chain mode, and disables the busy indicator. In this mode, CNV is held high during the conversion phase and the subsequent data readback.

When the conversion is complete, the MSB is output onto SDO, and the AD7686 enters the acquisition phase and powers down. The remaining data bits stored in the internal shift register are then clocked by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 16 × N clocks are required to read back the N ADCs. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate and, consequently, more AD7686s in the chain, provided the digital host has an acceptable hold time. The maximum conversion rate can be reduced due to the total readback time. For instance, with a 3 ns digital host setup time and 3 V interface, up to four AD7686s running at a conversion rate of 360 kSPS can be daisy-chained on a 3-wire port.

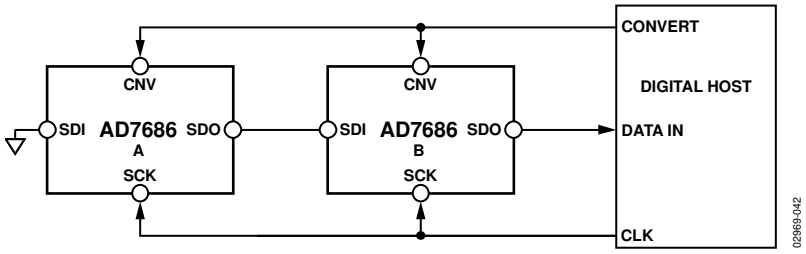


Figure 41. Chain Mode, No Busy Indicator Connection Diagram

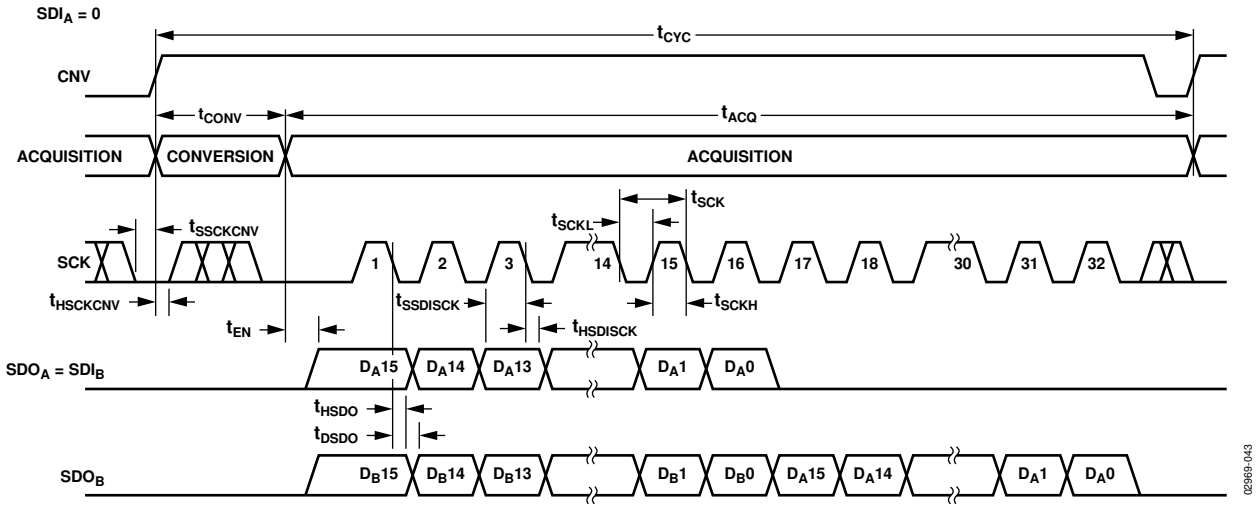


Figure 42. Chain Mode, No Busy Indicator Serial Interface Timing

CHAIN MODE WITH BUSY INDICATOR

This mode can be used to daisy-chain multiple AD7686s on a 3-wire serial interface while providing a busy indicator. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register. A connection diagram example using three AD7686s is shown in Figure 43, and the corresponding timing is given in Figure 44.

When SDI and CNV are low, SDO is driven low. With SCK high, a rising edge on CNV initiates a conversion, selects the chain mode, and enables the busy indicator feature. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When all ADCs in the chain have completed their conversions, the near-end ADC (ADC C in Figure 43) SDO is driven high.

This transition on SDO can be used as a busy indicator to trigger the data readback controlled by the digital host. The AD7686 then enters the acquisition phase and powers down. The data bits stored in the internal shift register are then clocked out, MSB first, by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 16 × N + 1 clocks are required to readback the N ADCs.

Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate and, consequently, more AD7686s in the chain, provided the digital host has an acceptable hold time. For instance, with a 3 ns digital host setup time and 3 V interface, up to four AD7686s running at a conversion rate of 360 kSPS can be daisy chained to a single 3-wire port.

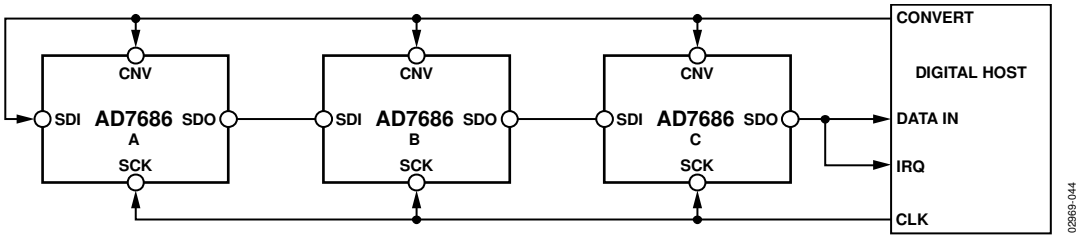


Figure 43. Chain Mode with Busy Indicator Connection Diagram

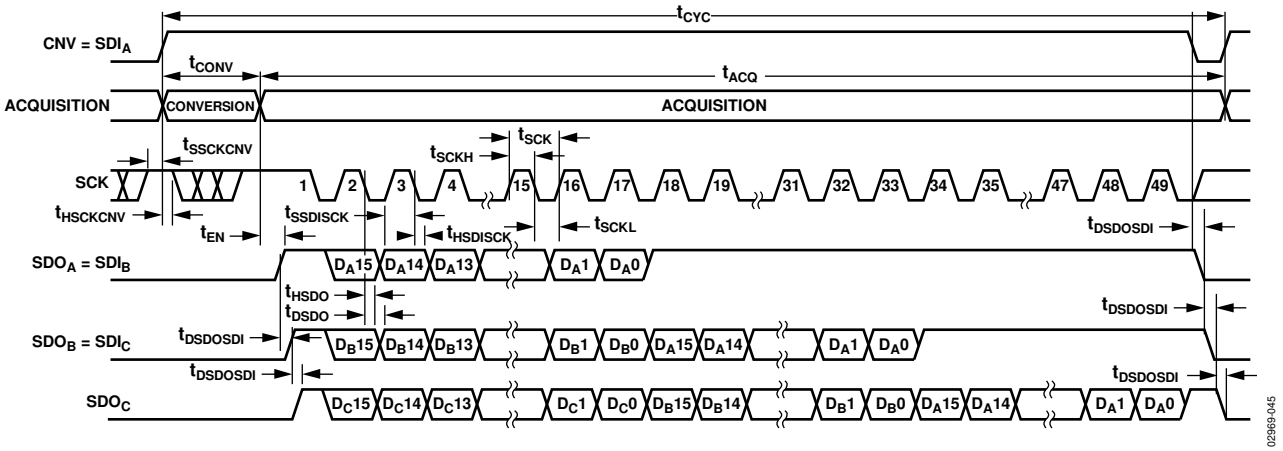


Figure 44. Chain Mode with Busy Indicator Serial Interface Timing

APPLICATION HINTS

LAYOUT

The printed circuit board (PCB) that houses the AD7686 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7686, with all its analog signals on the left side and all its digital signals on the right side, eases this task.

Avoid running digital lines under the device because doing so couples noise onto the die, unless a ground plane under the AD7686 is used as a shield. Fast switching signals, such as CNV or clocks, should never run near analog signal paths. Crossover of digital and analog signals should be avoided.

At least one ground plane should be used. It could be common or split between the digital and analog sections. In the latter case, the planes should be joined underneath the devices.

The AD7686 voltage reference input REF has a dynamic input impedance and should be decoupled with minimal parasitic inductances. This is done by placing the reference decoupling ceramic capacitor close to, and ideally right up against, the REF and GND pins and connecting it with wide, low impedance traces.

Finally, the AD7686 power supplies VDD and VIO should be decoupled with ceramic capacitors (typically 100 nF) placed close to the AD7686 and connected using short and wide traces. This provides low impedance paths and reduces the effect of glitches on the power supply lines. Examples of layouts that follow these rules are shown in Figure 45 and Figure 46.

EVALUATING THE PERFORMANCE OF THE AD7686

Other recommended layouts for the AD7686 are outlined in the documentation of the EVAL-AD7686SBZ evaluation board. The EVAL-AD7686SBZ evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-SDP-CB1Z.

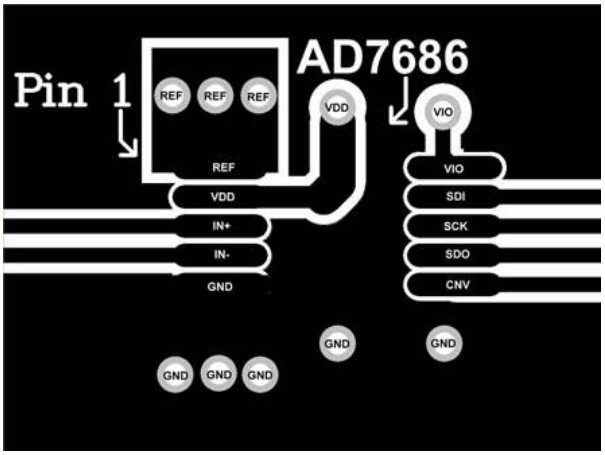


Figure 45. Example of Layout of the AD7686 (Top Layer)

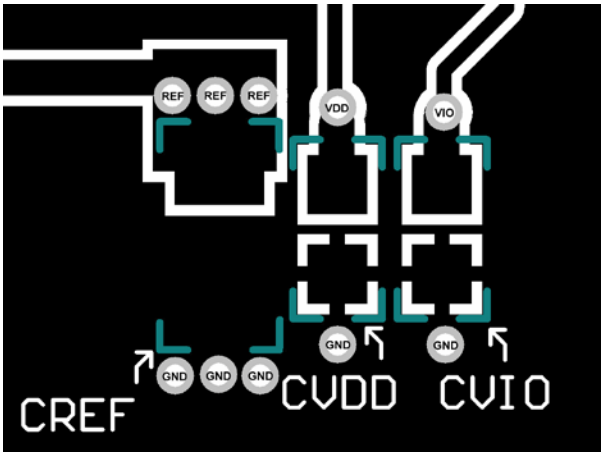


Figure 46. Example of Layout of the AD7686 (Bottom Layer)

TRUE 16-BIT ISOLATED APPLICATION EXAMPLE

In applications where high accuracy and isolation are required, such as power monitoring, motor control, and some medical equipment, the circuit shown in Figure 47, using the AD7686 and the ADuM1402C digital isolator, provides a compact and high performance solution.

Multiple AD7686 devices are daisy-chained to reduce the number of signals to isolate. Note that the SCKOUT, which is a readback of the AD7686 clock, has a very short skew with the DATA signal.

This skew is the channel-to-channel matching propagation delay of the digital isolator (t_{PSKCD}). This allows running the serial interface at the maximum speed of the digital isolator (45 Mbps for the ADuM1402C), which would have been otherwise limited by the cascade of the propagation delays of the digital isolator. For instance, four AD7686 devices running at 330 kSPS can be chained together.

The complete analog chain runs on a single 5 V supply using the ADR391 low dropout reference voltage and the rail-to-rail CMOS AD8618 amplifier while offering true bipolar input range.

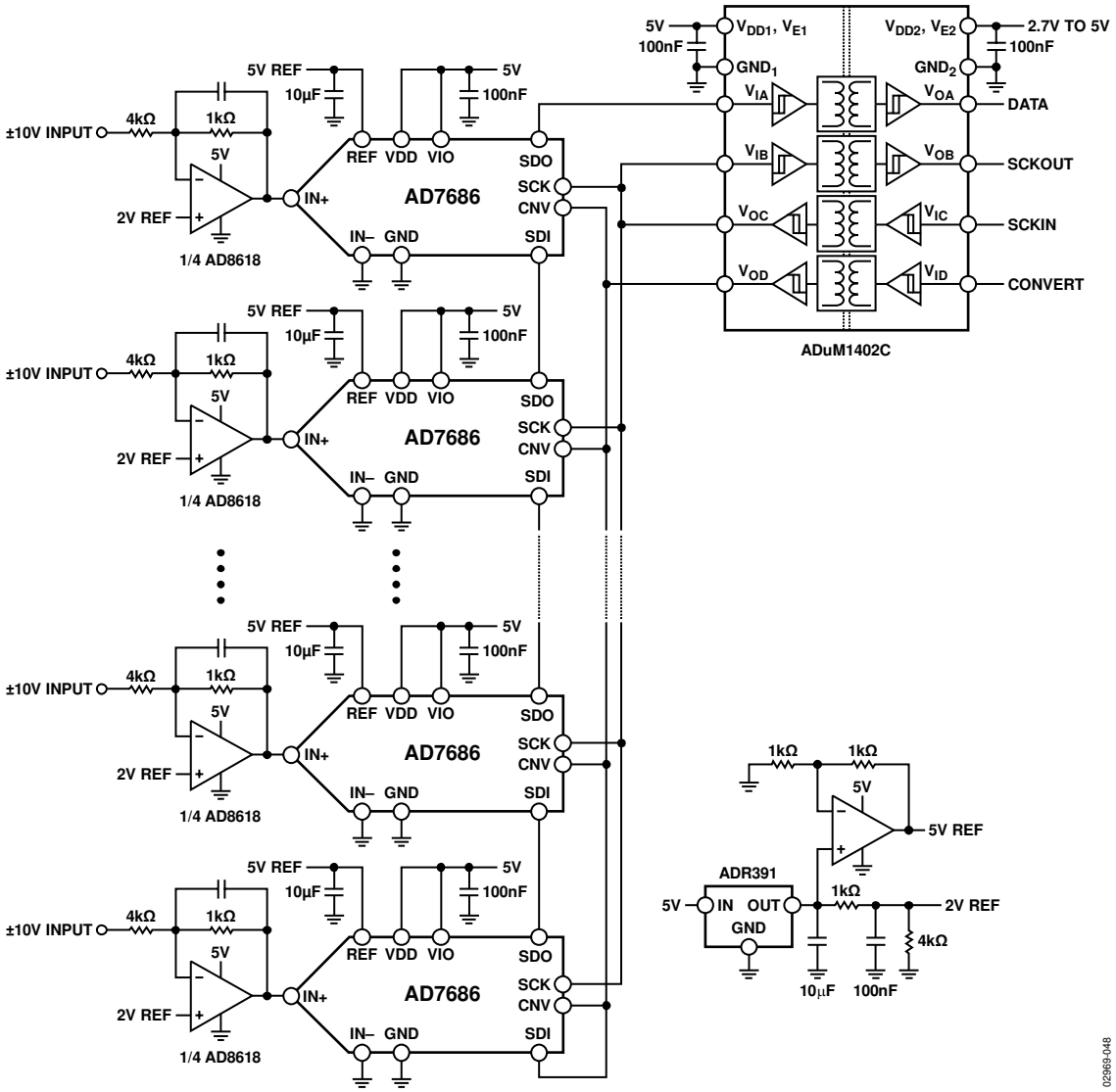


Figure 47. A True 16-Bit Isolated Simultaneous Sampling Acquisition System

OUTLINE DIMENSIONS

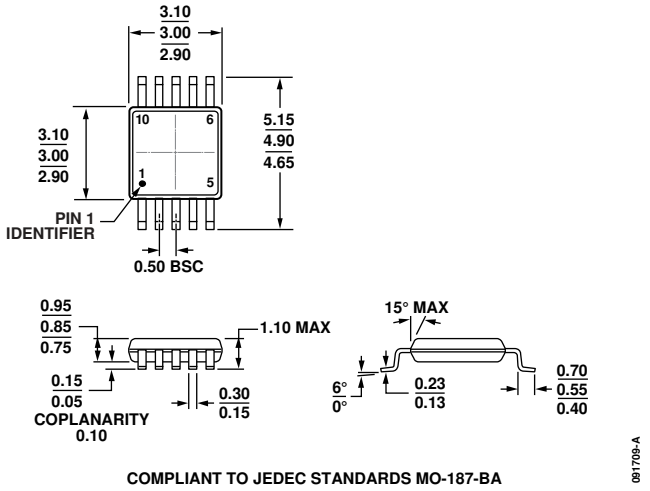


Figure 48. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

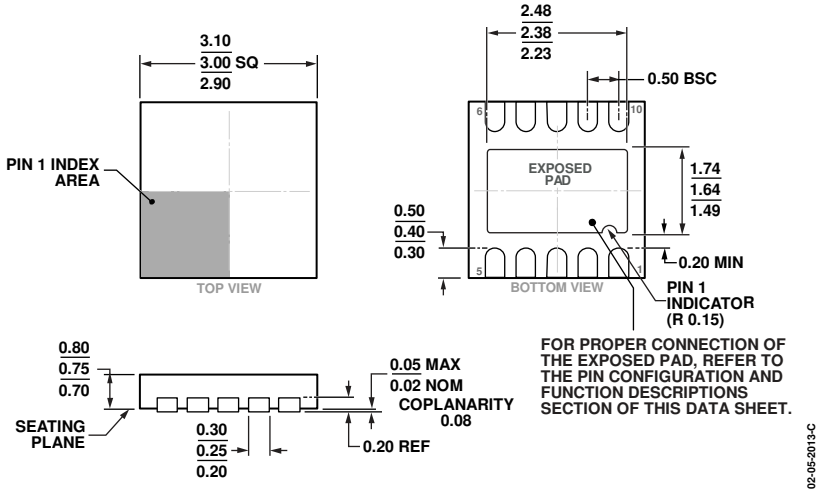


Figure 49. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Integral Nonlinearity	Temperature Range	Ordering Quantity	Package Description	Package Option	Branding
AD7686BCPZRL	±3 LSB max	−40°C to +85°C	Reel, 5000	10-Lead LFCSP_WD	CP-10-9	C02#
AD7686BCPZRL7	±3 LSB max	−40°C to +85°C	Reel, 1500	10-Lead LFCSP_WD	CP-10-9	C02#
AD7686BRMZ	±3 LSB max	−40°C to +85°C	Tube, 50	10-Lead MSOP	RM-10	C3N
AD7686BRMZRL7	±3 LSB max	−40°C to +85°C	Reel, 1000	10-Lead MSOP	RM-10	C3N
AD7686CCPZRL	±2 LSB max	−40°C to +85°C	Reel, 5000	10-Lead LFCSP_WD	CP-10-9	C2G#
AD7686CCPZRL7	±2 LSB max	−40°C to +85°C	Reel, 1500	10-Lead LFCSP_WD	CP-10-9	C2G#
AD7686CRMZ	±2 LSB max	−40°C to +85°C	Tube, 50	10-Lead MSOP	RM-10	C3P
AD7686CRMZRL7	±2 LSB max	−40°C to +85°C	Reel, 1000	10-Lead MSOP	RM-10	C3P
EVAL-AD7686SDZ				Evaluation Board		
EVAL-SDP-CB1Z				Controller Board		

[1] Z = RoHS Compliant Part, # denotes RoHS Compliant product may be top or bottom marked.
[2] The EVAL-AD786SDZ can be used as a standalone evaluation board or in conjunction with the EVAL-SDP-CB1Z for evaluation and/or demonstration purposes.
[3] The EVAL-SDP-CB1Z allows a PC to control and communicate with all Analog Devices, Inc. evaluation boards ending in the SDZ designator.

NOTES

NOTES

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