



# High Speed CMOS Transceivers With Parity

QS54/74FCT833T  
QS54/74FCT853T

QS54/74FCT2833T  
QS54/74FCT2853T

ADVANCE INFORMATION

## FEATURES/BENEFITS

- Pin and function compatible to the Am29833/53
- Parity generation and detection
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs
- TTL compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

### FCT 833T/53T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- I<sub>OL</sub> = 48 mA Com., 32 mA Mil.

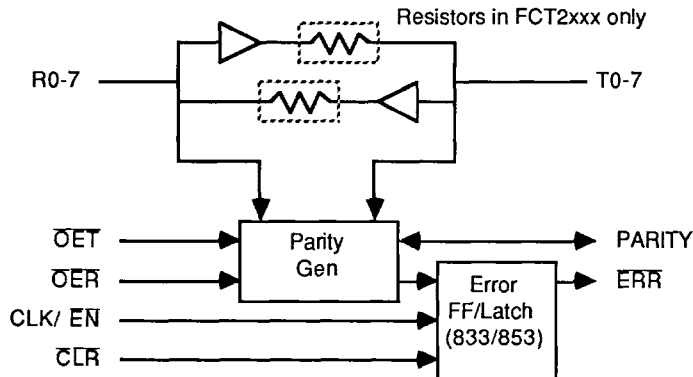
### FCT 2833T/53T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- I<sub>OL</sub> = 12 mA Com.

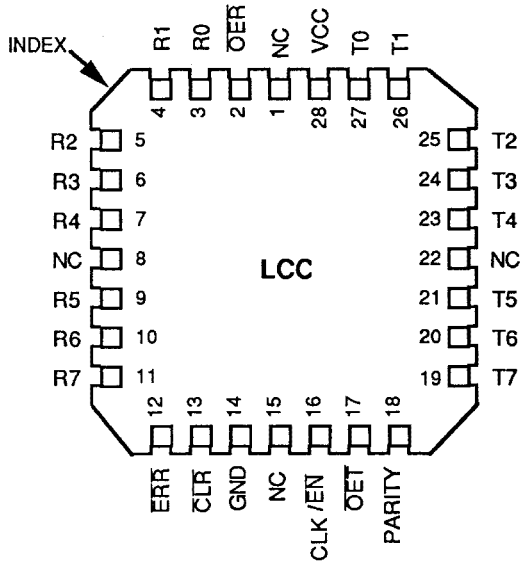
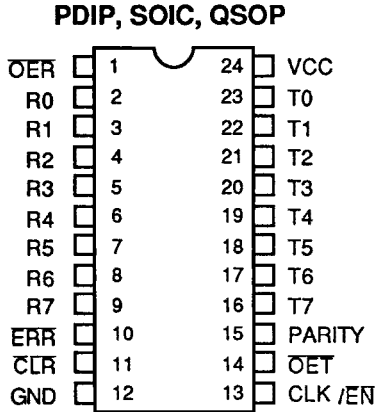
## DESCRIPTION

The QSFCT833T/853T and QSFCT2833T/2853T are 8-bit high-speed CMOS TTL compatible transceivers registers with three-state outputs and parity generate/detect logic that are ideal for driving high capacitance loads such as memory and address buses. These parts generate and check odd parity. All lows (zeros) in generates a one for parity. The 833 has a FF and the 853 has a latch to record a parity error defined as a difference between parity generated from the inputs and the parity bit supplied with the inputs. Once the FF/latch is set, it remains set until cleared by a pulse on CLR. ERR is the output from this FF/latch and is open drain allowing multiple devices to be ORed. The 2833/53 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2833 series parts can replace the 833 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V<sub>CC</sub> is removed from the device.

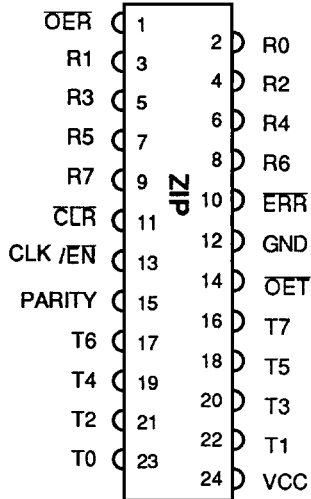
## FUNCTIONAL BLOCK DIAGRAM



FCT833/853 PIN CONFIGURATIONS



Note: Pin 13 (pin 16 of LCC) is CLK on 833 and EN on 853.



**PIN DESCRIPTIONS**

| Name           | I/O | Function                  |
|----------------|-----|---------------------------|
| R <sub>i</sub> | I/O | Data Bus, R side          |
| T <sub>i</sub> | I/O | Data Bus, T side          |
| OET            | I   | Enable R to T             |
| OER            | I   | Enable T to R             |
| CLK            | I   | Parity FF Clock (833)     |
| EN             | I   | Parity Latch Enable (853) |
| CLR            | I   | Parity FF/Latch Clear     |
| PARITY         | O   | Parity                    |
| ERR            | O   | Parity Error (Open Drain) |

All packages are shown with the Top View

FCT833 FUNCTION TABLE

| INPUTS |     |     |            |                                 |                                   | OUTPUTS |    |        |         | Function   |
|--------|-----|-----|------------|---------------------------------|-----------------------------------|---------|----|--------|---------|--|
| OET    | OER | CLR | CLK        | Ri ( $\Sigma$ of H's)           | Ti Incl Parity ( $\Sigma$ of H's) | Ri      | Ti | Parity | ERR     |  |
| L      | H   | H   | $\uparrow$ | H(Odd)                          | NA                                | NA      | H  | L      | H       | Transmit data from R port to T port with parity; receiving path is disabled                          |
| L      | H   | H   | $\uparrow$ | H(Even)                         | NA                                | NA      | H  | H      | L       |  |
| L      | H   | H   | $\uparrow$ | L(Odd)                          | NA                                | NA      | L  | L      | H       |  |
| L      | H   | H   | $\uparrow$ | L(even)                         | NA                                | NA      | L  | H      | L       |  |
| H      | L   | H   | $\uparrow$ | NA                              | H(odd)                            | H       | NA | NA     | H       | Recieve data from T port to R port with parity test resulting in flag; transmitting path is disabled |
| H      | L   | H   | $\uparrow$ | NA                              | H(even)                           | H       | NA | NA     | L       |  |
| H      | L   | H   | $\uparrow$ | NA                              | L(odd)                            | L       | NA | NA     | H       |  |
| H      | L   | H   | $\uparrow$ | NA                              | H(even)                           | L       | NA | NA     | L       |  |
| X      | X   | L   | X          | X                               | X                                 | NA      | NA | NA     | H       | Clear error flag register  |
| H      | H   | H   | H or L     | Hor<br>L(Odd)<br>Hor<br>L(even) | X                                 | Z       | Z  | Z      | No chng | Tranmit and receive paths disabled. Parity in transmit mode  |
| H      | H   | L   | X          |                                 | X                                 | Z       | Z  | Z      | H       |  |
| H      | H   | H   | $\uparrow$ |                                 | X                                 | Z       | Z  | Z      | H       |  |
| H      | H   | H   | $\uparrow$ |                                 | X                                 | Z       | Z  | Z      | L       |  |
| L      | L   | H   | $\uparrow$ | H(Odd)                          | NA                                | NA      | H  | H      | L       | Error checking   |
| L      | L   | H   | $\uparrow$ | H(Even)                         | NA                                | NA      | H  | L      | H       |  |
| L      | L   | H   | $\uparrow$ | L(Odd)                          | NA                                | NA      | L  | H      | L       |  |
| L      | L   | H   | $\uparrow$ | L(even)                         | NA                                | NA      | L  | L      | H       |  |

NOTES :

- 1.. Output state assumes HIGH output before the state.
2. Odd = Odd number of logic one's  
 Even = Even number of logic one's  
 i = 0,1,2,3,4,5,6,7  
 X = Don't care

**FCT853 FUNCTION TABLE**

| OET | OER | CLR | EN | Ri | Ri ( $\Sigma$ of H's) | Ti | Ti Incl Parity ( $\Sigma$ of H's) | Ri | Ti | Parity | ERR   | Function  |
|-----|-----|-----|----|----|-----------------------|----|-----------------------------------|----|----|--------|-------|---|
| L   | H   | X   | X  | H  | ODD                   | NA | NA                                | NA | H  | L      | NA    | Transmit data from R port to T port with parity; receiveing path is disabled                    |
| L   | H   | X   | X  | H  | EVEN                  | NA | NA                                | NA | H  | H      | NA    |   |
| L   | H   | X   | X  | L  | ODD                   | NA | NA                                | NA | L  | L      | NA    |   |
| L   | H   | X   | X  | L  | EVEN                  | NA | NA                                | NA | L  | H      | NA    |   |
| H   | L   | X   | L  | NA | NA                    | H  | ODD                               | H  | NA | NA     | H     | Receve data from T port to R port with parity test resulting in flag; transmit path is disabled |
| H   | L   | X   | L  | NA | NA                    | H  | EVEN                              | H  | NA | NA     | L     |   |
| H   | L   | X   | L  | NA | NA                    | L  | ODD                               | L  | NA | NA     | H     |   |
| H   | L   | X   | L  | NA | NA                    | L  | EVEN                              | L  | NA | NA     | L     |   |
| H   | L   | H   | H  | NA | NA                    | X  | X                                 | X  | NA | NA     | Store | Store the state of the error flag latch   |
| X   | X   | L   | H  | X  | X                     | X  | X                                 | X  | NA | NA     | H     | Clear error flag latch  |
| H   | H   | H   | H  | X  | X                     | X  | X                                 | Z  | Z  | Z      | Store | Transmit and receive paths are disabled. Prity logic in transmit mode                           |
| H   | H   | L   | H  | X  | X                     | X  | X                                 | Z  | Z  | Z      | H     |   |
| H   | H   | X   | L  | L  | ODD                   | X  | X                                 | Z  | Z  | Z      | H     |   |
| H   | H   | X   | L  | H  | EVEN                  | X  | X                                 | Z  | Z  | Z      | L     |   |
| L   | L   | X   | X  | H  | ODD                   | NA | NA                                | NA | H  | H      | NA    | Error checking  |
| L   | L   | X   | X  | H  | EVEN                  | NA | NA                                | NA | H  | L      | NA    |   |
| L   | L   | X   | X  | L  | ODD                   | NA | NA                                | NA | L  | H      | NA    |   |
| L   | L   | X   | X  | L  | EVEN                  | NA | NA                                | NA | L  | L      | NA    |   |
| L   | L   | H   | X  | H  | H(Odd)                |    | NA                                | NA | H  | H      | L     | Error checking  |
| L   | L   | H   | X  | H  | H(Even)               |    | NA                                | NA | H  | L      | H     |   |
| L   | L   | H   | X  | L  | L(Odd)                |    | NA                                | NA | L  | H      | L     |   |
| L   | L   | H   | X  | L  | L(even)               |    | NA                                | NA | L  | L      | H     |   |

**NOTES :**

- 1.. Output state assumes HIGH output before the state.
2. Odd = Odd number of logic one's  
 Even = Even number of logic one's  
 i = 0,1,2,3,4,5,6,7  
 X = Don't care

**833 ERROR FLAG OUTPUT FUNCTION**

| Inputs |     | Internal to Device | Output Pre-state | Output | Function             |
|--------|-----|--------------------|------------------|--------|----------------------|
| CLR    | CLK | Point"P"           | ERR n-1          | ERR    |                      |
| H      | ↑   | H                  | H                | H      | Sample (1's Capture) |
| H      | ↑   | —                  | L                | L      |                      |
| H      | ↑   | L                  | —                | L      |                      |
| L      | —   | —                  | —                | H      | Clear                |

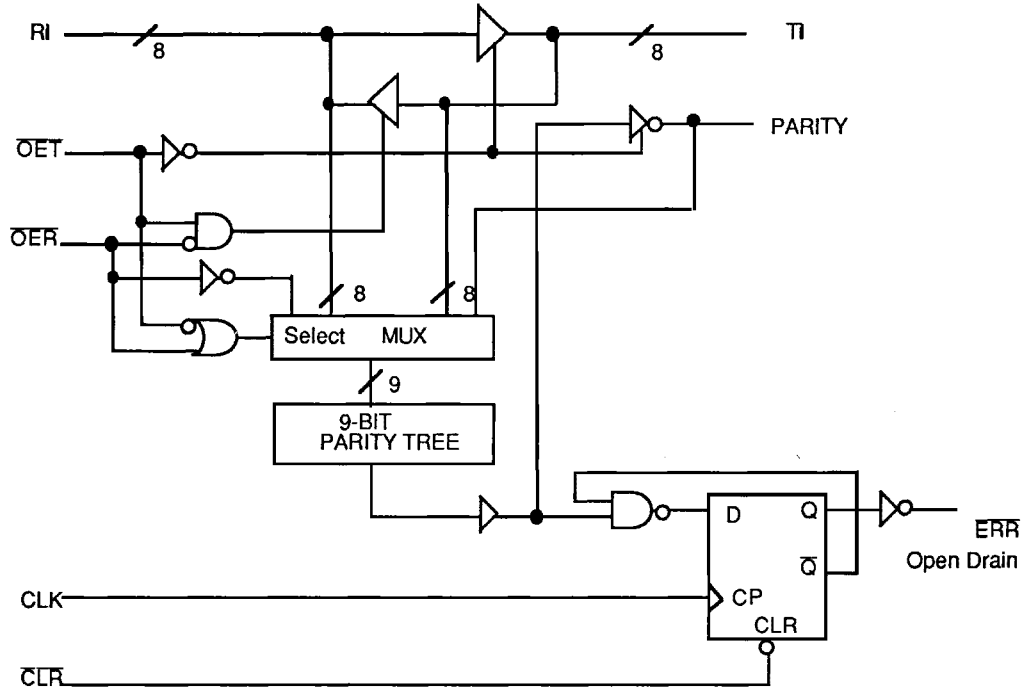
Note:  $\overline{OET}$  is HIGH and  $\overline{OER}$  is LOW

**853 ERROR FLAG OUTPUT**

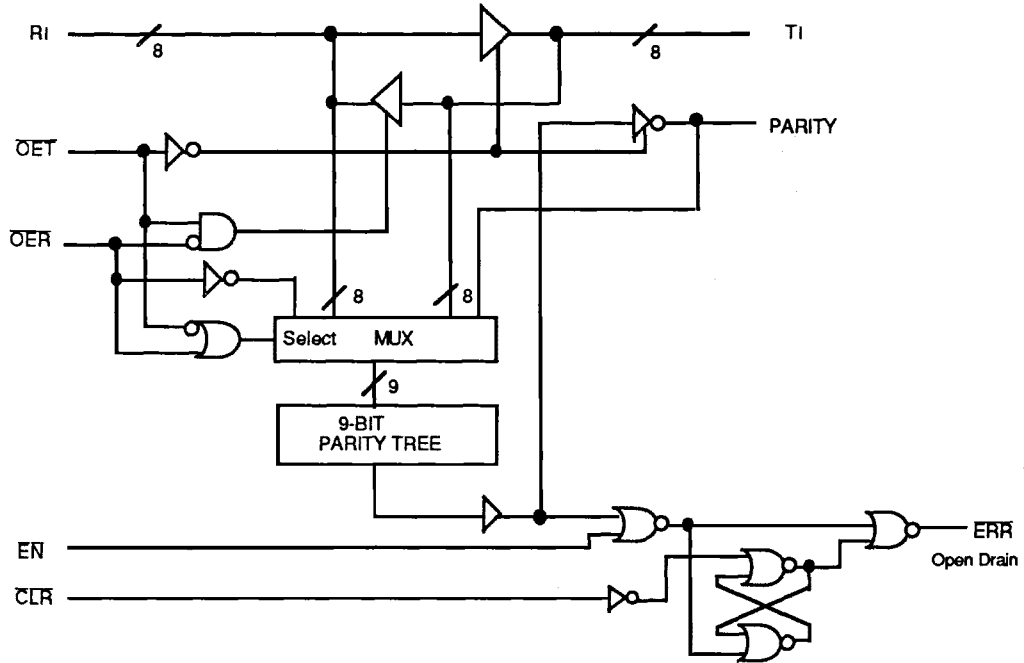
| Input |    | Internal to | Output Pre-stat | Output | Function |
|-------|----|-------------|-----------------|--------|----------|
| CLR   | EN | Point"P"    | ERR n-1         | ERR    |          |
| L     | L  | L           | X               | L      | Sample   |
| L     | L  | H           | X               | H      | Sample   |
| L     | H  | L           | X               | L      | Sample   |
| L     | L  | X           | L               | L      | Sample   |
| L     | H  | H           | H               | H      | Sample   |
| H     | L  | X           | X               | H      | Sample   |
| H     | H  | X           | L               | L      | Sample   |
| H     | H  | X           | H               | H      | Sample   |

Note:  $\overline{OET}$  is HIGH and  $\overline{OER}$  is LOW

FCT833 LOGIC DIAGRAM



**FCT853 LOGIC DIAGRAM**



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**ABSOLUTE MAXIMUM RATINGS**

- Supply Voltage to Ground..... -0.5V to +7.0V
- DC Output Voltage  $V_O$  ..... -0.5V to 7.0V
- DC Input Voltage  $V_I$  ..... -0.5V to 7.0V
- AC Input Voltage (for a pulse width  $\leq 20$  ns)..... -3.0V
- DC Input Diode Current with  $V_I < 0$ ..... -20 mA
- DC Output Diode Current with  $V_O < 0$ ..... -50 mA
- DC Output Current Max. sink current/pin..... 120 mA
- N=Number of Outputs, M=Number of inputs
- Maximum Power Dissipation.....0.5 watts
- $T_{STG}$ Storage Temperature..... -65° to +165°C

**CAPACITANCE**

$T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{in} = 0\text{V}$ ,  $V_{out} = 0\text{V}$

| Pins     | SOIC | QSOP | PDIP,LCC | ZIP | Unit |
|----------|------|------|----------|-----|------|
| ALL I/Os | 8    | 8    | 9        | 10  | pF   |

Note: Capacitance is characterized but not tested

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Commercial  $T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ,  $V_{CC}=5.0\text{V}\pm 5\%$

Military  $T_A=-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{CC}=5.0\text{V}\pm 10\%$

| Symbol                   | Parameter                                    | Test Conditions                                   |                          | Min | Typ (1) | Max  | Unit          |
|--------------------------|--|---|--------------------------|-----|---------|------|---------------|
| Vih                      | Input High Voltage                           | Logic HIGH for All Inputs                         |                          | 2.0 | -       | -    | Volts         |
| Vil                      | Input LOW Voltage                            | Logic LOW for All Inputs                          |                          | -   | -       | 0.8  |               |
| $\Delta V_t$             | Input Hysteresis                             | $V_{Ih} - V_{Il}$ for All Inputs                  |                          | -   | 0.2     | -    |               |
| $ I_{ih} $<br>$ I_{il} $ | Input Current<br>Input HIGH or LOW           | $V_{CC} = \text{MAX}$                             | $0 \leq V_{in} < V_{CC}$ | -   | -       | 5    | $\mu\text{A}$ |
| $ I_{oz} $               | Off State Output Current (Hi-Z)              | $V_{CC} = \text{MAX}, 0 \leq V_{in} \leq V_{CC}$  |                          | -   | -       | 5    |               |
| Ios                      | Short Circuit Current<br>FCTXXX              | $V_{CC} = \text{MAX}, V_o = \text{GND} (2,3)$     |                          | -60 | -       | -225 | mA            |
| Ior                      | Current Drive<br>FCT2XXX                     | $V_{CC} = \text{Min}, V_o = 2.0\text{V} (3)$      |                          | 50  | -       | -    | mA            |
| Vic                      | Input Clamp Voltage                          | $V_{CC} = \text{MIN}, I_{in} = 18 \text{ mA} (3)$ |                          | -   | -0.7    | -1.2 | Volts         |
| Voh                      | Output HIGH Voltage<br>FCTXXX & FCT2XXX      | $V_{CC} = \text{MIN}$                             | Ioh = 12 mA (MIL)        | 2.4 | -       | -    | Volts         |
|                          |  |   | Ioh = 15 mA (COM)        | 2.4 | -       | -    |               |
| Vol                      | Output LOW Voltage<br>FCTXXX                 | $V_{CC} = \text{MIN}$                             | Iol = 32 mA (MIL)        | -   | -       | 0.50 |               |
|                          |  |   | Iol = 48 mA (COM)        | -   | -       | 0.50 |               |
|                          | Output LOW Voltage<br>FCT2XXX (25 $\Omega$ ) | $V_{CC} = \text{MIN}$                             | Iol = 12 mA (MIL)        | -   | -       | 0.50 |               |
|                          |  |   | Iol = 12 mA (COM)        | -   | -       | 0.50 |               |
| Rout                     | Output Resistance<br>FCT2XXX (25 $\Omega$ )  | $V_{CC} = \text{MIN}$                             | Iol = 12 mA (MIL)        | -   | 25      | -    | $\Omega$      |
|                          |  |   | Iol = 12 mA (COM)        | 20  | 28      | 40   |               |

- Notes:**
1. Typical values indicate  $V_{CC}=5.0\text{V}$  and  $T_A=25^{\circ}\text{C}$ .
  2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
  3. These parameters are guaranteed by design but not tested.



**POWER SUPPLY CHARACTERISTICS**

| Symbol           | Parameter                           | Test Conditions (1)  | Min | Max  | Unit       |
|------------------|-------------------------------------|--|-----|------|------------|
| I <sub>cc</sub>  | Quiescent Power Supply Current      | V <sub>cc</sub> = MAX, freq = 0<br>0V ≤ V <sub>in</sub> ≤ 0.2V or V <sub>cc</sub> - 0.2V ≤ V <sub>in</sub> ≤ V <sub>cc</sub>         | -   | 1.5  | mA         |
| ΔI <sub>cc</sub> | Supply Current per Input @ TTL HIGH | V <sub>cc</sub> = MAX, V <sub>in</sub> = 3.4 V, freq = 0 (2)   | -   | 2.0  |            |
| Q <sub>ccd</sub> | Supply Current per input per MHz    | V <sub>cc</sub> = MAX, Outputs open and enabled<br>One bit toggling @ 50% duty cycle<br>Other inputs at GND or V <sub>cc</sub> (3,4) | -   | 0.25 | mA/<br>MHz |

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V<sub>i</sub>=3.4V)
3. For flipflops Q<sub>ccd</sub> is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I<sub>c</sub> can be computed using the above parameters as explained in the Technical Overview section.

**QSFCT833T, 853T, 2833T, 2853T**

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Commercial  $T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ,  $V_{CC}=5.0\text{V}\pm 5\%$  Military  $T_A=-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{CC}=5.0\text{V}\pm 10\%$   
 Load = 50 pF, Rload = 500Ω unless otherwise noted

| Symbol                             | Description                               | Notes | 833AT,853AT,<br>2833AT, 2853AT |      |      |      | 833AT,853AT,<br>2833AT, 2853AT |      |      |      | 2/833CT,<br>2/853CT |      | Unit |
|------------------------------------|---|-------|--------------------------------|------|------|------|--------------------------------|------|------|------|---------------------|------|------|
|                                    |   |       | Com                            |      | Mil  |      | Com                            |      | Mil  |      | Com                 |      |      |
|                                    |   |       | Min                            | Max  | Min  | Max  | Min                            | Max  | Min  | Max  | Min                 | Max  |      |
| t PHL<br>t PLH                     | Propagation Delay<br>Ti to /fm Ri         |       | -                              | 10   | -    | 14   | -                              | 7    | -    | 10   | -                   | 5.5  | ns   |
|                                    |   | 3     | -                              | 17.5 | -    | 21.5 | -                              | 14.5 | -    | 17.5 | -                   | 11.5 |      |
|                                    | Propagation Delay<br>Ri to PARITY         |       | -                              | 15   | -    | 20   | -                              | 10.5 | -    | 14   | -                   | 9    |      |
|                                    |   | 3     | -                              | 22.5 | -    | 27.5 | -                              | 21.5 | -    | 27.5 | -                   | 19.5 |      |
|                                    | Propagation Delay<br>CLK to ERR           |       | -                              | 12   | -    | 16   | -                              | 8.5  | -    | 11   | -                   | 7    |      |
|                                    | Propagation Delay<br>CLR to ERR           |       | -                              | 16   | -    | 20   | -                              | 15   | -    | 18   | -                   | 13   |      |
| Propagation Delay<br>OER to PARITY |   | -     | 15                             | -    | 20   | -    | 10.5                           | -    | 14   | -    | 9                   |      |      |
|                                    | 3   | -     | 22.5                           | -    | 27.5 | -    | 18                             | -    | 21.5 | -    | 15                  |      |      |
| t PZH<br>t PZL                     | Output Enable Time<br>OER, OET to Ri, Ti  |       | -                              | 12   | -    | 16   | -                              | 8.5  | -    | 11   | -                   | 8.5  |      |
|                                    |   | 3     | -                              | 19.5 | -    | 23.5 | -                              | 16   | -    | 18.5 | -                   | 16   |      |
| tPHZ<br>tPLZ                       | Output Disable Time<br>OER, OET to Ri, Ti |       | -                              | 10.7 | -    | 14.7 | -                              | 7.2  | -    | 9.8  | -                   | 7.2  |      |
|                                    |   | 3     | -                              | 12   | -    | 16   | -                              | 8.5  | -    | 11   | -                   | 8.5  |      |
| tSU                                | Ti PARITY to CLK<br>setup                 |       | 12                             | -    | 16   | -    | 8.5                            | -    | 11   | -    | 8                   | -    |      |
| tH                                 | Ti PARITY to CLK<br>Hold                  |       | 0                              | -    | 0    | -    | 0                              | -    | 0    | -    | 0                   | -    |      |
| tREM                               | CLR to CLK<br>recovery                    |       | 15                             | -    | 20   | -    | 10.5                           | -    | 14   | -    | 9                   | -    |      |
| tW                                 | Clock pulse width                         | 2     | 7                              | -    | 9.5  | -    | 5.5                            | -    | 7    | -    | 5                   | -    |      |
| tW                                 | CLR pulse width                           | 2     | 7                              | -    | 9.5  | -    | 5.5                            | -    | 7    | -    | 5                   | -    |      |

**Notes:**

- 1) See Test Circuit and Waveforms.
- 2) This parameter is guaranteed by design but not tested.
- 3) Load = 300pF