3 A, Fault Protected, Slew Rate Controlled Load Switch

DESCRIPTION

The SiP32441 is an integrated slew rate control load switch operates in the voltage range of 1.7 V to 5.5 V. The integrated charge pump drivers enable the part with low on resistance over the wide input voltage range. Its V_{IN} can tolerate over -2 V without causing damage or device malfunction.

The SiP32441 features a controlled soft-on slew rate of typical 2.5 ms that limits the inrush current for designs of heavy capacitive load and minimizes the resulting voltage droop at the power rails.

The SiP32441 integrated a special logic circuit to define the status of the power switch. This is to meet system design of both removable and embedded types.

The SiP32441 has exceptionally low shutdown current and provides reverse blocking to prevent high current flowing into the power source when the switch is off or V_{IN} is ground.

The switch blocks the current flow at both forward and reverse directions at off state. When V_{IN} and EN are OPEN, the switch will remains OFF in case voltage is applied on OUT pin.

This device is specified to operate over the industrial temperature range of -40 °C to +85 °C

FEATURES

- 1.7 V to 5.5 V input voltage range
- Negative input voltage tolerance down to -2 V
- 38 mΩ typical R_{ON} from 1.8 V to 5 V
- 3 A maximum continuous switch current
- Slew rate controlled turn-on: 2.5 ms at 3.6 V
- 2.3 V UVLO when EN is open
- Reverse current blocking when switch is off or V_{IN} is ground
- ESD protected
  - HBM: > 6 kV
  - MM: > 300 V
  - IEC61000-4-2 air discharge: > 15 kV
  - IEC61000-4-2 contact discharge: > 8 kV
- Compact TDFN4 package
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE Available

APPLICATIONS

- PDAs / smart phones
- Notebook / netbook computers
- Tablet PC
- Portable media players
- Digital camera
- GPS navigation devices
- Data storage devices
- Optical, industrial, medical, and healthcare devices

TYPICAL APPLICATION CIRCUIT

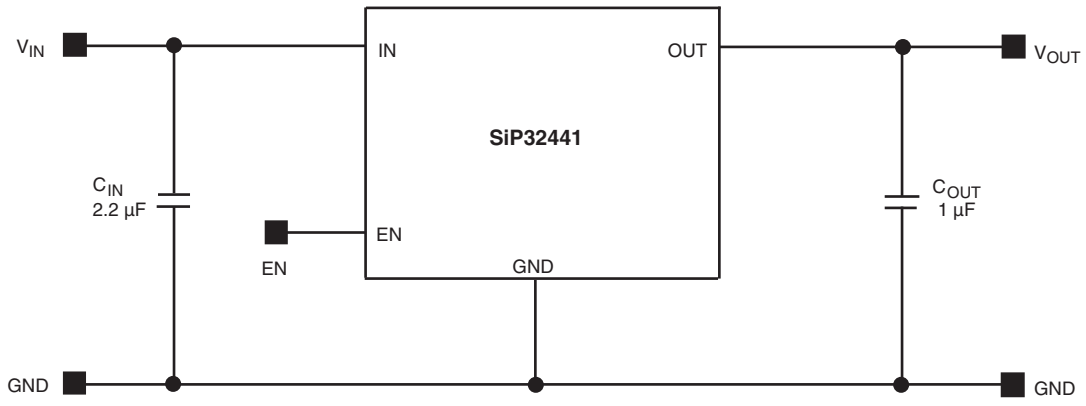


Fig. 1 - SiP32441 Typical Application Circuit

ORDERING INFORMATION

Part Number	Package	Marking	Temperature Range
SiP32441DNP-T1-GE4	TDFN4 1.2 mm x 1.6 mm	Tx	-40 °C to +85 °C

Notes
- x = Lot code
- GE4 denotes halogen-free and RoHS compliant

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Supply Input Voltage (V_{IN})		-2 to +6	V
Enable Input Voltage (V_{EN})		-2 to +6	
Output Voltage (V_{OUT})		-0.3 to +6	
Maximum Continuous Switch Current ($I_{max.}$) [c]		3.5	A
Maximum Repetitive Pulsed Current (1 ms, 10 % Duty Cycle) [c]		7	
Maximum Non-Repetitive Pulsed Current (100 µs, EN = Active) [c]		12	
Junction Temperature (T_J)		-40 to +150	°C
Thermal Resistance (q_{JA}) [a]		170	°C/W
Power Dissipation (P_D) [a,b]		735	mW
ESD Rating	HBM	6	kV
	MM	300	V
	IEC41000-4-2 Air Discharge [d]	15	kV
	IEC41000-4-2 Contact Discharge [d]	8	

Notes
a. Device mounted with all leads and power pad soldered or welded to PC board, see PCB layout.
b. Derate 5.9 mW/°C above T_A = 25 °C, see PCB layout.
c. T_A = 25 °C, see PCB layout.
d. Tested on V_{IN} with 2.2 µF C_{IN}. V_{IN} connected to micro-USB connector.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Limit	Unit
Input Voltage Range (V_{IN})	1.7 to 5.5	V
Operating Junction Temperature Range (T_J)	-40 to +125	°C

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified V_{IN} = 1.8 V to 5 V, T_A = -40 °C to +85 °C (typical values are at T_A = 25 °C)	Limits -40 °C to +85 °C			Unit
			Min. [a]	Typ. [b]	Max. [a]	
Operating Voltage	V_{IN}		1.8	-	5.5	V
Negative Input Voltage Tolerance	I_{NEG}	V_{IN} = -2 V	-	-15	-	mA
Under Voltage Lock Out	$UVLO_{H-L}$	EN = open, 25 °C (switch On to Off)	-	-	2	V
	$UVLO_{L-H}$	EN = open, 25 °C (switch Off to On)	2.5	2.3	-	
UVLO Hysteresis	$UVLO_{HYS}$	EN = open, 25 °C	-	0.25	-	
Quiescent Current	I_Q	V_{IN} = 1.8 V, EN = active	-	38	50	µA
		V_{IN} = 2.5 V	-	58	70 [d]	
		V_{IN} = 3.6 V	-	82	100 [d]	
		V_{IN} = 4.3 V	-	101	120 [d]	
		V_{IN} = 5 V	-	119	150	
Off Supply Current	$I_{Q(off)}$	V_{IN} = 2 V, V_{EN} = 0 V, OUT = open	-	6.3	10	
Off Switch Current	$I_{DS(off)}$	V_{IN} = 2 V, V_{EN} = 0 V, V_{OUT} = 0 V	-	-	1	
Reverse Blocking Current	I_{RB}	V_{OUT} = 5 V, V_{IN} = 0 V, V_{EN} = 0 V or open	-	-	10	
On-Resistance	$R_{DS(on)}$	V_{IN} = 1.8 V, I_L = 500 mA, T_A = 25 °C	-	38	43	mΩ
		V_{IN} = 2.5 V, I_L = 500 mA, T_A = 25 °C	-	38	43	
		V_{IN} = 3.6 V, I_L = 500 mA, T_A = 25 °C	-	38	43	
		V_{IN} = 4.3 V, I_L = 500 mA, T_A = 25 °C	-	38	43	
		V_{IN} = 5 V, I_L = 500 mA, T_A = 25 °C	-	38	43	
Input Logic Low [c]	V_{IL}	V_{IN} = 1.8 V	-	-	0.5	V
		V_{IN} = 2.5 V	-	-	0.7 [d]	
		V_{IN} = 3.6 V	-	-	1.1 [d]	
		V_{IN} = 4.3 V	-	-	1.3 [d]	
		V_{IN} = 5 V	-	-	1.5 [d]	
Input Logic High [c]	V_{IH}	V_{IN} = 1.8 V	1.3	-	-	
		V_{IN} = 2.5 V	1.6 [d]	-	-	
		V_{IN} = 3.6 V	1.9 [d]	-	-	
		V_{IN} = 4.3 V	2.1 [d]	-	-	
		V_{IN} = 5 V	2.4 [d]	-	-	
Enable Pin Bias Current	I_{EN}	V_{EN} = 5 V	-	5.4	7	µA
Output Turn-On Delay Time	$t_{d(on)}$	V_{IN} = 3.6 V, R_{load} = 10 Ω, C_L = 0.1 µF, T_A = 25 °C	-	1.3	-	ms
Output Turn-On Rise Time	$t_{(on)}$		-	1.8	2.5	
Output Turn-Off Delay Time	$t_{d(off)}$		-	0.0002	-	

Notes

a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. For V_{IN} outside this range consult typical EN threshold curve.
d. Not tested, guarantee by design.

PIN CONFIGURATION

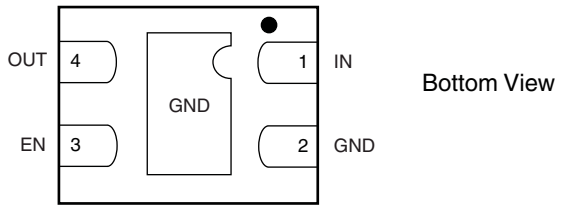


Fig. 2 - TDFN4 1.2 mm x 1.6 mm Package

PIN DESCRIPTION		
Pin Number	**Name**	**Function**
1	IN	This is the input pin of the switch
2	GND	Ground connection
3	EN	Enable input
4	OUT	This is the output pin of the switch

BLOCK DIAGRAM

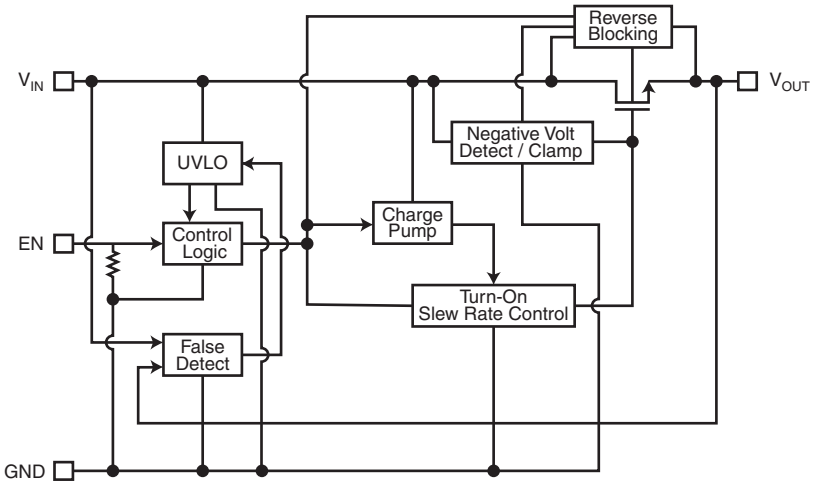


Fig. 3 - Functional Block Diagram

TRUTH TABLE				
IN		**OUT**	**EN**	**SWITCH**
L		X	X	OFF
H	> UVLO	⎍	X	ON
	> 1.5 < UVLO		H	ON
			L	OFF
L		⎍	X	OFF
⎍		H	H	ON
⎍		H	L	OFF
⎎		H	(1)	ON

Notes

(1) It will be depending on the status of latch of the OR gate output. If latch is at high, then EN cannot off the switch. If latch is low, then EN can off the switch.

- IN has UVLO. High at IN column means a voltage source is applied to IN, that is high enough to power the logic circuit but could be lower than the UVLO threshold.
- EN pin has a pull down of ~1 MΩ.
- UVLO threshold is about 2.3 V.

DETAILED DESCRIPTION

SiP32441 is an advanced slew rate controlled high side load switch with an integrated N-channel power switch. When the device is on the gate of the power switch is turned on at a controlled rate to avoid excessive inrush current. Once fully on the gate to source voltage of the power switch is biased at a constant level. The design gives a flat on resistance throughout the operating voltages. A special reverse blocking circuitry prevents current flowing from output to input when the switch is off. The V_{IN} and EN pin can tolerate -2 V voltage without drawing excessive current. The device is turn-on after the UVLO voltage regardless the condition of the EN pin. A fault protection circuitry is incorporated to define the status of the switch. Its states are described in the truth table.

APPLICATION INFORMATION

Input Capacitor

In general, under steady state conditions the SiP32441 does not require an input capacitor. Nevertheless, an input bypass capacitor is recommended in order to reduce the input voltage drop caused by transient inrush currents. Commonly, a 2.2 µF ceramic capacitor is sufficient and should be placed in close proximity to V_{IN} and GND pins. A higher value input capacitor can help to further reduce the voltage drop. Ceramic capacitors are recommended for their low ESR characteristic.

Output Capacitor

While these devices work without an output capacitor, a 1 µF or higher value capacitor across V_{OUT} and GND is recommended in order to handle potential load transient conditions. In the event that the switch is turning of while running high current, circuit stray inductances might force the output to some negative voltage in order to mitigate this phenomenon a proper output capacitor is required.

Enable

The device is logic high active, the enable pin voltage can exceed V_{IN} as long as it is within the absolute maximum rating range.

If the input voltage is available before output voltage and either input or output voltage is above input UVLO threshold, the switch is on regardless of the enable pin voltage even if the input pin is left open later. In this case, the enable pin cannot be used to turn off the switch except in the certain fault conditions as described by the truth table.

If the input voltage is available before output voltage and both the input voltage and output voltage are lower than the input UVLO threshold and above 1.5 V, the enable pin can be used to turn on and off the switch even if either input pin or output pin is left open later.

If the output voltage is available before the input voltage, the enable pin can be used to turn on/off the switch.

Reverse Voltage Protection

The SiP32441 contains a reverse blocking circuitry to protect the current from going to the input from the output when the switch is off. Reverse blocking works for input voltage as low as 0 V.

THERMAL CONSIDERATIONS

The maximum allowed DC Current depends on the thermal condition in which the device operates. In order to calculate max allowed DC current, first the max power dissipation should be considered.

The SiP32441 is packaged in a TDFN4 1.2 mm x 1.6 mm package which has a thermal resistance of $\theta_{J\text{-}A}$ [a] = 170 °C/W.

Note

a. Device mounted with all leads and power pad soldered or welded to PC board, see PCB layout. For any other layout configuration the actual junction to ambient thermal impedance should be considered

The following formula shows the maximum allowed power dissipation as a function of the ambient temperature T_A when the maximum junction temperature is limited to $T_{J\ (max.)}$ = 125 °C:

$$P_{max.} = \frac{T_J(max.) - T_A}{\theta_{J\text{-}A}} = \frac{125 - T_A}{170}$$

For example at ambient temperature of 70 °C, the maximum power dissipation will be limited to about 324 mW.

In order to calculate the maximum allowed DC current the switch $R_{DS(on)}$ temperature dependency should be considered.

As an example let us calculate maximum load current at T_A = 70 °C and input voltage of 1.8 V. At this input voltage the $R_{DS(on)}$ at 25 °C 43 mΩ (see specification table). The $R_{DS(on)}$ at 125 °C can be extrapolated from this data using the following formula:

$$R_{DS(on)\_125\ °C} = R_{DS(on)\_25\ °C} \times (1 + T_C \times (T_{J\ max.} - 25)/100)$$

Where T_C is the $R_{DS(on)}$ temperature coefficient expressed in percent change per ° C.

For SiP32441 the approximated value is 0.31 %/°C. $T_{J\ max.}$ is the maximum allowed junction temperature (125 °C).

Therefore,

$$R_{DS(on)\ (at\ 125\ °C)} = 43\ m\Omega \times (1 + 0.31 \times (125 - 25)/100) \approx 57\ m\Omega$$

The maximum current limit is then determined by

$$I_{LOAD}\ (max.) < \sqrt{\frac{P\ (max.)}{R_{DS(on)}}}$$

Which in this case is 2.38 A.

Due to device limitation the max switch DC current should not exceed 3 A in any condition.

To obtain the highest power dissipation the power pad of the device should be connected to a heat sink on the printed circuit board. Fig. 4 shows a typical PCB layout. All copper traces and vias for the V_{IN} and V_{OUT} pins should be sized adequately to carry the maximum continuous current.

Negative Input Voltage

The SiP32441 can withstand maximum negative 2 V at its input due to any spike from abnormal or fault condition of the system.

Recommended Board Layout

For improved performance, all traces should be as short as possible to minimize stray inductances and parasitic effects. The input and output capacitors should be kept as close as possible to the input and output pins respectively. Connecting the central exposed pad to GND, using wide traces for input, output, and GND help reducing the case to ambient thermal impedance. See fig. 4.

BOARD LAYOUT

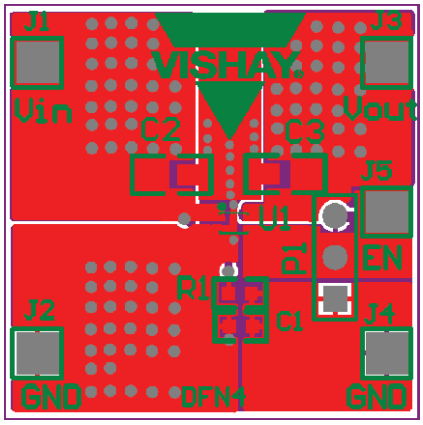


Fig. 4 - Recommended Board Layout

TYPICAL APPLICATION SCHEMATIC

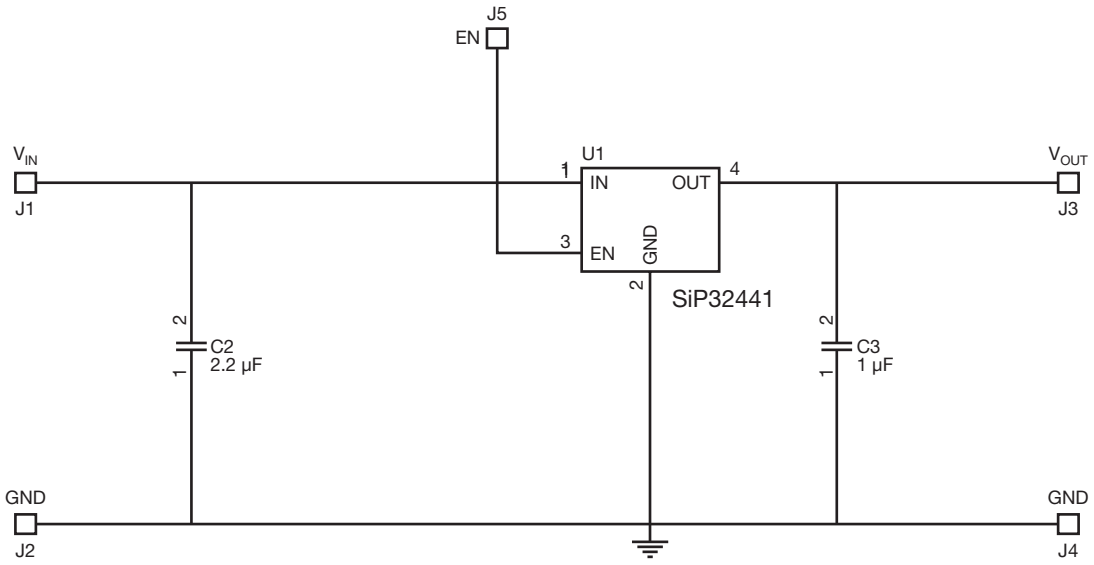
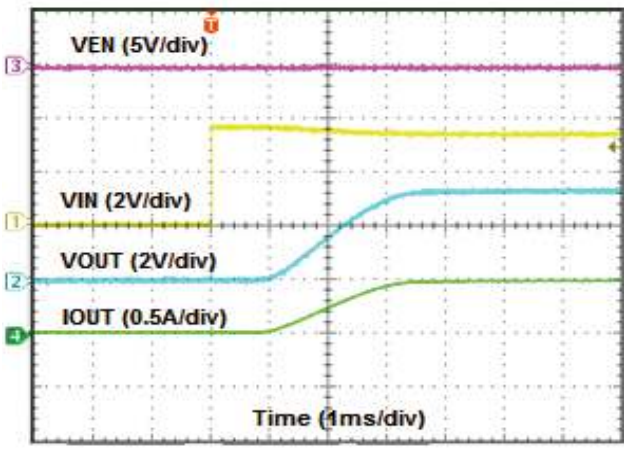
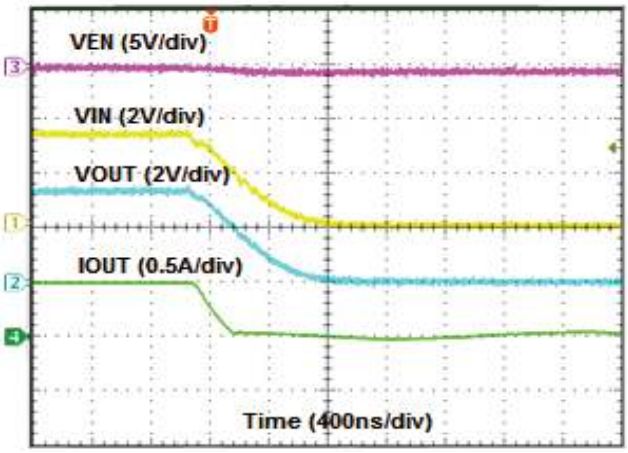


Fig. 5 - Application Schematic

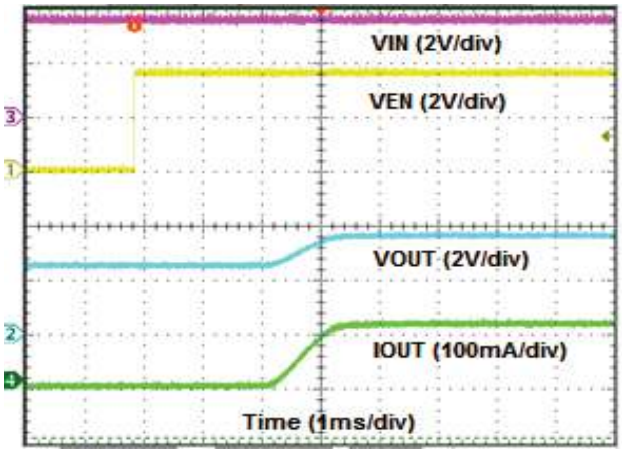
TYPICAL TURN-ON AND TURN-OFF WAVEFORMS



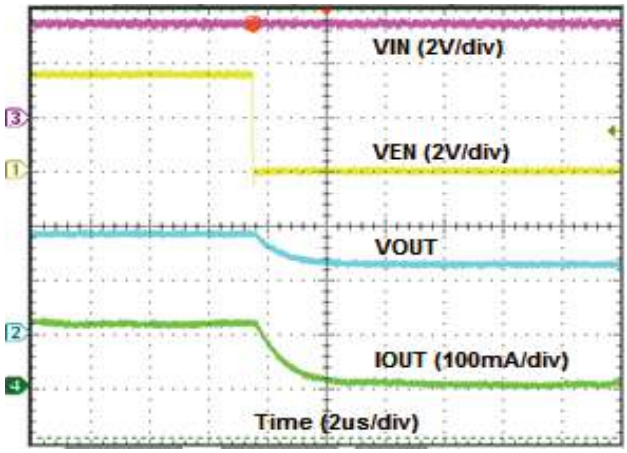
Turn-On Time
V_{IN} = 0 V to 3.6 V, R_L = 7.2 Ω, C_L = 0.1 µF



Turn-Off Time
V_{IN} = 3.6 V to 0 V, R_L = 7.2 Ω, C_L = 0.1 µF



Turn-On Time
V_{IN} = 3.6 V, R_L = 10 Ω between OUT and 2.5 V, C_L = 0.1 µF



Turn-Off Time
V_{IN} = 3.6 V, R_L = 10 Ω between OUT and 2.5 V, C_L = 0.1 µF

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

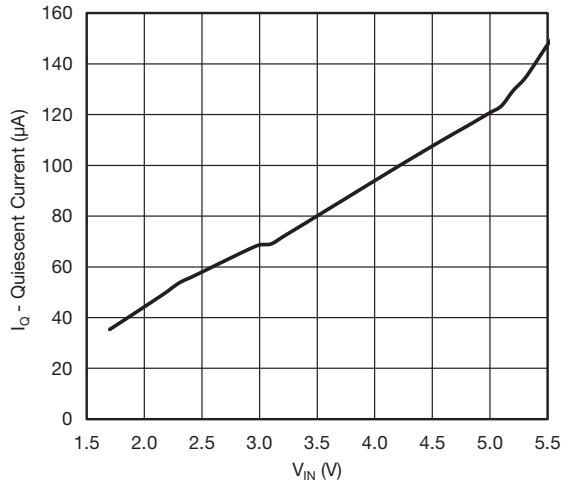


Fig. 6 - Quiescent Current vs. Input Voltage

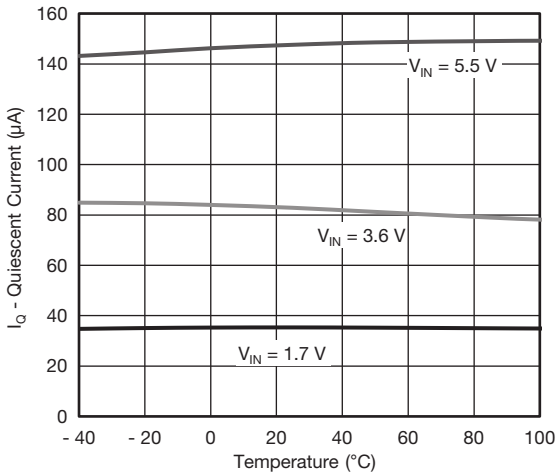


Fig. 9 - Quiescent Current vs. Temperature

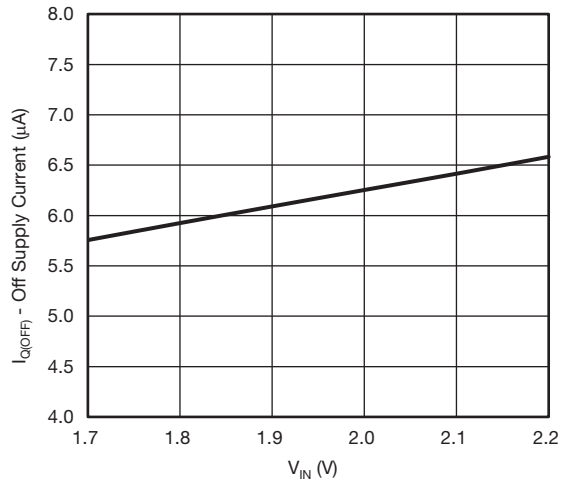


Fig. 7 - Off Supply Current vs. Input Voltage

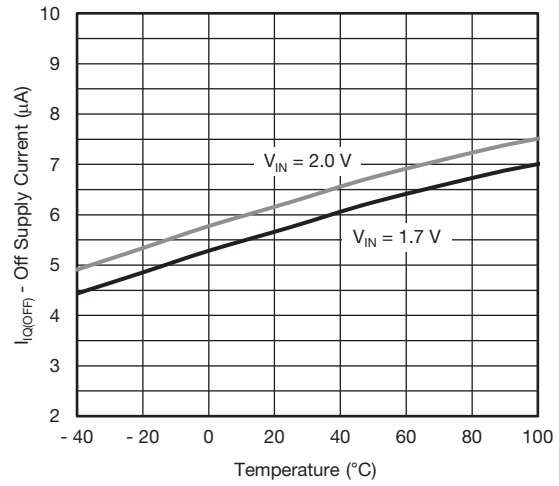


Fig. 10 - Off Supply Current vs. Temperature

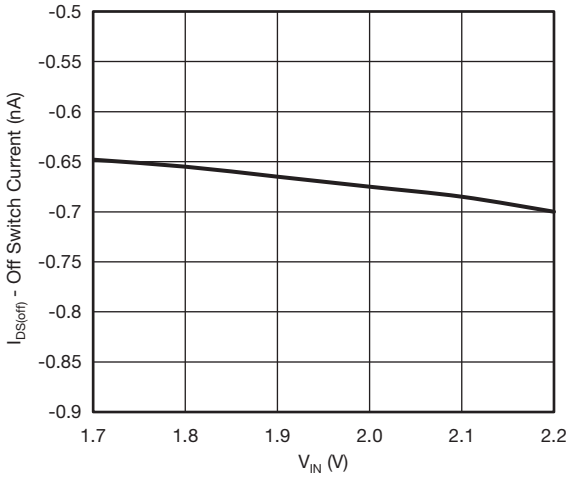


Fig. 8 - Off Switch Current vs. Input Voltage

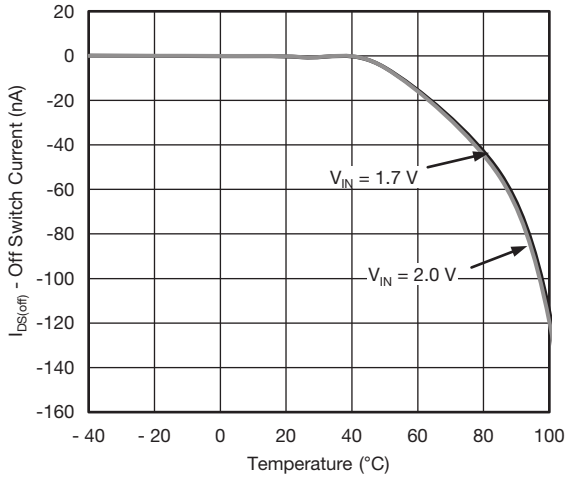


Fig. 11 - Off Switch Current vs. Temperature

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

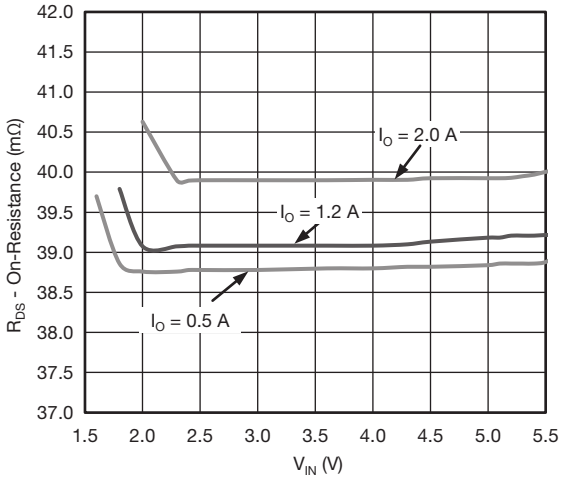


Fig. 12 - On-Resistance vs. Input Voltage

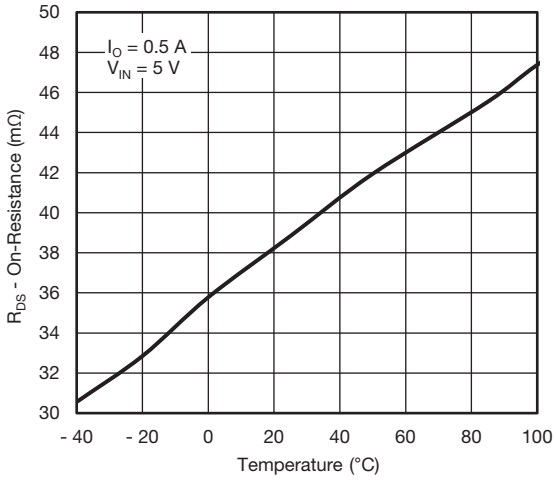


Fig. 15 - On-Resistance vs. Temperature

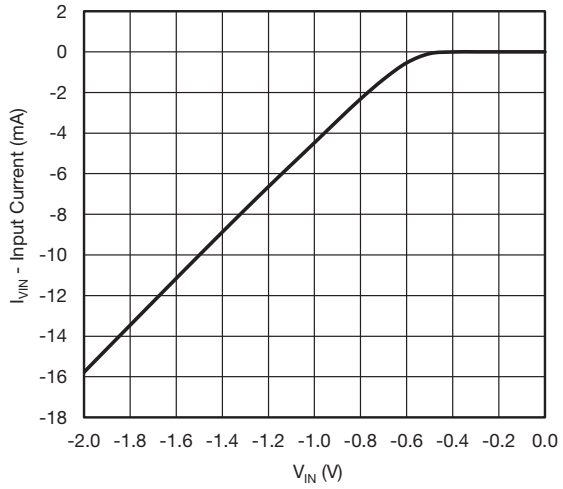


Fig. 13 - Input Current vs. Negative Input Voltage

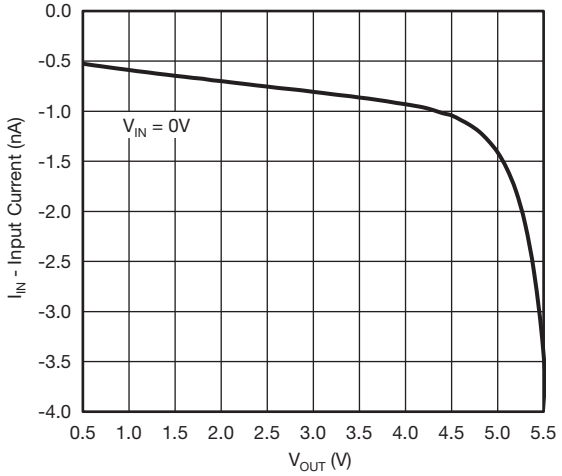


Fig. 16 - Reverse Blocking Current vs. Output Voltage

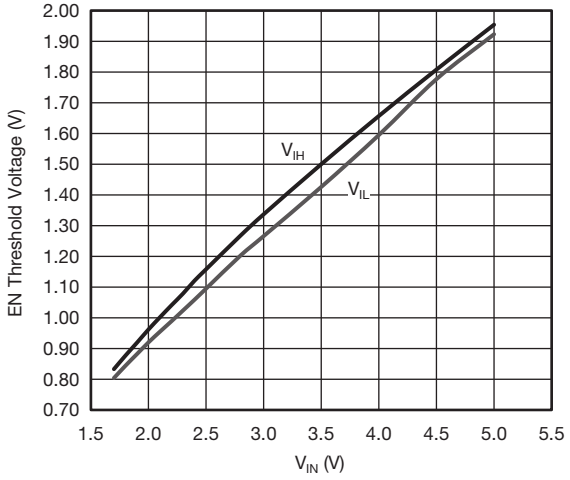


Fig. 14 - Threshold Voltage vs. Input Voltage

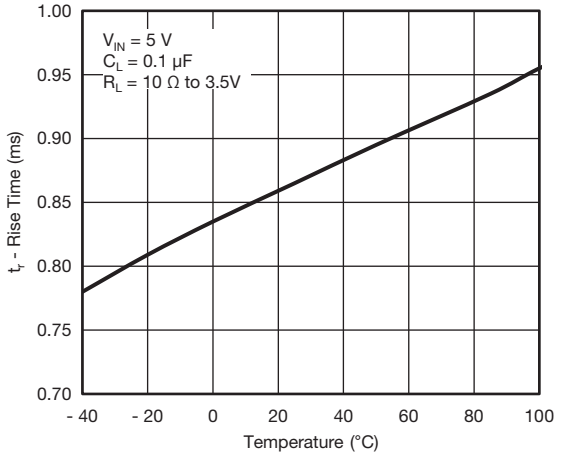


Fig. 17 - Rise Time vs. Temperature

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

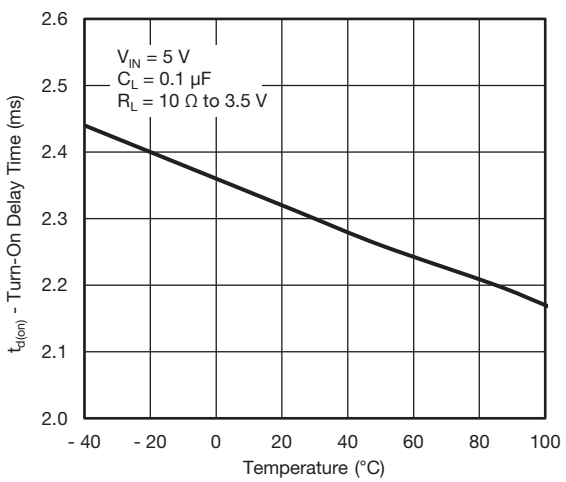


Fig. 18 - Turn-On Delay Time vs. Temperature

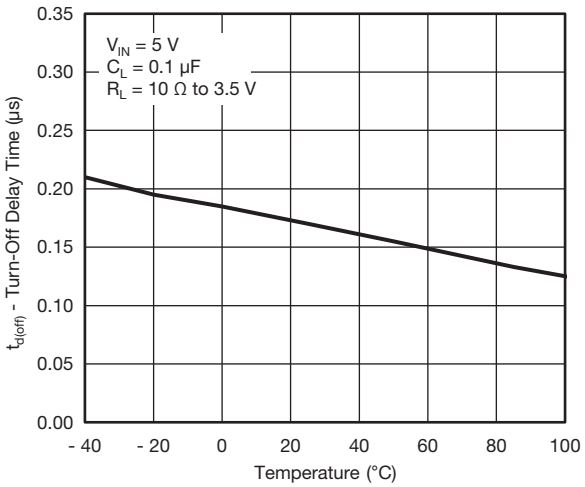


Fig. 19 - Turn-Off Delay Time vs. Temperature

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