Bus-Polarity Correcting RS-485 Transceiver for E-Meters

Check for Samples: SN888C

FEATURES

- **Exceeds Requirements of EIA-485 Standard**
- **Bus-Polarity Correction within 76 ms**
- **Data Rate: 300 bps to 250 kbps**
- **Works with Two Configurations:**
  - **Failsafe Resistors Only**
  - **Failsafe and Termination Resistors**
- **Up to 256 Nodes on a Bus**
- **SOIC-8 Package for Backward Compatibility**
- **Bus-Pin Protection:**
  - **±16 kV HBM protection**
  - **±12 kV IEC61000-4-2 Contact Discharge**
  - **+4 kV IEC61000-4-4 Fast Transient Burst**

APPLICATIONS

- **E-meters**

DESCRIPTION

The SN888C is a low-power RS-485 transceiver with bus-polarity correction and transient protection. Upon hot plug-in the device detects and corrects the bus polarity within the first 76 ms of bus idling. On-chip transient protection protects the device against IEC61000 ESD and EFT transients.

The SN888C is available in an SOIC-8 package. The device is characterized from –40°C to 85°C.

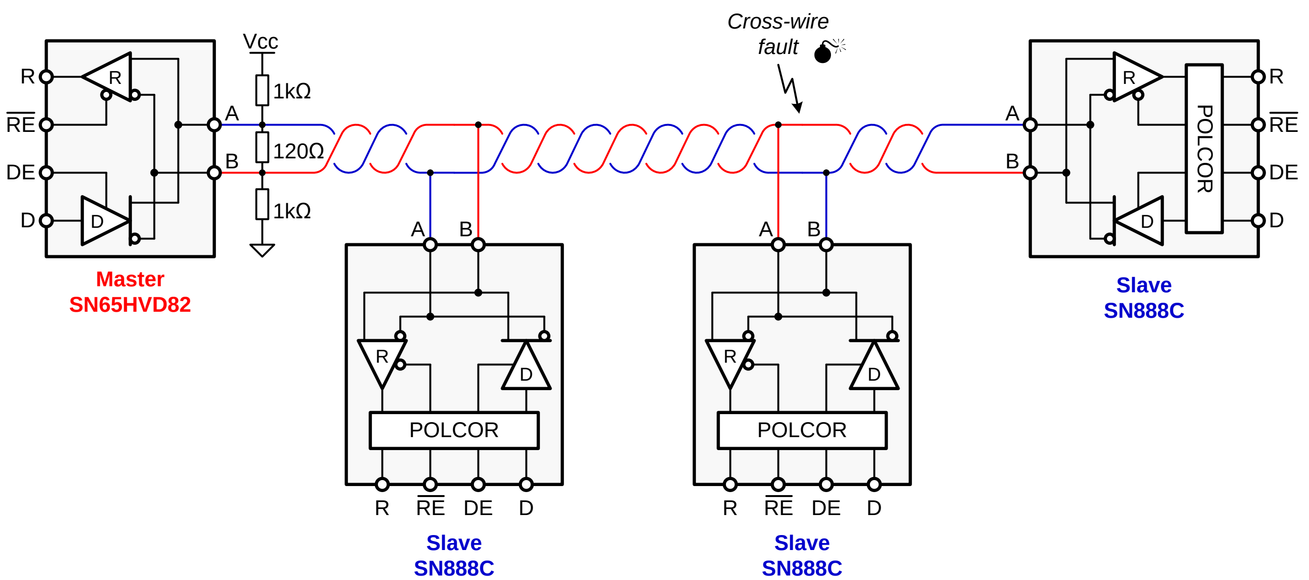
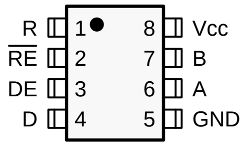


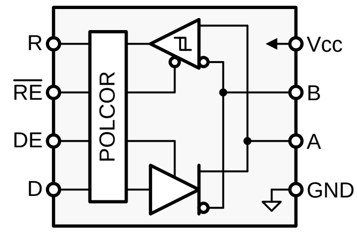
Figure 1. Typical Network Application With Polarity Correction (POLCOR)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SOIC-8
(TOP VIEW)



Block Diagram



DRIVER PIN FUNCTIONS

INPUT	ENABLE	OUTPUTS		DESCRIPTION
D	DE	A	B	
NORMAL MODE				
H	H	H	L	Actively drives bus high
L	H	L	H	Actively drives bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drives bus high
POLARITY-CORRECTING MODE(1)				
H	H	L	H	Actively drives bus low
L	H	H	L	Actively drives bus high
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	L	H	Actively drives bus low

(1) The polarity-correcting mode is entered when $V_{ID} < V_{IT-}$ and $t > t_{FS}$ and DE = low. This state is latched when /RE turns from low to high.

RECEIVER PIN FUNCTIONS

DIFFERENTIAL INPUT	ENABLE	OUTPUT	DESCRIPTION
$V_{ID} = V_A – V_B$	/RE	R	
NORMAL MODE			
$V_{IT+} < V_{ID}$	L	H	Receive valid bus high
$V_{IT–} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT–}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled
Open, short, idle bus	L	?	Indeterminate bus state
POLARITY-CORRECTING MODE(1)			
$V_{IT+} < V_{ID}$	L	L	Receive valid bus low
$V_{IT–} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT–}$	L	H	Receive polarity corrected bus high
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled
Open, short, idle bus	L	?	Indeterminate bus state

(1) The polarity-correcting mode is entered when $V_{ID} < V_{IT-}$ and $t > t_{FS}$ and DE = low. This state is latched when /RE turns from low to high.

ABSOLUTE MAXIMUM RATINGS(1)

			VALUE MIN	VALUE MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
	Input voltage range at any logic pin		–0.3	5.7	V
	Voltage input range, transient pulse, A and B, through 100 Ω		–100	100	V
	Voltage range at A or B inputs		–18	18	V
	Receiver output current		–24	24	mA
	Continuous total-power dissipation		See THERMAL INFORMATION table		
	IEC 61000-4-2 ESD (Contact Discharge), bus terminals and GND			±12	kV
	IEC 61000-4-4 EFT (Fast transient or burst) bus terminals and GND			±4	kV
	IEC 60749-26 ESD (HBM), bus terminals and GND			±16	kV
	JEDEC Standard 22	Test Method A114 (HBM), all pins		±8	kV
	JEDEC Standard 22	Test Method C101 (Charged Device Model), all pins		±1.5	kV
	JEDEC Standard 22	Test Method A115 (Machine Model), all pins		±200	V
T_J	Junction temperature			170	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		SN888C PACKAGE SOIC (D)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	116.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	60.8	°C/W
θ_{JB}	Junction-to-board thermal resistance(2)	57.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.5	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

POWER DISSIPATION

PARAMETER			TEST CONDITIONS	VALUE	UNITS
PD	Power dissipation Driver and receiver enabled, V_{CC} = 5.5 V, T_J = 150°C 50% duty cycle square-wave signal at 250-kbps signaling rate:	Unterminated	R_L = 300 Ω, C_L = 50 pF (driver)	164	mW
		RS-422 load	R_L = 100 Ω, C_L = 50 pF (driver)	247	mW
		RS-485 load	R_L = 54 Ω, C_L = 50 pF (driver)	316	mW

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{ID}	Differential input voltage		–12		12	V
V_I	Input voltage at any bus terminal (separate or common mode)[1]		–7		12	V
V_{IH}	High-level input voltage (driver, driver-enable, and receiver-enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver-enable, and receiver-enable inputs)		0		0.8	V
I_O	Output current	Driver	–60		60	mA
		Receiver	–8		8	mA
C_L	Differential load capacitance			50		pF
R_L	Differential load resistance			60		Ω
$1/t_{UI}$	Signaling rate		0.3		250	kbps
T_J	Junction temperature		–40		150	°C
T_A[2]	Operating free-air temperature (see THERMAL INFORMATION for additional information)		–40		85	°C

(1) The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver outputs when the junction temperature reaches 170°C.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential-output voltage magnitude	RL = 60 Ω, 375 Ω on each output from –7 to +12 V	See Figure 2	1.5	2.5		V
		RL = 54 Ω (RS-485)	See Figure 3	1.5	2.5		V
		RL = 100 Ω (RS-422)	See Figure 3	2	3		V
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential-output voltage	RL = 54 Ω, CL = 50 pF	See Figure 3	–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27-Ω load resistors	See Figure 3	1	V_{CC} / 2	3	V
ΔV_{OC}	Change in differential driver common-mode output voltage	Center of two 27-Ω load resistors	See Figure 3	–0.2	0	0.2	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors	See Figure 3		850		mV
C_{OD}	Differential output capacitance				8		pF
V_{IT+}	Positive-going receiver differential-input voltage threshold				35	100	mV
V_{IT-}	Negative-going receiver differential-input voltage threshold			–100	–35		mV
V_{HYS}[1]	Receiver differential-input voltage threshold hysteresis ($V_{IT+} - V_{IT-}$)			40	60		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA		2.4	V_{CC} – 0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA			0.2	0.4	V
I_I	Driver input, driver enable, and receiver enable input current			–2		2	µA

(1) Under any specific conditions, V_{IT+} is ensured to be at least V_{HYS} higher than V_{IT-}.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OZ}	Receiver high-impedance output current	VO = 0 V or VCC, /RE at VCC		–10		10	μA
$\lvert I_{OS} \rvert$	Driver short-circuit output current	$\lvert I_{OS} \rvert$ with V_A or V_B from –7 to +12 V				150	mA
I_I	Bus input current (driver disabled)	V_{CC} = 4.5 to 5.5 V or	V_I = 12 V		75	125	μA
		V_{CC} = 0 V, DE at 0 V	V_I = –7 V	–100	–40		
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V_{CC}, /RE = GND, No load		750	900	μA
		Driver enabled, receiver disabled	DE = V_{CC}, /RE = V_{CC}, No load			650	
		Driver disabled, receiver enabled	DE = GND, /RE = GND, No load			750	
		Driver and receiver disabled	DE = GND, D = GND /RE = VCC, No load		0.4	5	
	Supply current (dynamic)	See					

SWITCHING CHARACTERISTICS

3.3 ms > bit time > 4 μs (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential-output rise and fall times	RL = 54 Ω, CL = 50 pF	See Figure 4	400	700	1200	ns
t_{PHL}, t_{PLH}	Driver propagation delay			90	700	1000	
$t_{SK(P)}$	Driver pulse skew, $\lvert t_{PHL} – t_{PLH} \rvert$				25	200	
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 5 and Figure 6		50	500	ns
t_{PHZ}, t_{PLZ}	Driver enable time	Receiver enabled			500	1000	
		Receiver disabled			3	9	μs
RECEIVER							
t_r, t_f	Receiver output rise and fall times	CL = 15 pF	See Figure 7		18	30	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				85	195	
$t_{SK(P)}$	Receiver pulse skew, $\lvert t_{PHL} – t_{PLH} \rvert$				1	15	
t_{PHZ}, t_{PLZ}	Receiver disable time				50	500	
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See Figure 8		20	130	ns
		Driver disabled	See Figure 9		2	8	μs
t_{FS}	Bus failsafe time	Driver disabled	See Figure 10	44	58	76	ms

PARAMETER MEASUREMENT INFORMATION

DRIVER

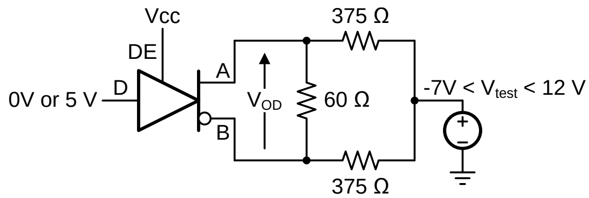


Figure 2. Measurement of Driver Differential-Output Voltage With Common-Mode Load

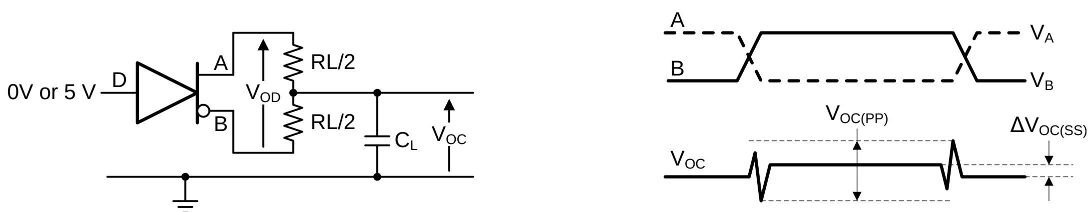


Figure 3. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

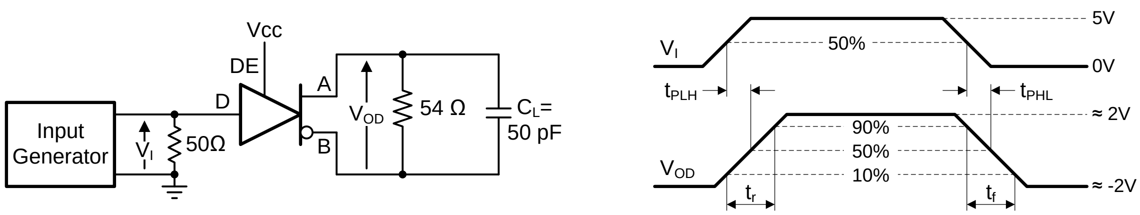


Figure 4. Measurement of Driver Differential-Output Rise and Fall Times and Propagation Delays

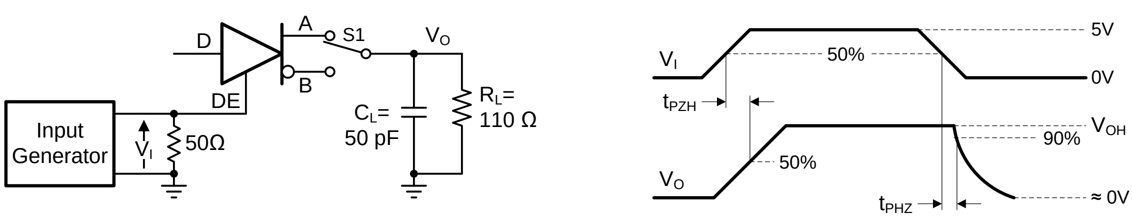


Figure 5. Measurement of Driver Enable and Disable Times With Active-High Output and Pull-Down Load

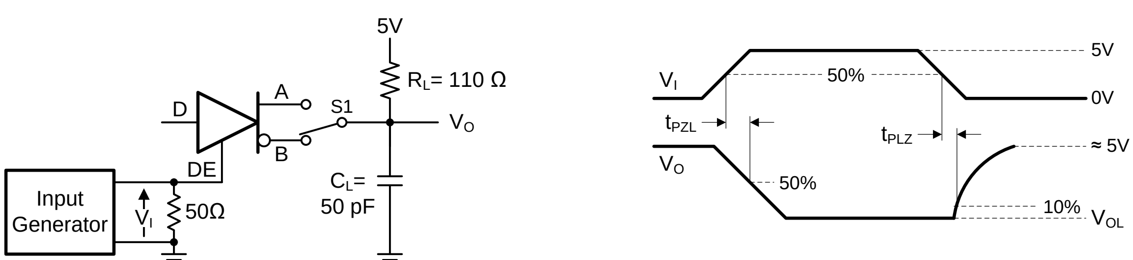


Figure 6. Measurement of Driver Enable and Disable Times With Active-Low Output and Pull-Up Load

PARAMETER MEASUREMENT INFORMATION (continued)

RECEIVER

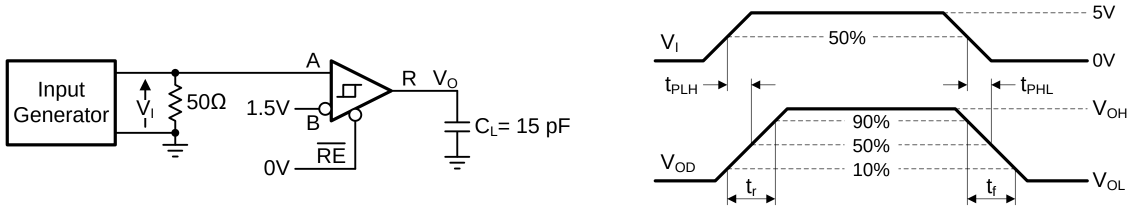


Figure 7. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

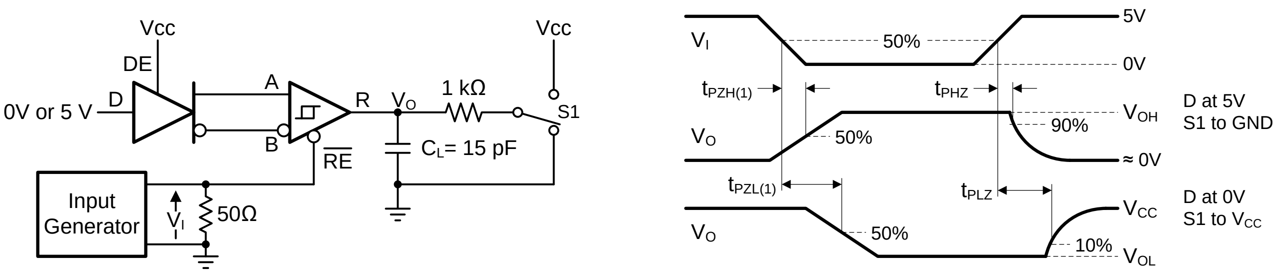


Figure 8. Measurement of Receiver Enable and Disable Times With Driver Enabled

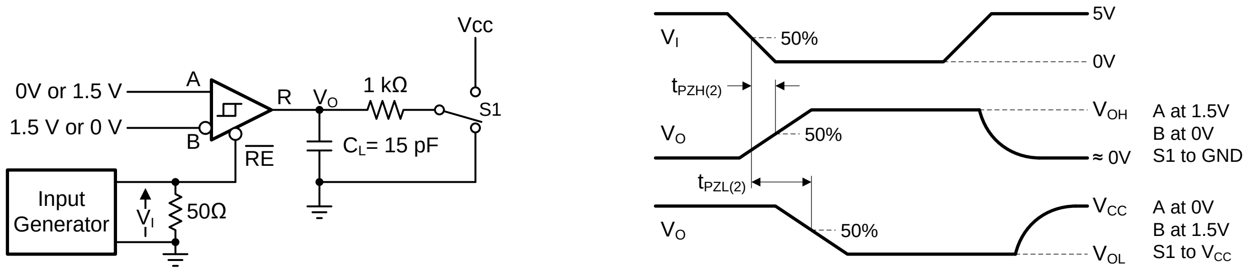


Figure 9. Measurement of Receiver Enable Times With Driver Disabled

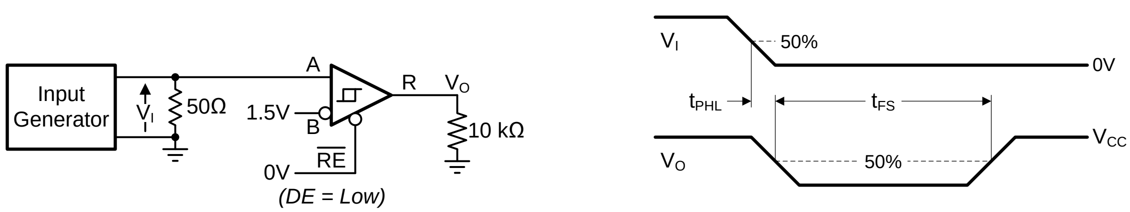
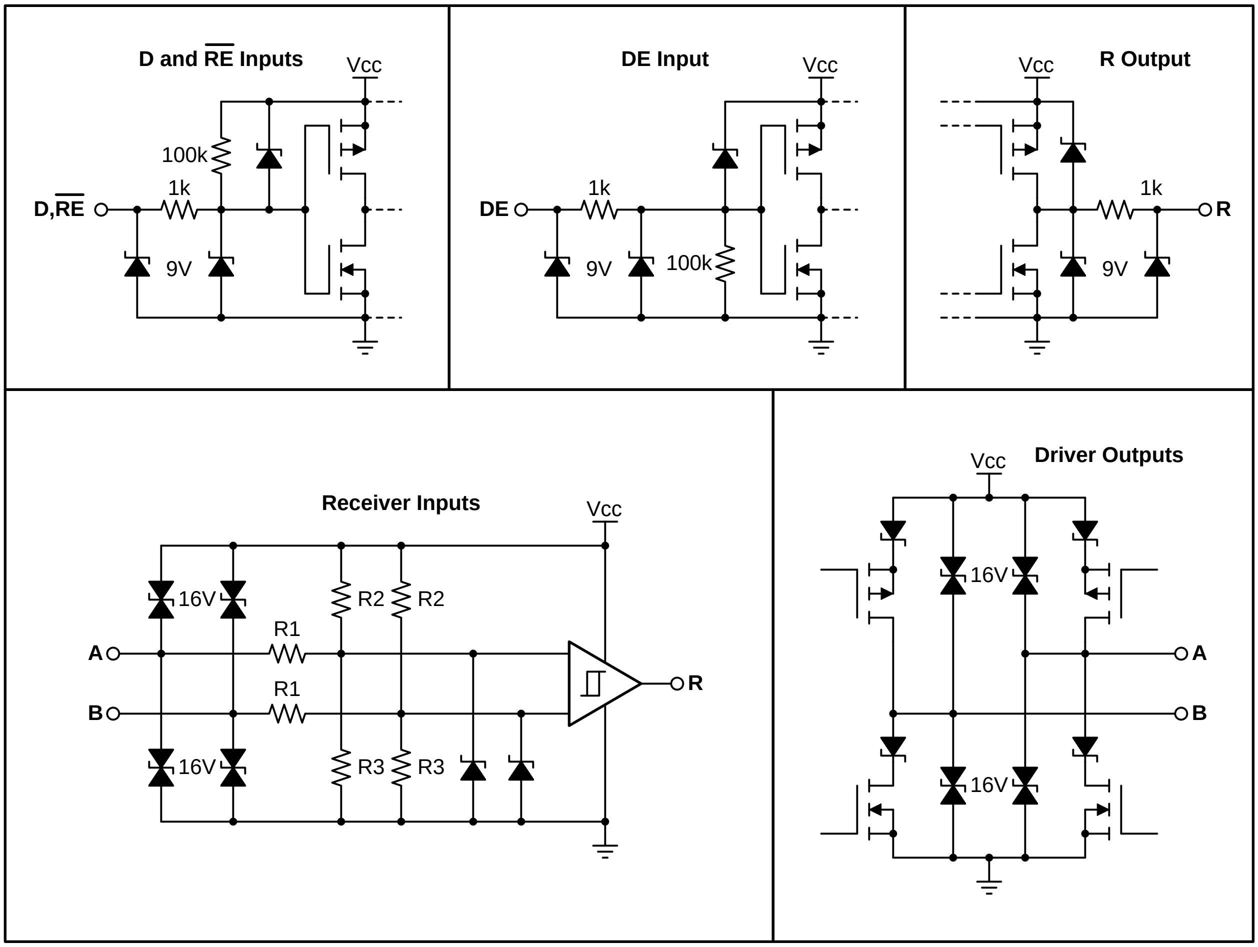


Figure 10. Measurement of Receiver Polarity-Correction Time With Driver Disabled

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



DEVICE INFORMATION

Low-Power Standby Mode

When the driver and the receiver are both disabled (DE = low and RE = high) the device enters standby mode. If the enable inputs are in the disabled state for only a brief time (for example: less than 100 ns), the device does not enter standby mode, preventing the SN888C device from entering standby mode during driver or receiver enabling. Only when the enable inputs are held in the disabled state for a duration of 300 ns or more does the device enter low-power standby mode. In this mode most internal circuitry is powered down, and the steady-state supply current is typically less than 400 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active. During V_{CC} power-up, when the device is set for both driver and receiver disabled mode, the device may consume more than 5-µA of ICC disabled current because of capacitance charging effects. This condition occurs only during V_{CC} power-up.

Bus Polarity Correction

The SN888C device automatically corrects a wrong bus-signal polarity caused by a cross-wire fault. In order to detect the bus polarity, all three of the following conditions must be met:

- A failsafe-biasing network (commonly at the master node) must define the signal polarity of the bus.
- A slave node must enable the receiver and disable the driver (/RE = DE = low).
- The bus must idle for the failsafe time, $t_{FS\text{-}max}$.

After the failsafe time has passed, the polarity correction is complete and applied to both the receive and transmit channels. The status of the bus polarity latches within the transceiver and maintains for subsequent data transmissions.

NOTE

Avoid data string durations of consecutive 0s or 1s exceeding $t_{FS\text{-}min}$, which can accidently trigger a wrong polarity correction.

Figure 11 shows a simple point-to-point data link between a master node and a slave node. Because the master node with the failsafe biasing network determines the signal polarity on the bus, an RS-485 transceiver without polarity correction, such as SN65HVD82, suffices. All other bus nodes, typically performing as slaves, require the SN888C transceiver with polarity correction.

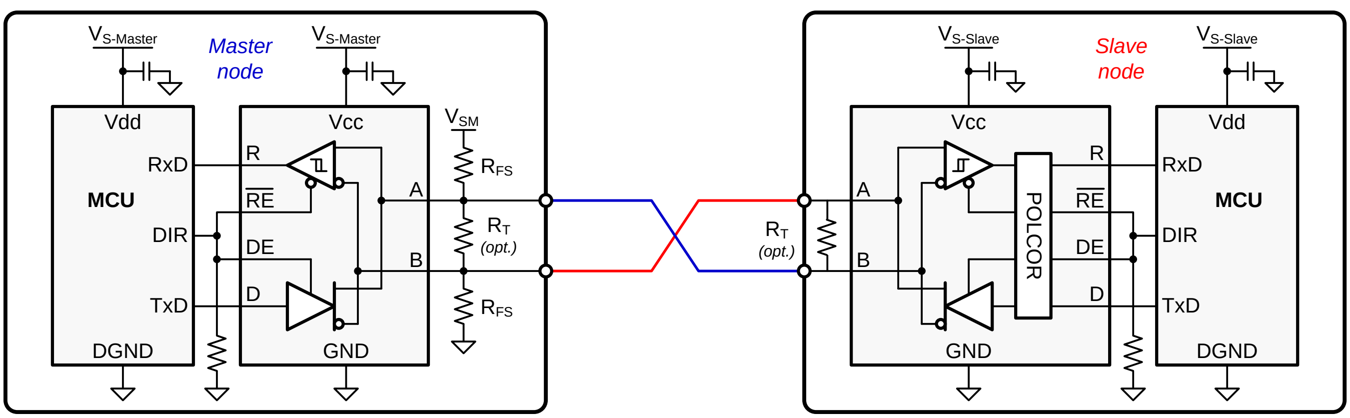


Figure 11. Point-To-Point Data Link With Cross-Wire Fault

Prior to initiating data transmission the master transceiver must idle for a time span that exceeds the maximum failsafe time, $t_{FS\text{-}max}$, of a slave transceiver. To accomplish this idle time, drive the direction control line, DIR, low. After a time, $t > t_{FS\text{-}max}$, the master begins transmitting data.

Because of the indicated cross-wire fault between master and slave, the slave node receives bus signals with reversed polarity. Assuming the slave node has just been connected to the bus, the direction-control pin is pulled-down during power-up, and then is actively driven low by the slave MCU. The polarity correction begins as soon as the slave supply is established and ends after approximately 44 to 76 ms.

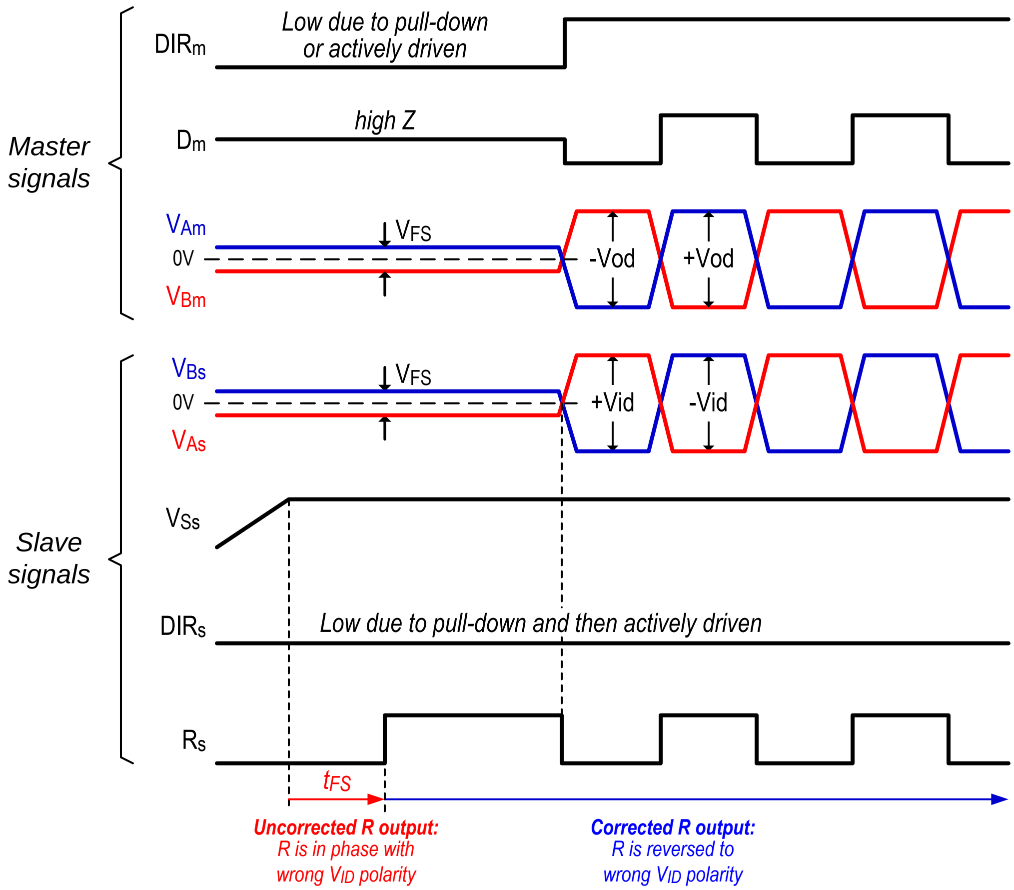


Figure 12. Polarity Correction Timing Prior to a Data Transmission

Initially the slave receiver assumes that the correct bus polarity is applied to the inputs and performs no polarity reversal. Because of the reversed polarity of the bus-failsafe voltage, the output of the slave receiver, R_S, turns low. After t_{FS} has passed and the receiver has detected the wrong bus polarity, the internal POLCOR logic reverses the input signal and R_S turns high.

At this point, all incoming bus data with reversed polarity are polarity-corrected within the transceiver. Because polarity correction is also applied to the transmit path, the data sent by the slave MCU are reversed by the POLCOR logic, then fed into the driver.

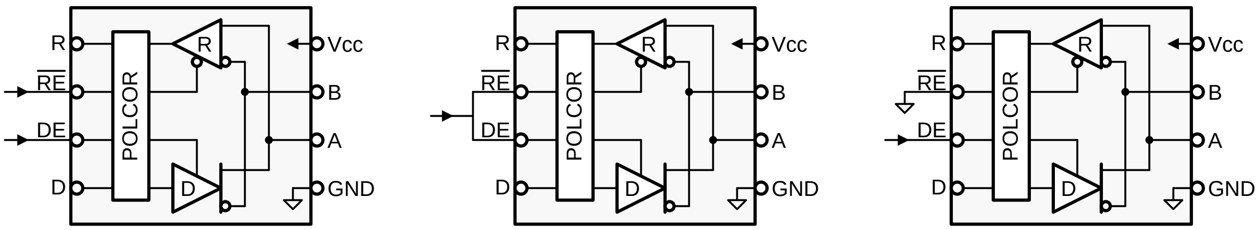
The reversed data from the slave MCU are reversed again by the cross-wire fault in the bus, and the correct bus polarity is reestablished at the master end.

This process repeats each time the device powers up and detects an incorrect bus polarity.

APPLICATION INFORMATION

Device Configuration

The SN888C device is a half-duplex RS-485 transceiver operating from a single 5-V ±10% supply. The driver and receiver enable pins that allow for the configuration of different operating modes.



a) Independent driver and receiver enable signals
b) Combined enable signals for use as directional control pin
c) Receiver always on

Figure 13. Transceiver Configurations

Using independent enable lines provides the most flexible control as the lines allow for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening to the bus traffic, whether the driver is transmitting data or not. Only this configuration allows the SN888C device to enter low-power standby mode because it allows both the driver and receiver to be disabled simultaneously.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. Thus, when the direction-control line is high, the transceiver is configured as a driver, while when low, the device operates as a receiver.

Tying the receiver enable to ground and controlling only the driver-enable input also uses only one control line. In this configuration, a node not only receives the data on the bus sent by other nodes, but also receives the data sent on the bus, enabling the node to verify the correct data has been transmitted.

Bus Design

An RS-485 bus consists of multiple transceivers connected in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, RT, whose value matches the characteristic impedance, Z0, of the cable. This method, known as parallel termination, allows for relatively high data rates over long cable length.

Common cables used are unshielded twisted pair (UTP), such as low-cost CAT-5 cable with Z0 = 100 Ω, and RS-485 cable with Z0 = 120 Ω. Typical cable sizes are AWG 22 and AWG 24.

The maximum bus length is typically given as 4000 ft or 1200 m, and represents the length of an AWG 24 cable whose cable resistance approaches the value of the termination resistance, thus reducing the bus signal by half or 6 dB. Actual maximum usable cable length depends on the signaling rate, cable characteristics, and environmental conditions.

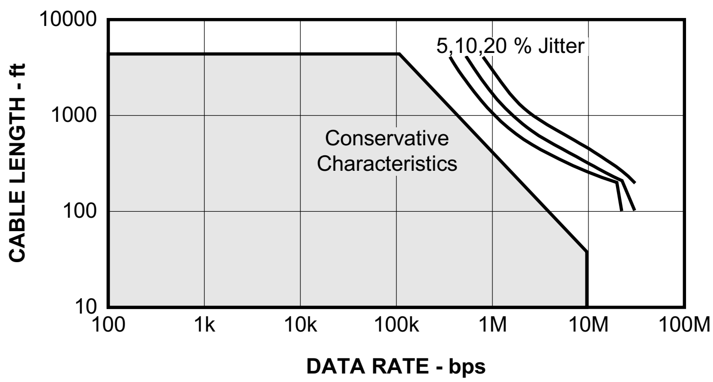
Table 1. VID With a Failsafe Network and Bus Termination

V_{CC}	R_L Differential Termination	R_{FS} Pull-Up	R_{FS} Pull-Down	V_{ID}
5 V	54 Ω	560 Ω	560 Ω	230 mV
		1 KΩ	1 KΩ	131 mV
		4.7 KΩ	4.7 KΩ	29 mV
		10 KΩ	10 KΩ	13 mV

An external failsafe-resistor network must be used to ensure failsafe operation during an idle bus state. When the bus is not actively driven, the differential receiver inputs could float allowing the receiver output to assume a random output. A proper failsafe network forces the receiver inputs to exceed the VIT threshold, thus forcing the SN888C receiver output into the failsafe (high) state. Table 1 shows the differential input voltage (V_{ID}) for various failsafe networks with a 54-Ω differential bus termination.

Cable Length Versus Data Rate

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, applications such as e-metering often operate at rates of up to 250 kbps even at distances of 4000 ft and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.



Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. The reason for the short distance is because a stub presents a non-terminated piece of bus line, which can introduce reflections if the distance is too long. As a general guideline, the electrical length or round-trip delay of a stub should be less than one-tenth of the rise time of the driver, thus leading to a maximum physical stub length as shown in Equation 1.

$L_{Stub} \leq 0.1 \times t_r \times v \times c$

where

- t_r is the 10 / 90 rise time of the driver
- c is the speed of light (3×10^8 m/s or 9.8×10^8 ft/s)
- v is the signal velocity of the cable (v = 78%) or trace (v = 45%) as a factor of c (1)

Based on Equation 1, with a minimum rise time of 400 ns, Equation 2 shows the maximum cable-stub length of the SN888C device.

$L_{Stub} \leq 0.1 \times 400 \times 10^{-9} \times 3 \times 10^8 \times 0.78 = 9{,}4$ m (or 30.6 ft) (2)

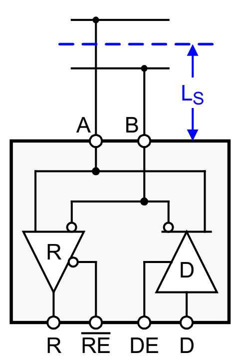


Figure 14. Stub Length

3-V to 5-V Interface

Interfacing the SN888C device to a 3-V controller is easy. Because the 5-V logic inputs of the transceiver accept 3-V input signals, they can be directly connected to the controller I/O. The 5-V receiver output, R, however, must be level-shifted by a Schottky diode and a 10-k resistor to connect to the controller input (see Figure 15). When R is high, the diode is reverse biased and the controller supply potential lies at the controller RxD input. When R is low, the diode is forward biased and conducts. Only in this case, the diode forward voltage of 0.2 V lies at the controller RxD input.

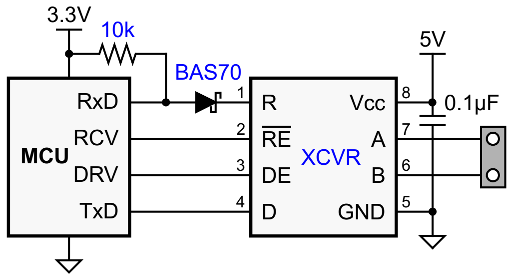


Figure 15. 3-V to 5-V Interface

Noise Immunity

The input sensitivity of a standard RS-485 transceiver is ±200 mV. When the differential input voltage, V_{ID}, is greater than +200 mV, the receiver output turns high, for V_{ID} < –200 mV the receiver outputs low.

The SN888C transceiver implements high receiver noise-immunity by providing a typical positive-going input threshold of 35 mV and a minimum hysteresis of 40 mV. In the case of a noisy input condition, a differential noise voltage of up to 40 mV_{PP} can be present without causing the receiver output to change states from high to low.

Transient Protection

The bus terminals of the SN888C transceiver family possess on-chip ESD protection against ±16 kV HBM and ±12 kV IEC61000-4-2 contact discharge. The International Electrotechnical Commision (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, C_S, and 78% lower discharge resistance, R_D of the IEC model produce significantly higher discharge currents than the HBM model.

As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method. Although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from the contact discharge test results.

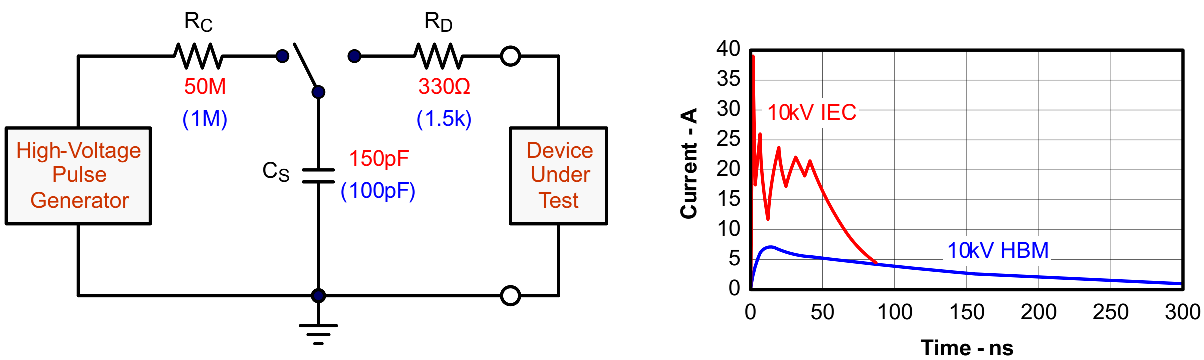


Figure 16. HBM and IEC-ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients. Figure 10 suggests two circuit designs providing protection against short and long-duration surge transients, in addition to ESD and Electrical Fast Transients (EFT) transients. Table 2 lists the bill of materials for the external protection devices.

EFTs are generally caused by relay-contact bounce, or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induces voltages and currents), or the switching of power systems, including load changes and short circuits switching. These transients are often encountered in industrial environments, such as in factory automation and power-grid systems.

Figure 17 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. In the diagram on the left of Figure 17, the tiny blue blip in the bottom left corner represents the power of a 10-kV ESD transient, which is low compared to the significantly higher EFT power spike, and certainly lower than the 500-V surge transient. This type of transient power is well representative of factory environments in industrial and process automation. The diagram on the right of Figure 17 compares the enormous power of a 6-kV surge transient, most likely occurring in e-metering applications of power generating and power grid systems, with the aforementioned 500-V surge transient.

NOTE

The unit of the pulse-power changes from kW to MW, thus making the power of the 500-V surge transient almost disappear from the scale.

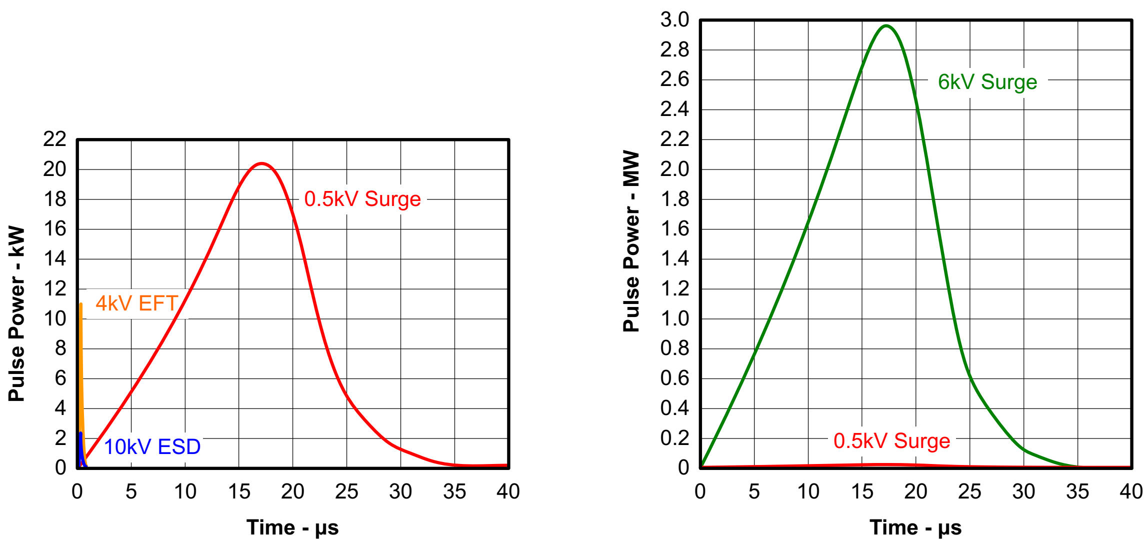


Figure 17. Power Comparison of ESD, EFT, and Surge Transients

In the case of surge transients, hgih-energy content is signified by long pulse duration and slow-decaying pulse power

The electrical energy of a transient that is dumped into the internal protection cells of the transceiver is converted into thermal energy. This thermal energy heats the protection cells and literally destroys them, thus destroying the transceiver. Figure 18 shows the large differences in transient energies for single ESD, EFT, and surge transients as well as for an EFT pulse train, commonly applied during compliance testing.

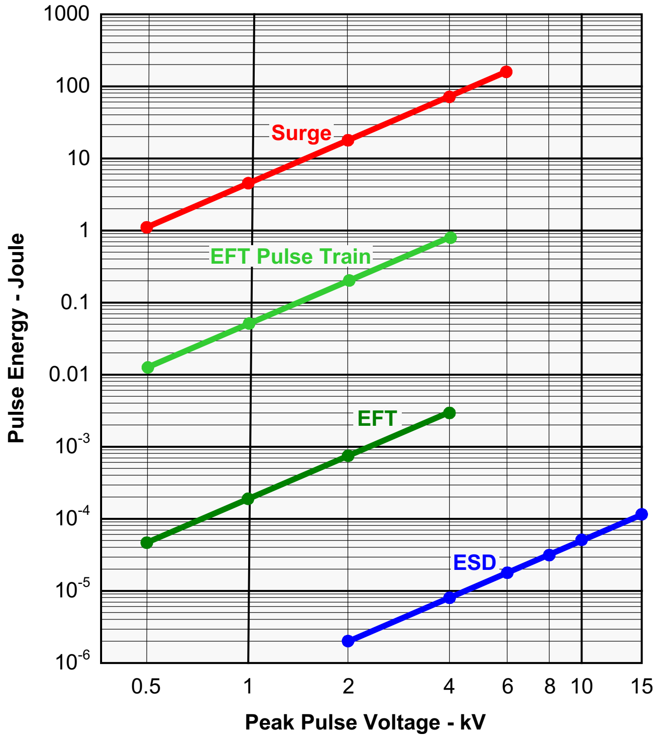


Figure 18. Comparison of Transient Energies

Table 2. Bill of Materials

Device	Function	Order Number	Manufacturer
XCVR	5-V, 250-kbps RS-485 Transceiver	SN888C	TI
R1, R2	10-Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400-W Transient Suppressor	CDSOT23-SM712	Bourns
TBU1, TBU2	Bidirectional.	TBU-CA-065-200-WH	Bourns
MOV1, MOV2	200mA Transient Blocking Unit 200-V, Metal-Oxide Varistor	MOV-10D201K	Bourns

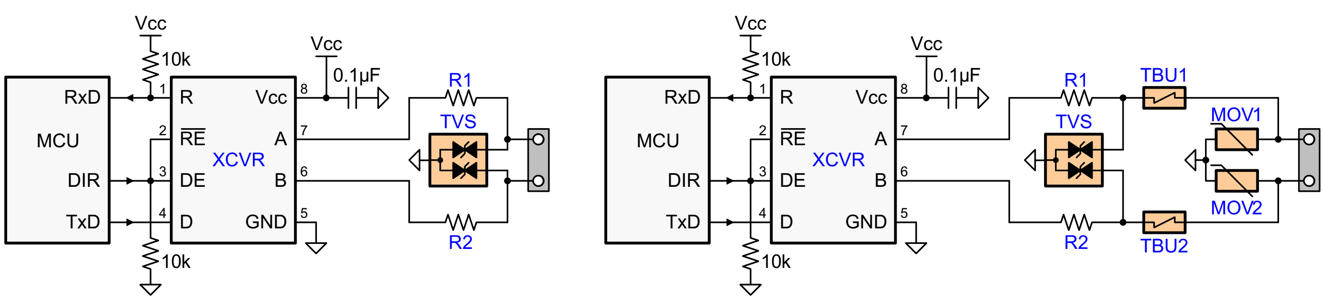


Figure 19. Transient Protections Against ESD, EFT, and Surge Transients

The left circuit shown in Figure 19 provides surge protection of ≥ 500-V transients, while the right protection circuits can withstand surge transients of 5 kV.

Design and Layout Considerations for Transient Protection

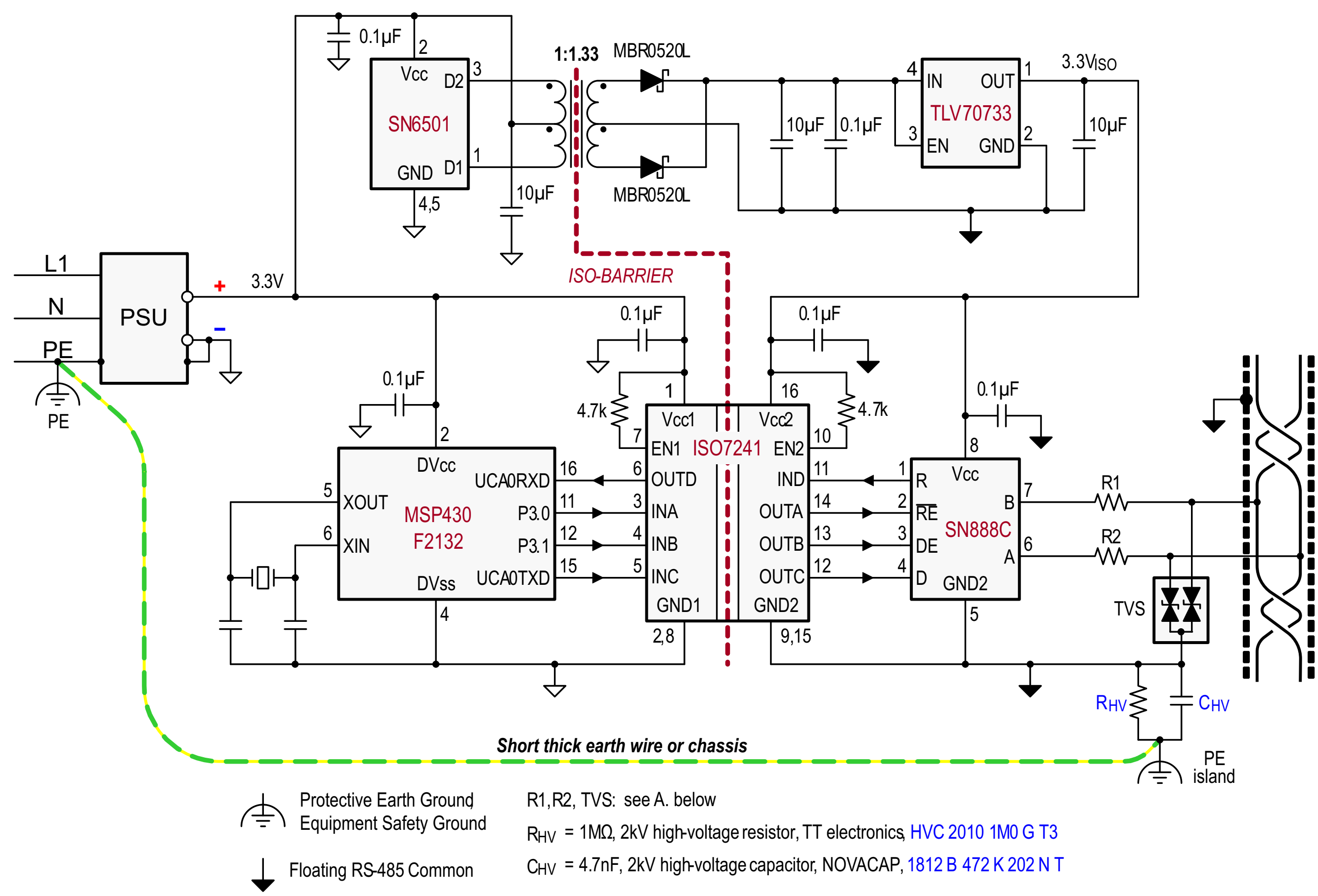
Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

In order for PCB design to be successful, begin with the design of the protection circuit in mind.

1. Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
2. Use V_{cc} and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance, not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
4. Apply 100-NF to 220-nF bypass capacitors as close as possible to the V_{CC}-pins of transceiver, UART, controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1-k to 10-k pull-up or pull-down resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines, if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
   – While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs), which reduce the transients to a few-hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to 200 mA.

Isolated Bus Node Design

Many RS-485 networks use isolated bus nodes to prevent the creation of unintended ground loops and their disruptive impact on signal integrity. An isolated bus node typically includes a micro controller that connects to the bus transceiver through a multi-channel, digital isolator (Figure 20).



A. See Table 2.

Figure 20. Isolated Bus Node With Transient Protection

Power isolation is accomplished using the push-pull transformer driver SN6501 and a low-cost LDO, TLV70733.

Signal isolation uses the quadruple digital isolator ISO7241. Notice that both enable inputs, EN1 and EN2, are pulled-up via 4.7-k resistors to limit input currents during transient events.

While the transient protection is similar to the one in Figure 19 (left circuit), an additional high-voltage capacitor diverts transient energy from the floating RS-485 common further towards protective earth (PE) ground. This diversion is necessary as noise transients on the bus are usually referred to earth potential.

R_{VH} refers to a high-voltage resistor, and in some applications, even a varistor. This resistance is applied to prevent charging of the floating ground to dangerous potentials during normal operation.

Occasionally varistors are used instead of resistors in order to rapidly discharge C_{HV}, if expecting that fast transients might charge C_{HV} to high-potentials.

Note that the PE island represents a copper island on the PCB for the provision of a short, thick earth wire connecting this island to PE ground at the entrance of the power supply unit (PSU).

In equipment designs using a chassis, the PE connection is usually provided through the chassis itself. Typically the PE conductor is tied to the chassis at one end, while the high-voltage components, C_{HV} and R_{HV}, connect to the chassis at the other end.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN888CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS485N EESA	Samples
SN888CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS485N EESA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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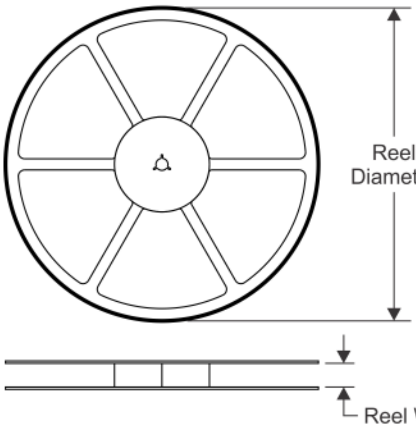
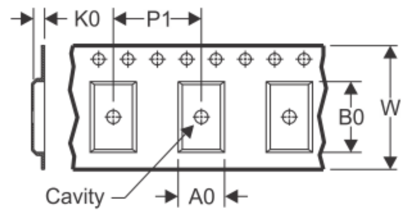
TAPE AND REEL INFORMATION

REEL DIMENSIONS

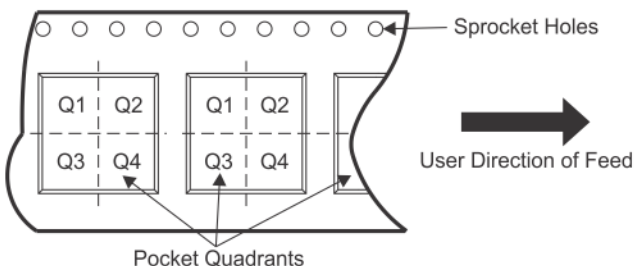


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

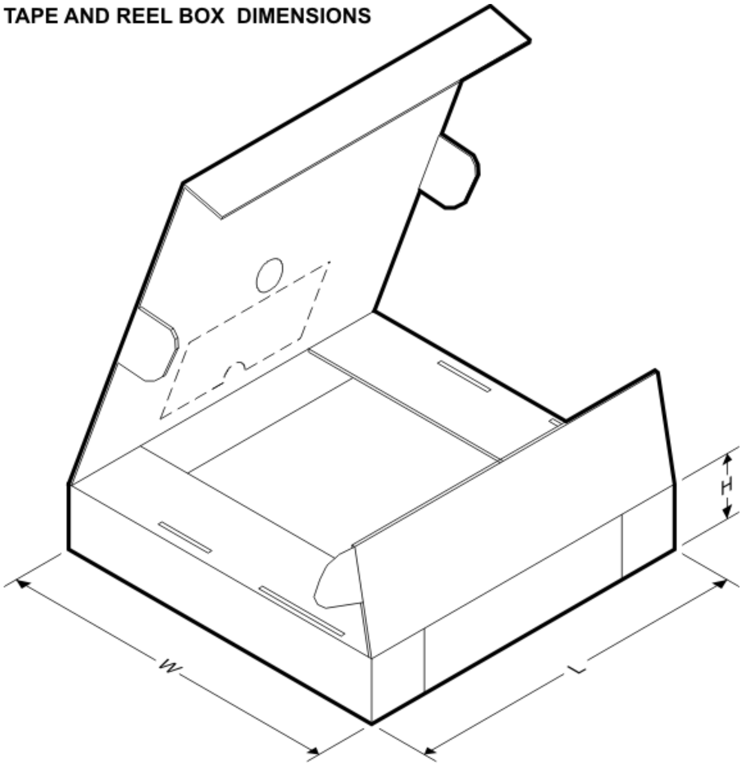
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN888CDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

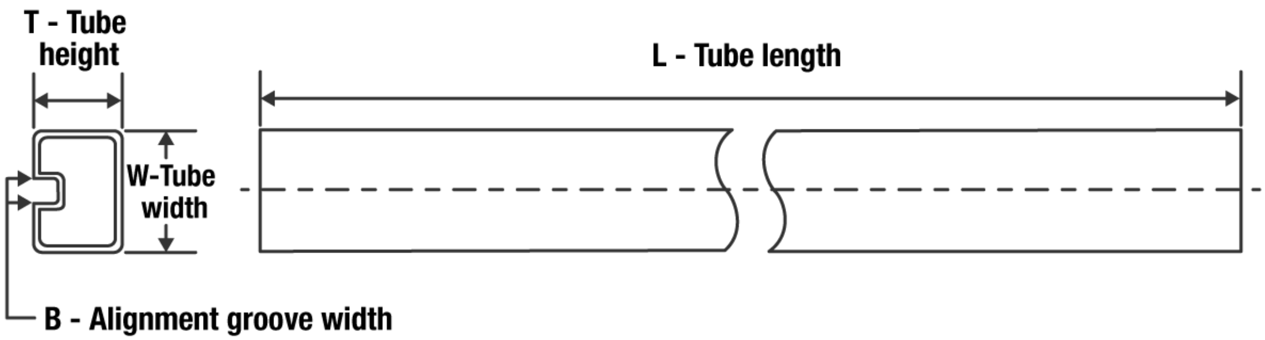
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

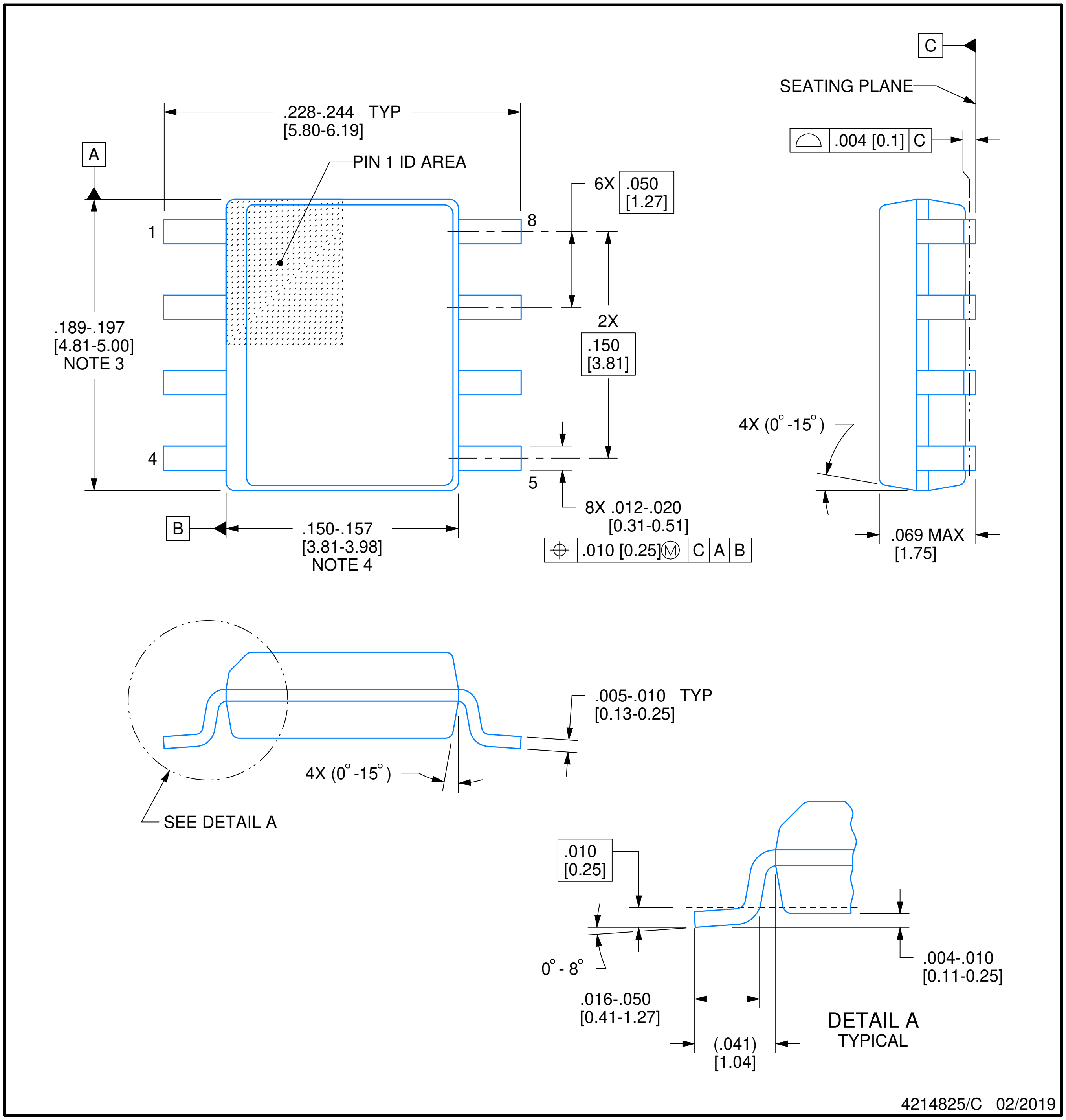
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN888CDR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN888CD	D	SOIC	8	75	507	8	3940	4.32



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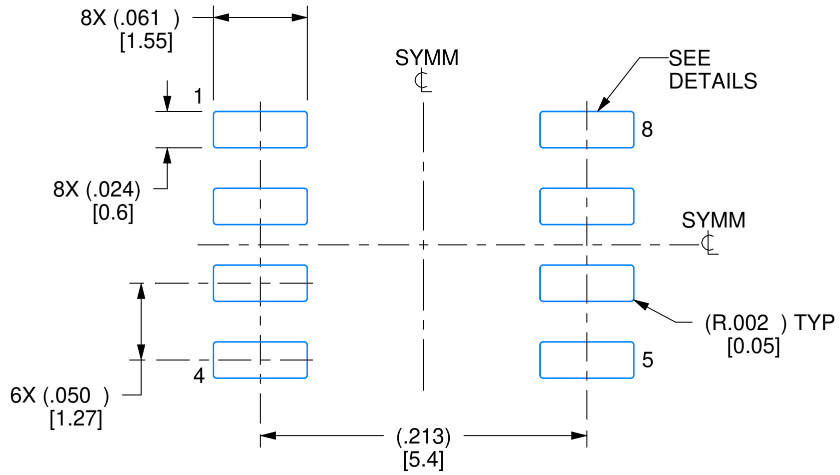
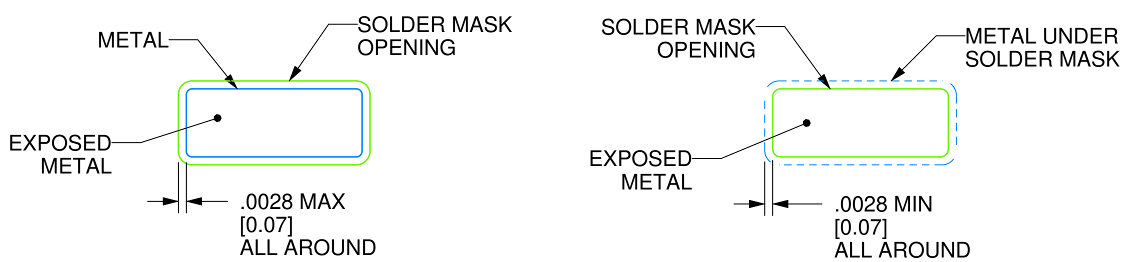
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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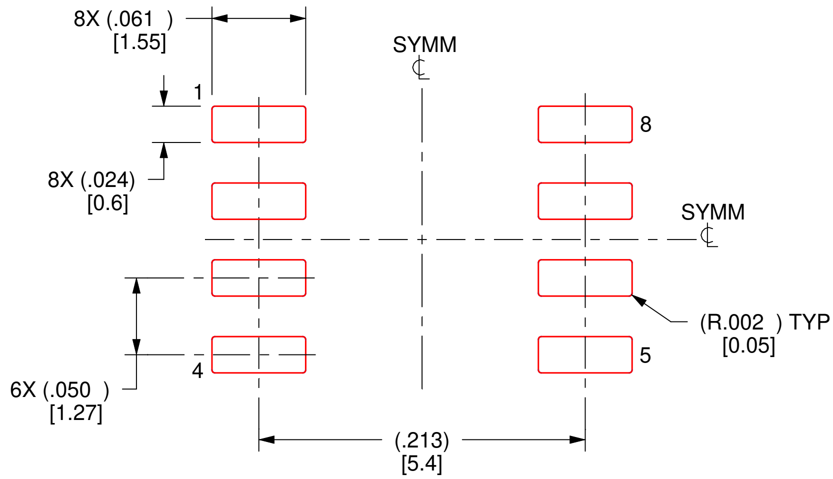
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.