April 2007

74VHC273
Octal D-Type Flip-Flop

Features

- High Speed: f_{MAX} = 165MHz (typ) at V_{CC} = 5V
- Low power dissipation: I_{CC} = 4μA (max) at T_A = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Power down protection is provided on all inputs
- Low noise: V_{OLP} = 0.9V (max)
- Pin and function compatible with 74HC273
- Leadless DQFN Package

General Description

The VHC273 is an advanced high speed CMOS Octal D-type flip-flop fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The register has a common buffered Clock (CP) which is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The Master Reset ($\overline{MR}$) input will clear all flip-flops simultaneously. All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input.

An input protection circuit insures that 0V to 7V can be applied to the inputs pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

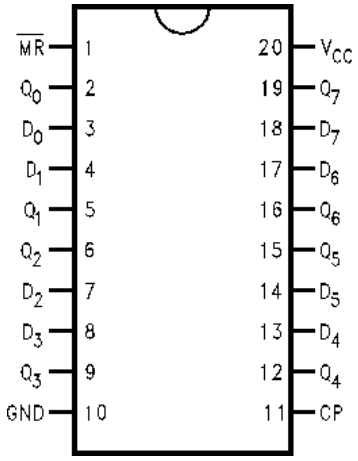
Ordering Information

Order Number	Package Number	Package Description
74VHC273M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VHC273SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC273BQ (Preliminary)	MLP020B (Preliminary)	20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm
74VHC273MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

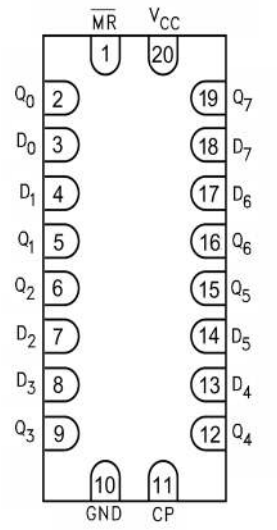
Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter “X” to the ordering number. Pb-Free package per JEDEC J-STD-020B.

Connection Diagrams

Pin Assignments for PDIP, SOIC, SOP, and TSSOP

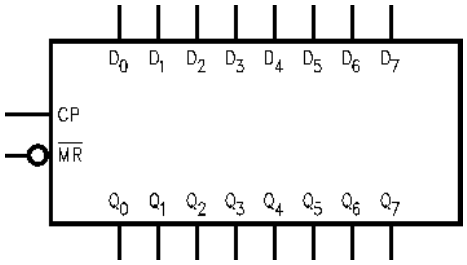


Pad Assignments for DQFN

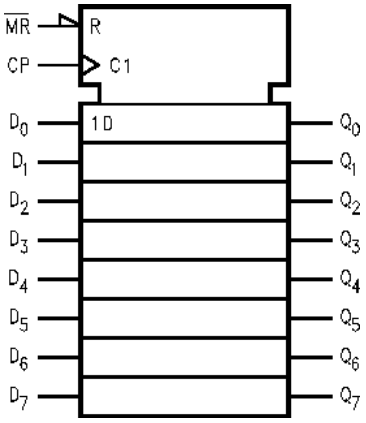


(Top Through View)

Logic Symbols



IEEE/IEC



Function Table

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H	⌐	H	H
Load '0'	H	⌐	L	L

H = HIGH Voltage Level

L = LOW Voltage Level

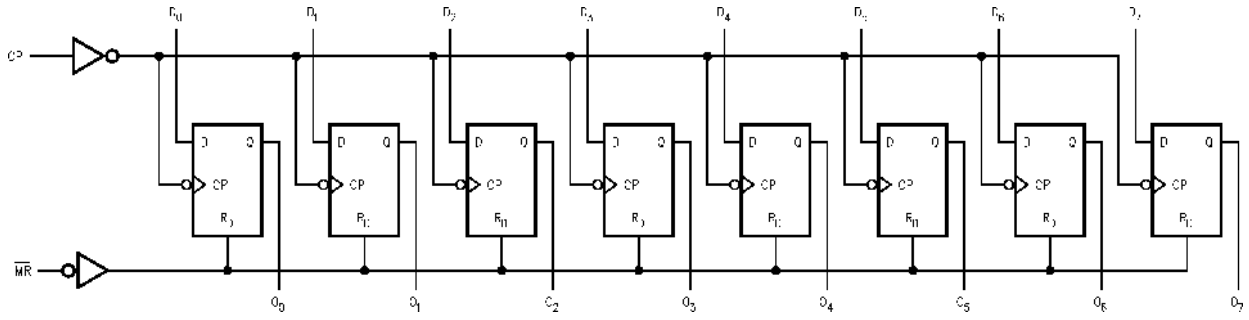
X = Immaterial

⌐ = LOW-to-HIGH Transition

Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 1.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_{IN}	DC Input Voltage	–0.5V to +7.0V
V_{OUT}	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_{IK}	Input Diode Current	–20mA
I_{OK}	Output Diode Current	±20mA
I_{OUT}	DC Output Current	±25mA
I_{CC}	DC V_{CC}/GND Current	±75mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions(1)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0V to +5.5V
V_{IN}	Input Voltage	0V to +5.5V
V_{OUT}	Output Voltage	0V to V_{CC}
T_{OPR}	Operating Temperature	–40°C to +85°C
t_r, t_f	Input Rise and Fall Time,	
	V_{CC} = 3.3V ± 0.3V	0ns/V ~ 100ns/V
	V_{CC} = 5.0V ± 0.5V	0ns/V ~ 20ns/V

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = 25°C Min.	T_A = 25°C Typ.	T_A = 25°C Max.	T_A = –40°C to +85°C Min.	T_A = –40°C to +85°C Max.	Units
V_{IH}	HIGH Level Input Voltage	2.0			1.50			1.50		V
		3.0–5.5			0.7 x V_{CC}			0.7 x V_{CC}		
V_{IL}	LOW Level Input Voltage	2.0					0.50		0.50	V
		3.0–5.5					0.3 x V_{CC}		0.3 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	2.0	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –50µA	1.9	2.0		1.9		V
		3.0			2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		3.0		I_{OH} = –4mA	2.58			2.48		
		4.5		I_{OH} = –8mA	3.94			3.80		
V_{OL}	LOW Level Output Voltage	2.0	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50µA		0.0	0.1		0.1	V
		3.0				0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		3.0		I_{OL} = 4mA			0.36		0.44	
		4.5		I_{OL} = 8mA			0.36		0.44	
I_{IN}	Input Leakage Current	0–5.5	V_{IN} = 5.5V or GND				±0.1		±1.0	µA
I_{CC}	Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND				4.0		40.0	µA

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C Typ.	T_A = 25°C Limits	Units
V_{OLP}(2)	Quiet Output Maximum Dynamic V_{OL}	5.0	C_L = 50pF	0.6	0.9	V
V_{OLV}(2)	Quiet Output Minimum Dynamic V_{OL}	5.0	C_L = 50pF	–0.6	–0.9	V
V_{IHD}(2)	Minimum HIGH Level Dynamic Input Voltage	5.0	C_L = 50pF		3.5	V
V_{ILD}(2)	Maximum LOW Level Dynamic Input Voltage	5.0	C_L = 50pF		1.5	V

Note:

2. Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = 25°C			T_A = –40°C to +85°C		Units
					Min.	Typ.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	3.3 ± 0.3		C_L = 15pF	75	120		65		MHz
				C_L = 50pF	50	75		45		
		5.0 ± 0.5		C_L = 15pF	120	165		100		MHz
				C_L = 50pF	80	110		70		
t_{PLH}, t_{PHL}	Propagation Delay Time (CK – Q)	3.3 ± 0.3		C_L = 15pF		8.7	13.6	1.0	16.0	ns
				C_L = 50pF		11.2	17.1	1.0	19.5	
		5.0 ± 0.5		C_L = 15pF		5.8	9.0	1.0	10.5	ns
				C_L = 50pF		7.3	11.0	1.0	12.5	
t_{PHL}	Propagation Delay Time ($\overline{MR}$ – Q)	3.3 ± 0.3		C_L = 15pF		8.9	13.6	1.0	16.0	ns
				C_L = 50pF		11.4	17.1	1.0	19.5	
		5.0 ± 0.5		C_L = 15pF		5.2	8.5	1.0	10.0	ns
				C_L = 50pF		6.7	10.5	1.0	12.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew	3.3 ± 0.3	(3)	C_L = 50pF			1.5		1.5	ns
		5.0 ± 0.5		C_L = 50pF			1.0		1.0	
C_{IN}	Input Capacitance		V_{CC} = Open			4.0	10.0		10.0	pF
C_{PD}	Power Dissipation Capacitance		(4)			31				pF

Notes:

3. Parameter guaranteed by design $t_{OSLH} = |t_{PLH}max – t_{PLH}min|$; $t_{OSHL} = |t_{PHL}max – t_{PHL}min|$.

4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I_{CC} (opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8$ (per F/F). The total C_{PD} when n pieces of the Flip-Flop operates can be calculated by the equation: C_{PD} (total) = 22 + 9n.

AC Operating Requirements

Symbol	Parameter	V_{CC} (V)(5)	T_A = 25°C	T_A = –40°C to +85°C		Units
			Typ.	Guaranteed Minimum		
t_W(L), t_W(H)	Minimum Pulse Width (CK)	3.3		5.5	6.5	ns
		5.0		5.0	5.0	
t_W(L)	Minimum Pulse Width ($\overline{MR}$)	3.3		5.0	6.0	ns
		5.0		5.0	5.0	
t_S	Minimum Setup Time	3.3		5.5	6.5	ns
		5.0		4.5	4.5	
t_H	Minimum Hold Time	3.3		1.0	1.0	ns
		5.0		1.0	1.0	
t_{REC}	Minimum Removal Time ($\overline{MR}$)	3.3		2.5	2.5	ns
		5.0		2.0	2.0	

Note:

5. V_{CC} is 3.3 ± 0.3V or 5.0 ± 0.5V

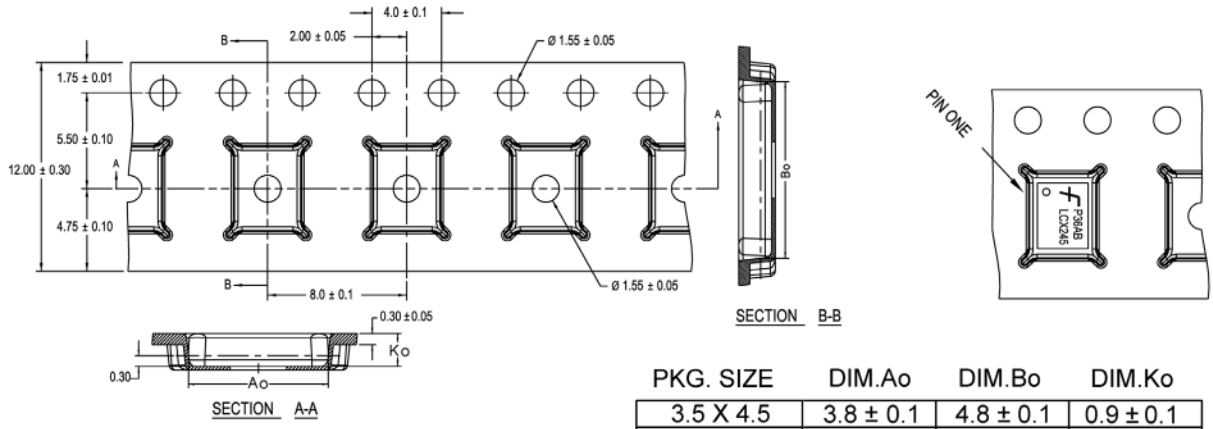
Tape and Reel Specification

Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQ	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

Tape Dimensions

Dimensions are in millimeters unless otherwise noted.



PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

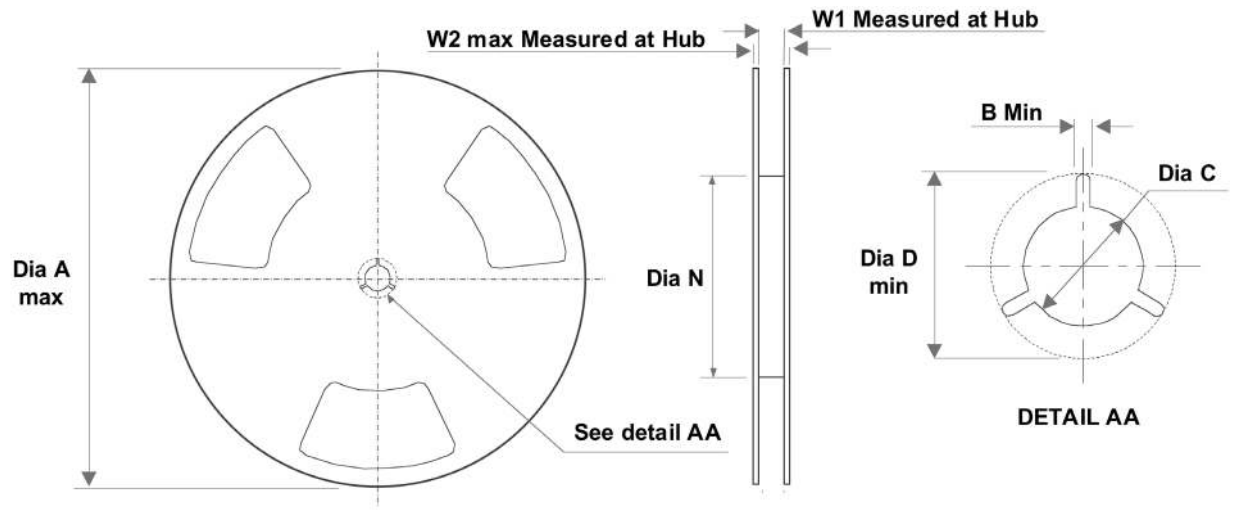
1. Cummulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Diemension in inches rounded.

Figure 2.

Tape and Reel Specification (Continued)

Reel Dimensions for DQFN

Dimensions are in inches (millimeters) unless otherwise noted.



Tape Size	A	B	C	D	N	W1	W2
12mm	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)

Figure 3.

Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

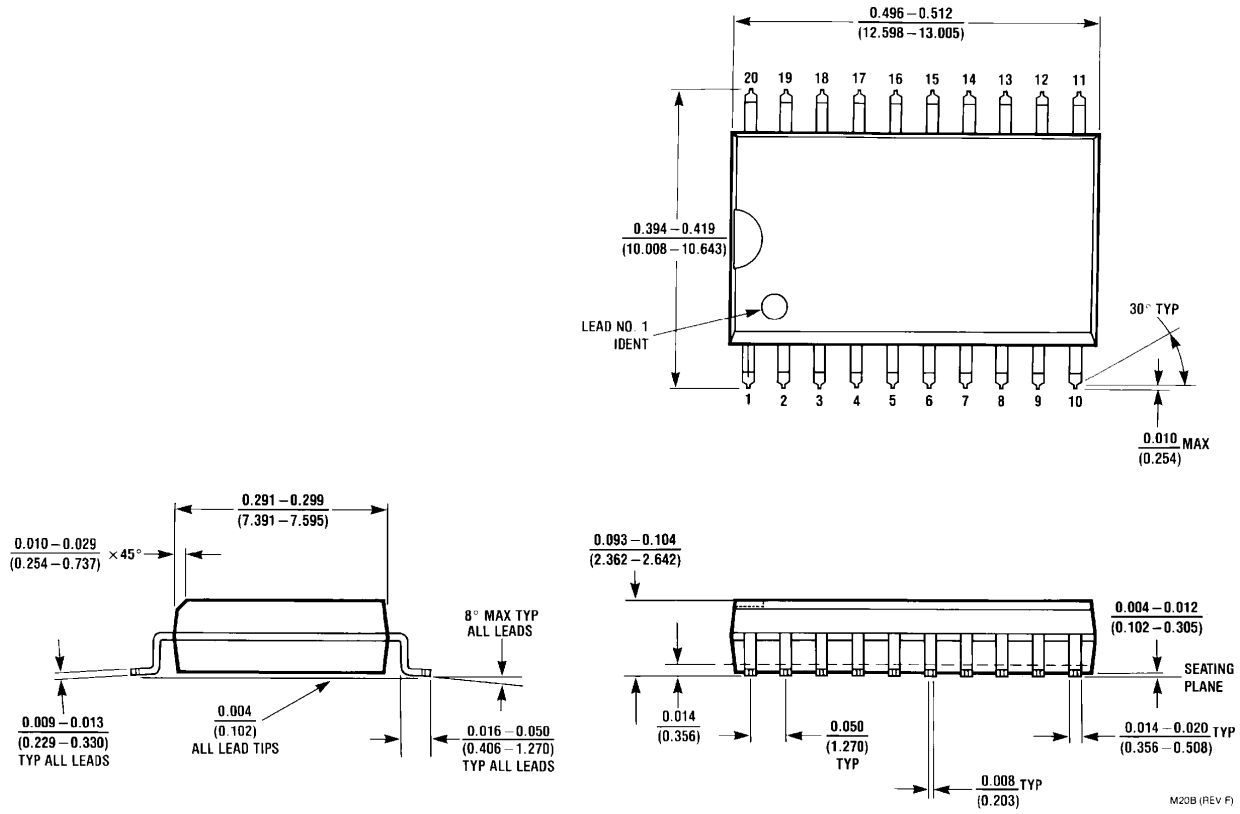


Figure 4. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.

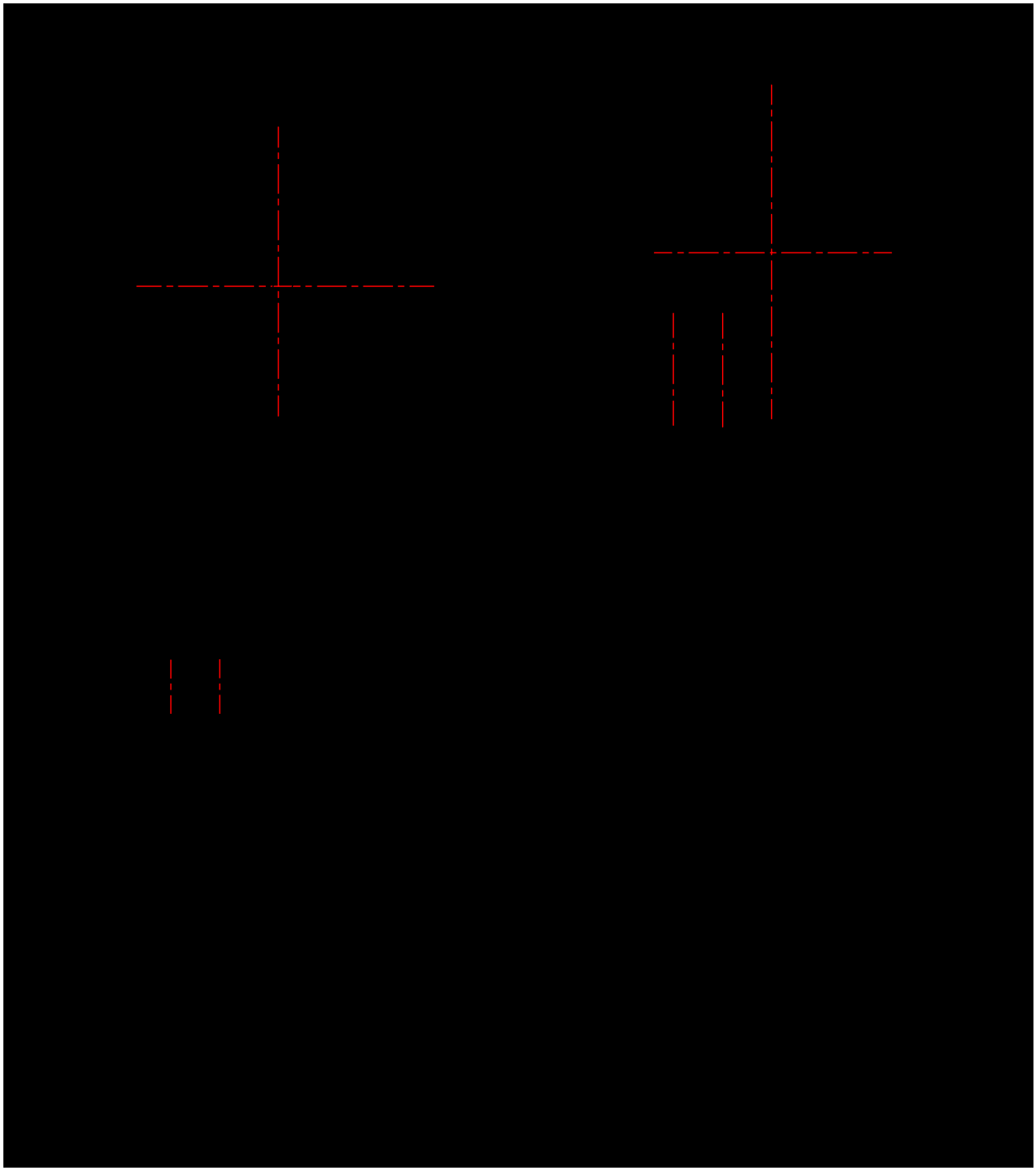
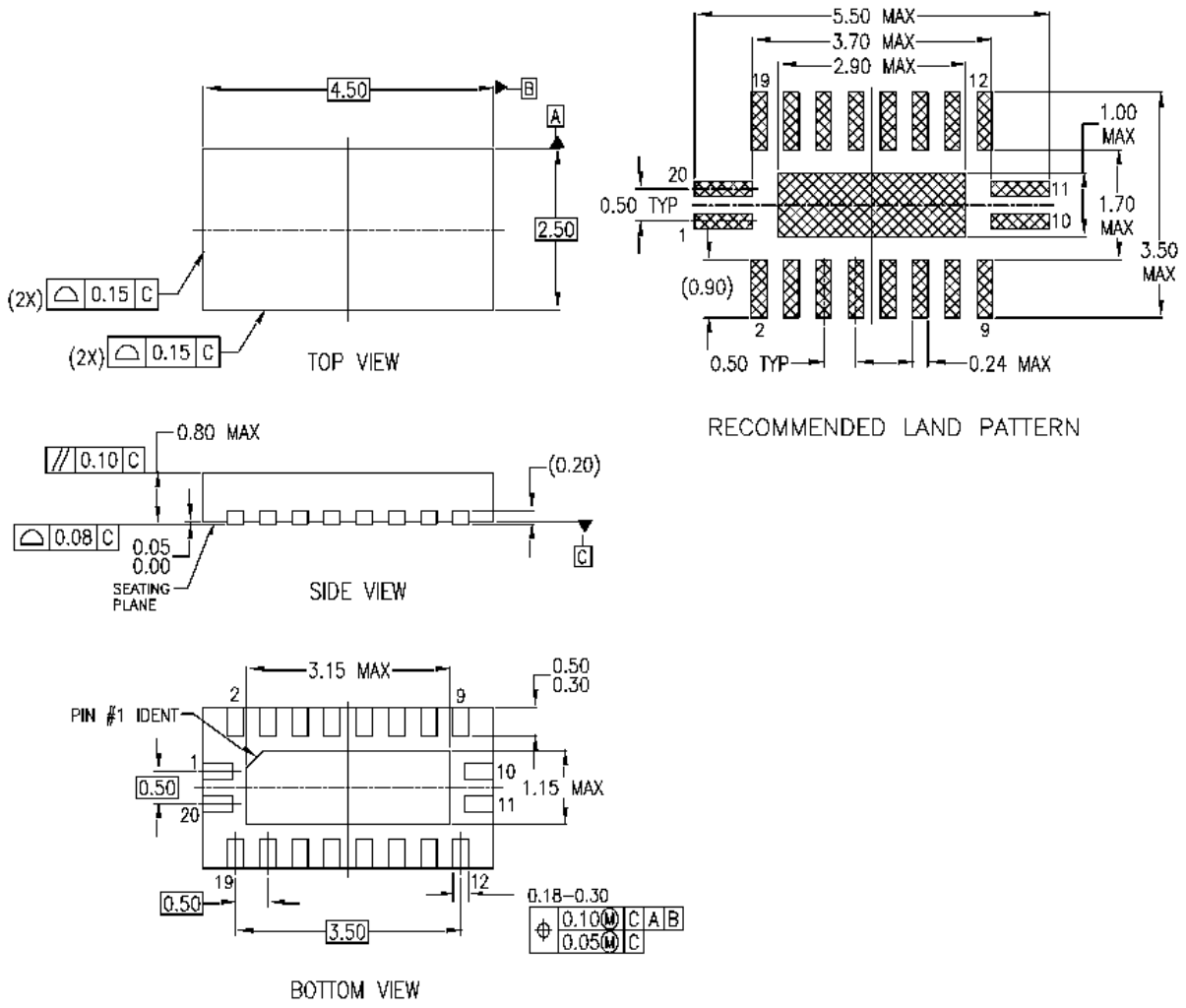


Figure 5. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AC
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP020BrevA

Figure 6. 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm Package Number MLP020B (Preliminary)

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.

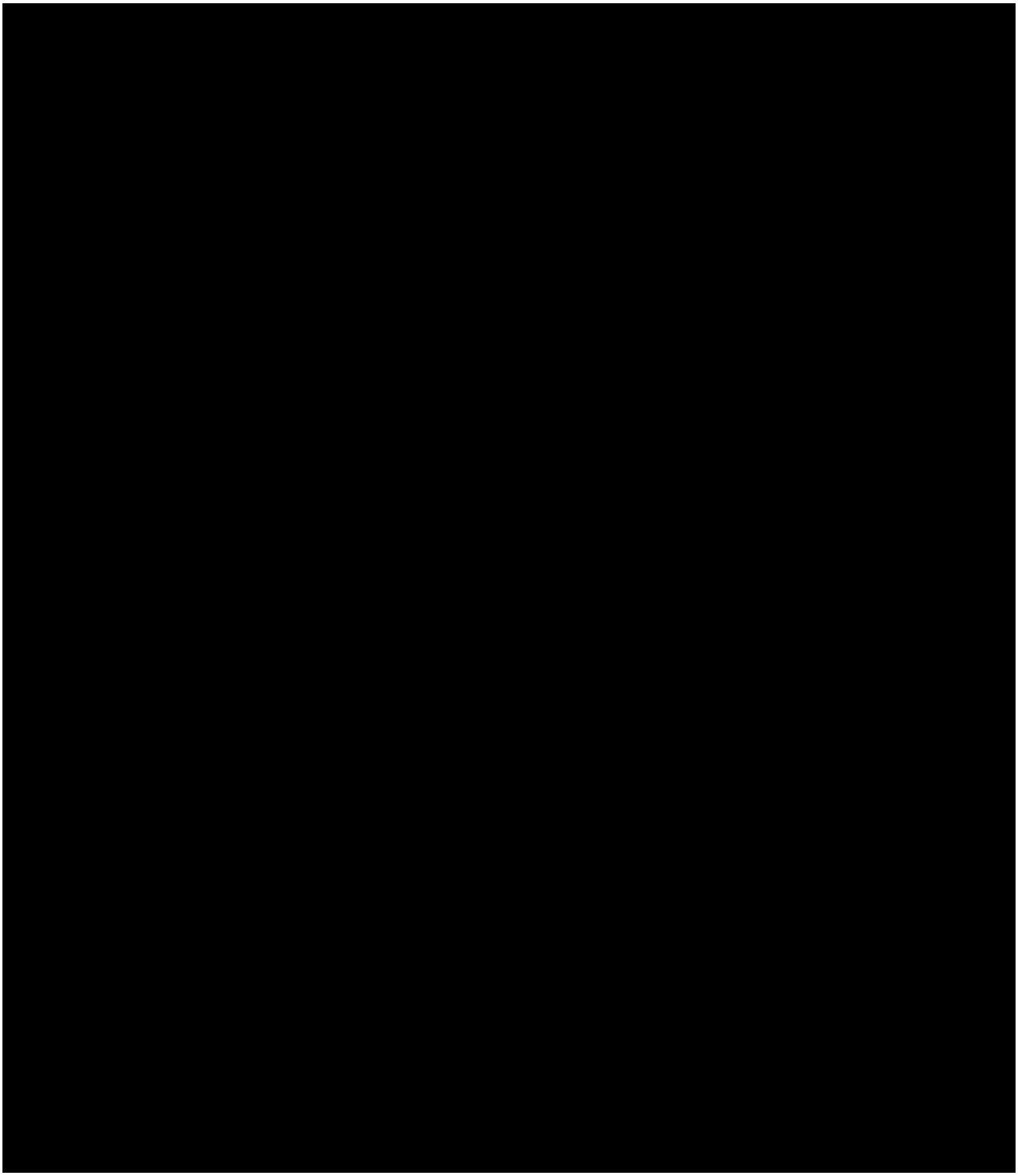


Figure 7. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20