

# ISO308x Isolated 5-V Full- and Half-Duplex RS-485 Transceivers

## 1 Features

- Meets or exceeds TIA/EIA RS-485 requirements
- Signaling rates up to 20 Mbps
- 1/8 unit load – up to 256 nodes on a bus
- Thermal shutdown protection
- Low bus capacitance – 16 pF (typical)
- 50 kV/μs typical transient immunity
- Fail-safe receiver for bus open, short, idle
- 3.3-V inputs are 5-V tolerant
- Bus-pin ESD protection
  - 12-kV HBM between bus pins and GND2
  - 6-kV HBM between bus pins and GND1
- Safety-related certifications:
  - 4000- $V_{PK}$  basic insulation, 560  $V_{PK}$   $V_{IORM}$  per DIN EN IEC 60747-17 (VDE 0884-17)
  - 2500  $V_{RMS}$  isolation per UL 1577
  - 4000  $V_{PK}$  isolation per CSA 62368-1

## 2 Applications

- Security systems
- Chemical production
- Factory automation
- Motor and motion control
- HVAC and building automation networks
- Networked security stations

## 3 Description

The ISO3080 and ISO3086 devices are isolated full-duplex differential line drivers and receivers while the ISO3082 and ISO3088 devices are isolated half-duplex differential line transceivers for TIA/EIA 485/422 applications.

These devices are ideal for long transmission lines because the ground loop is broken to allow for a much larger common-mode voltage range. The symmetrical isolation barrier of the device is tested to provide 2500  $V_{RMS}$  of isolation for 60 s per UL 1577 between the bus-line transceiver and the logic-level interface.

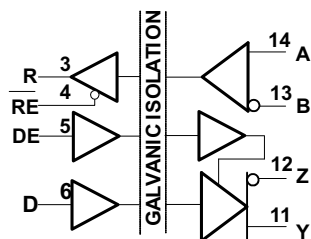
Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver or nearby sensitive circuitry if they are of sufficient magnitude and duration. These isolated devices can significantly increase protection and reduce the risk of damage to expensive control circuits.

The ISO3080, ISO3082, ISO3086, and ISO3088 device are qualified for use from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

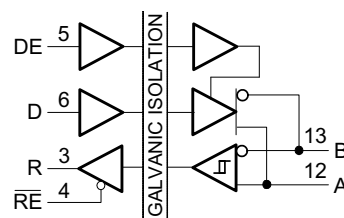
### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE   | BODY SIZE (NOM)    |
|-------------|-----------|--------------------|
| ISO3080     | SOIC (16) | 10.30 mm × 7.50 mm |
| ISO3082     |           |                    |
| ISO3086     |           |                    |
| ISO3088     |           |                    |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



ISO3080, IOS3086 Function Diagram



ISO3082, IOS3088 Function Diagram



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision I (April 2017) to Revision J (August 2023)</b>  | <b>Page</b> |
|--|-------------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document.....  | 1           |
| • Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations.....   | 6           |
| • Updated electrical and switching characteristics to match device performance.....  | 8           |
| <b>Changes from Revision H (December 2015) to Revision I (April 2017)</b>  | <b>Page</b> |
| • Switched the R and D pins of the master device in the <i>Typical RS-485 Network With Full-Duplex Transceivers</i> figure.....  | 22          |
| • Added the <i>Receiving Notification of Documentation Updates</i> section.....  | 26          |
| • Changed the <i>Electrostatic Discharge Caution</i> statement.....  | 26          |
| <b>Changes from Revision G (July 2015) to Revision H (December 2015)</b>   | <b>Page</b> |
| • Moved the last list item "Routing the high-speed traces..." to the second list items in <i>Layout Guidelines</i> section.....  | 24          |
| <b>Changes from Revision F (May 2015) to Revision G (July 2015)</b>  | <b>Page</b> |
| • Changed the <i>Layout Guidelines</i> section .....   | 24          |
| <b>Changes from Revision E (September 2011) to Revision F (May 2015)</b>   | <b>Page</b> |
| • Added <i>ESD Rating</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section..... | 1           |
| • Changed <i>Features</i> list item From: IEC 60747-5-2 (VDE 0884, Rev. 2) To: DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12.....   | 1           |
| • VDE standard changed to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12.....   | 1           |

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**Changes from Revision D (January 2011) to Revision E (September 2011) Page**

- Changed *Features* list item From: 16 kV HBM To: 12 kV HBM..... **1**

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**Changes from Revision C (October 2009) to Revision D (January 2011) Page**

- Changed graph for " DW-16  $\theta_{JC}$  Thermal Derating Curve per IEC 60747-5-2 " , *Thermal Derating Curve* .... **12**
- Added the *ISO3086 Recommended Minimum Differential Input Voltage vs Signaling Rate* graph..... **13**
- Added note to bottom of first page of the *Parameter Measurement Information* ..... **15**
- Added Footnotes to the *Driver Function Table* and *Receiver Function Table* ..... **20**

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**Changes from Revision A (June 2008) to Revision B (December 2008) Page**

- Changed *Features* bullet From: 4000-V<sub>PEAK</sub> Isolation, To: 4000-V<sub>PEAK</sub> Isolation,, 560-V<sub>PEAK</sub> V<sub>IORM</sub> ..... **1**

## 5 Pin Configuration and Functions

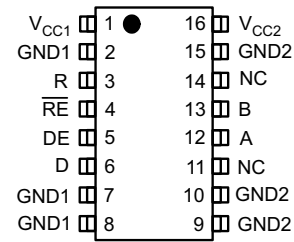
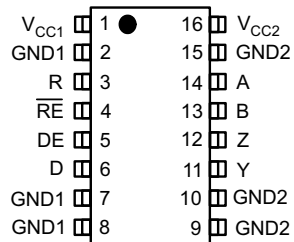


Figure 5-1. ISO3080 and ISO3086 DW Package 16-Pin SOIC Top View

Figure 5-2. ISO3082 and ISO3088 DW Package 16-Pin SOIC Top View

Table 5-1. Pin Functions

| NAME      | PIN              |                  | I/O | DESCRIPTION   |
|-----------|------------------|------------------|-----|---|
|           | ISO3080, ISO3086 | ISO3082, ISO3088 |     |   |
| A         | 14               | —                | I   | Receiver noninverting input on the bus-side                                   |
|           | —                | 12               | I/O | Transceiver noninverting Input or output (I/O) on the bus-side                |
| B         | 13               | —                | I   | Receiver inverting Input on the bus-side                                      |
|           | —                | 13               | I/O | Transceiver inverting input or output (I/O) on the bus-side                   |
| D         | 6                | 6                | I   | Driver input  |
| DE        | 5                | 5                | I   | Enables (when high) or disables (when low or open) driver output of ISO308x   |
| GND1      | 2                | 2                | —   | Ground connection for $V_{CC1}$   |
|           | 7                | 7                |     |   |
|           | 8                | 8                |     |   |
| GND2      | 9                | 9                | —   | Ground connection for $V_{CC2}$   |
|           | 10               | 10               |     |   |
|           | 15               | 15               |     |   |
| NC        | —                | 11               | —   | No connect  |
|           | —                | 14               |     |   |
| R         | 3                | 3                | O   | Receiver output   |
| RE        | 4                | 4                | I   | Disables (when high or open) or enables (when low) receiver output of ISO308x |
| $V_{CC1}$ | 1                | 1                | —   | Power supply, $V_{CC1}$   |
| $V_{CC2}$ | 16               | 16               | —   | Power supply, $V_{CC2}$   |
| Y         | 11               | —                | O   | Driver noninverting output  |
| Z         | 12               | —                | O   | Driver inverting output   |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                         |   | MIN  | MAX | UNIT |
|-------------------------|---|------|-----|------|
| $V_{CC}$ <sup>(2)</sup> | Supply voltage, $V_{CC1}$ , $V_{CC2}$   | -0.3 | 6   | V    |
| $V_O$                   | Voltage at any bus I/O terminal   | -9   | 14  | V    |
| $V_{IT}$                | Voltage input, transient pulse, A, B, Y, and Z (through 100 $\Omega$ , see Figure 21) | -50  | 50  | V    |
| $V_I$                   | Voltage input at any D, DE or RE terminal   | -0.5 | 6   | V    |
| $I_O$                   | Receiver output current   | -10  | 10  | mA   |
| $T_J$                   | Junction temperature  |      | 150 | °C   |
| $T_{STG}$               | Storage temperature   | -65  | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

### 6.2 ESD Ratings

|                                     |  | VALUE             | UNIT   |   |
|-------------------------------------|--|-------------------|--------|---|
| $V_{(ESD)}$ Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>                        | Bus pins and GND1 | ±6000  | V |
|                                     |  | Bus pins and GND2 | ±12000 | V |
|                                     |  | All pins          | ±4000  | V |
|                                     | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> |                   | ±1000  | V |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

|           |  | MIN           | TYP | MAX      | UNIT     |
|-----------|--|---------------|-----|----------|----------|
| $V_{CC1}$ | Logic-side supply voltage                                | 3.15          |     | 5.5      | V        |
| $V_{CC2}$ | Bus-side supply voltage                                  | 4.5           | 5   | 5.5      | V        |
| $V_{OC}$  | Voltage at either bus I/O pin A, B                       | -7            |     | 12       | V        |
| $V_{IH}$  | High-level input voltage (D, DE, $\overline{RE}$ inputs) | 2             |     | $V_{CC}$ | V        |
| $V_{IL}$  | Low-level input voltage (D, DE, $\overline{RE}$ inputs)  | 0             |     | 0.8      | V        |
| $V_{ID}$  | Differential input voltage, A with respect to B          | -12           |     | 12       | V        |
| $V_{ID}$  | Differential input voltage, Dynamic (ISO3086)            | See Figure 10 |     |          | V        |
| $R_L$     | Differential load resistance                             | 54            | 60  |          | $\Omega$ |
| $I_O$     | Output current, Driver                                   | -60           |     | 60       | mA       |
| $I_O$     | Output current, Receiver                                 | -8            |     | 8        | mA       |
| $T_A$     | Operating ambient temperature (ISO15 and ISO35)          | -40           |     | 85       | °C       |

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | ISO308x   | UNIT |
|-------------------------------|--|-----------|------|
|                               |  | DW (SOIC) |      |
|                               |  | 16 PINS   |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 79.6      | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 39.7      | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 44.7      | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 13.2      | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 44.0      | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | —         | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 6.5 Insulation Specifications

| PARAMETER   |   | TEST CONDITIONS   | VALUE             | UNIT             |
|---|---|---|-------------------|------------------|
|   |   |   | DW-16             |                  |
| CLR   | External clearance <sup>(1)</sup>                   | Shortest terminal-to-terminal distance through air  | 8                 | mm               |
| CPG   | External creepage <sup>(1)</sup>                    | Shortest terminal-to-terminal distance across the package surface   | 8                 | mm               |
| DTI   | Distance through the insulation                     | Minimum internal gap (internal clearance)   | 8                 | um               |
| CTI   | Comparative tracking index                          | DIN EN 60112 (VDE 0303-11); IEC 60112   | >400              | V                |
|   | Material group                                      | According to IEC 60664-1  | II                |                  |
|   | Overvoltage category per IEC 60664-1                | Rated mains voltage ≤ 150 V <sub>RMS</sub>  | I-IV              |                  |
|   |   | Rated mains voltage ≤ 300 V <sub>RMS</sub>  | I-III             |                  |
| <b>DIN EN IEC 60747-17 (VDE 0884-17) <sup>(2)</sup></b> |   |   |                   |                  |
| V <sub>IORM</sub>                                       | Maximum repetitive peak isolation voltage           | AC voltage (bipolar)  | 560               | V <sub>PK</sub>  |
| V <sub>IOTM</sub>                                       | Maximum transient isolation voltage                 | V <sub>TEST</sub> = V <sub>IOTM</sub> ,<br>t = 60 s (qualification);<br>V <sub>TEST</sub> = 1.2 x V <sub>IOTM</sub> ,<br>t = 1 s (100% production)  | 4000              | V <sub>PK</sub>  |
| q <sub>pd</sub>   | Apparent charge <sup>(3)</sup>                      | Method b; At routine test (100% production)<br>V <sub>ini</sub> = 1.2 x V <sub>IOTM</sub> , t <sub>ini</sub> = 1 s;<br>V <sub>pd(m)</sub> = 1.5x V <sub>IORM</sub> , t <sub>m</sub> = 1 s | ≤5                | pC               |
| C <sub>IO</sub>   | Barrier capacitance, input to output <sup>(4)</sup> | V <sub>IO</sub> = 0.4 x sin(2πft), f = 1 MHz  | 2                 | pF               |
| C <sub>I</sub>  | Input capacitance to ground                         | V <sub>I</sub> = VCC/ 2 + 0.4×sin(2πft), f = 1 MHz, VCC = 5 V   | 2                 | pF               |
| R <sub>IO</sub>   | Isolation resistance <sup>(4)</sup>                 | V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C  | >10 <sup>12</sup> | Ω                |
|   |   | V <sub>IO</sub> = 500 V, T <sub>S</sub> = 150°C   | >10 <sup>9</sup>  |                  |
|   | Pollution degree                                    |   | 2                 |                  |
|   | Climatic category                                   |   | 40/125/21         |                  |
| <b>UL 1577</b>  |   |   |                   |                  |
| V <sub>ISO</sub>  | Maximum withstanding isolation voltage              | V <sub>TEST</sub> = V <sub>ISO</sub> , t = 60 s (qualification),<br>V <sub>TEST</sub> = 1.2 x V <sub>ISO</sub> , t = 1 s (100% production)  | 2500              | V <sub>RMS</sub> |

- Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
- This coupler is suitable for *basic electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- Apparent charge is electrical discharge caused by a partial discharge (pd).

- (4) All pins on each side of the barrier tied together creating a two-terminal device.

## 6.6 Safety-Related Certifications

| VDE   | CSA   | UL   |
|---|---|--|
| Certified according to DIN EN IEC 60747-17 (VDE 0884-17)  | Certified according to IEC 60950-1 and IEC 62368-1  | Recognized under UL 1577 Component Recognition Program |
| Basic insulation, 4000 V <sub>PK</sub> Maximum transient isolation voltage, 560 V <sub>PK</sub> Maximum repetitive peak isolation voltage | 4000V <sub>RMS</sub> Isolation Rating; Reinforced insulation per CSA 60950-1 and IEC 60950-1 148 V <sub>RMS</sub> working voltage; Basic insulation per CSA 62368-1 and IEC 62368-1 300V <sub>RMS</sub> working voltage | Single protection, 2500 V <sub>RMS</sub>               |
| Certificate number: 40047657  | Master contract number: 220991  | File number: E181974                                   |

## 6.7 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

| PARAMETER            |   | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |
|----------------------|---|---|-----|-----|-----|------|
| <b>DW-16 PACKAGE</b> |   |   |     |     |     |      |
| I <sub>S</sub>       | Safety input, output, or supply current | R <sub>θJA</sub> = 79.6°C/W, V <sub>I</sub> = 5.5 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see |     |     | 286 | mA   |
| T <sub>S</sub>       | Maximum safety temperature              |   |     |     | 150 | °C   |

- (1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of I<sub>S</sub> and P<sub>S</sub> should not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>. The junction-to-air thermal resistance, R<sub>θJA</sub>, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:  
 $T_J = T_A + R_{\theta JA} \times P$ , where P is the power dissipated in the device.  
 $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$ , where T<sub>J(max)</sub> is the maximum allowed junction temperature.  
 $P_S = I_S \times V_I$ , where V<sub>I</sub> is the maximum input voltage.

## 6.8 Electrical Characteristics: Driver

All typical specs are at  $V_{CC1}=3.3V$ ,  $V_{CC2}=5V$ ,  $T_A=27^\circ C$ , (Min/Max specs are over recommended operating conditions unless otherwise noted)

| PARAMETER           |  | TEST CONDITIONS  | MIN  | TYP   | MAX       | UNIT        |
|---------------------|--|--|------|---|-----------|-------------|
| $ V_{OD} $          | Driver differential-output voltage magnitude                         | $I_O = 0$ mA, no load  | 3    | 4.3   | $V_{CC2}$ | V           |
|                     |  | $R_L = 54 \Omega$ , See Figure 11  | 1.5  | 2.3   |           | V           |
|                     |  | $R_L = 100 \Omega$ (RS-422), See Figure 11   | 2    | 2.3   |           | V           |
|                     |  | $V_{test}$ from $-7$ V to $+12$ V, See Figure 12   | 1.5  |   |           | V           |
| $\Delta V_{OD} $    | Change in differential output voltage between two states             | See Figure 11 and Figure 12  | -200 |   | 200       | mV          |
| $V_{OC}$            | Common-mode output voltage   | See Figure 13  | 1    | 2.6   | 3         | V           |
| $\Delta V_{OC(SS)}$ | change in steady-state common-mode output voltage between two states | See Figure 13  | -100 |   | 100       | mV          |
| $V_{OC(PP)}$        | Peak-to-peak common-mode output voltage                              | See Figure 13  |      | 0.5   |           | V           |
| $I_I$               | Input current  | D, DE, $V_I$ at 0 V or $V_{CC1}$   | -10  |   | 10        | $\mu A$     |
| $I_{OZ}$            | High-impedance state output current                                  | ISO3082, ISO3088   |      | See the receiver bias input current parameter |           |             |
|                     |  | ISO3080, ISO3086; $V_Y$ or $V_Z = 12$ V, $V_{CC} = 0$ V or 5 V, DE = 0 V, Other input at 0 V |      |   | 1         | $\mu A$     |
|                     |  | ISO3080, ISO3086; $V_Y$ or $V_Z = -7$ V, $V_{CC} = 0$ V or 5 V, DE = 0 V, Other input at 0 V | -1   |   |           | $\mu A$     |
| $I_{OS}$            | Short-circuit output current   | $V_A$ or $V_B$ at $-7$ V, Other input at 0 V   | -200 |   | 200       | mA          |
|                     |  | $V_A$ or $V_B$ at 12 V, Other input at 0 V   | -200 |   | 200       | mA          |
| CMTI                | Common-mode transient immunity                                       | $V_I = V_{CC}$ or 0 V, See Figure 14 and Figure 15   | 25   | 50  |           | kV/ $\mu s$ |

## 6.9 Electrical Characteristics: Receiver

All typical specs are at  $V_{CC1}=3.3V$ ,  $V_{CC2}=5V$ ,  $T_A=27^\circ C$ , (Min/Max specs are over recommended operating conditions unless otherwise noted)

| PARAMETER  |  | TEST CONDITIONS                                   | MIN             | TYP  | MAX | UNIT    |
|------------|--|---|-----------------|------|-----|---------|
| $V_{IT+}$  | Positive-going input threshold voltage     | $I_O = -8$ mA                                     |                 | -85  | -10 | mV      |
| $V_{IT-}$  | Negative-going input threshold voltage     | $I_O = 8$ mA                                      | -200            | -115 |     | mV      |
| $V_{hys}$  | Input hysteresis ( $V_{IT+} - V_{IT-}$ )   |   |                 | 30   |     | mV      |
| $V_{OH}$   | High-level output voltage                  | $V_{ID} = 200$ mV, $I_O = -8$ mA, 3.3 V $V_{CC1}$ | $V_{CC1} - 0.4$ | 3.1  |     | V       |
|            | High-level output voltage                  | $V_{ID} = 200$ mV, $I_O = -8$ mA, 5 V $V_{CC1}$   | 4               | 4.8  |     | V       |
| $V_{OL}$   | Low-level output voltage                   | $V_{ID} = -200$ mV, $I_O = 8$ mA, 3.3 V $V_{CC1}$ |                 | 0.15 | 0.4 | V       |
|            | Low-level output voltage                   | $V_{ID} = -200$ mV, $I_O = 8$ mA, 5 V $V_{CC1}$   |                 | 0.15 | 0.4 | V       |
| $I_{O(Z)}$ | Output high-impedance current on the R pin | $V_I = -7$ to 12 V, Other input = 0 V             | -1              |      | 1   | $\mu A$ |



All typical specs are at  $V_{CC1}=3.3V$ ,  $V_{CC2}=5V$ ,  $T_A=27^{\circ}C$ , (Min/Max specs are over recommended operating conditions unless otherwise noted)

| PARAMETER |                                | TEST CONDITIONS   | MIN   | TYP   | MAX  | UNIT          |
|-----------|--------------------------------|---|-------|-------|------|---------------|
| $I_I$     | Bus input current              | $V_A$ or $V_B = 12\text{ V}$ , Other input at 0 V   |       | 0.04  | 0.1  | mA            |
|           |                                | $V_A$ or $V_B = 12\text{ V}$ , $V_{CC} = 0$ , Other input at 0 V                                      |       | 0.06  | 0.13 | mA            |
|           |                                | $V_A$ or $V_B = -7\text{ V}$ , Other input at 0 V   | -0.1  | -0.04 |      | mA            |
|           |                                | $V_A$ or $V_B = -7\text{ V}$ , $V_{CC} = 0$ , Other input at 0 V                                      | -0.05 | -0.03 |      | mA            |
| $I_{IH}$  | High-level input current, RE   | $V_{IH} = 2\text{ V}$   | -10   |       | 10   | $\mu\text{A}$ |
| $I_{IL}$  | Low-level input current, RE    | $V_{IL} = 0.8\text{ V}$   | -10   |       | 10   | $\mu\text{A}$ |
| $R_{ID}$  | Differential input resistance  | A, B  | 48    |       |      | kohm          |
| $C_{ID}$  | Differential input capacitance | Test input signal is a 1.5-MHz sine wave with 1- $V_{PP}$ amplitude. $C_D$ is measured across A and B |       | 16    |      | pF            |
| $C_I$     | Input capacitance to ground    | $V_I = 0.4 \sin(4E6\pi t)$  |       | 8     |      | pF            |

## 6.10 Supply Current

Bus loaded or unloaded (over recommended operating conditions unless otherwise noted)

| PARAMETER                                | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |
|--|---|-----|-----|-----|------|
| <b>DRIVER ENABLED, RECEIVER DISABLED</b> |   |     |     |     |      |
| I <sub>CC1</sub>                         | Logic-side supply current, $\overline{RE}$ at 0 V or V <sub>CC</sub> , DE at 0 V or V <sub>CC1</sub> , 3.3-V V <sub>CC1</sub> |     |     | 8   | mA   |
|  | Logic-side supply current, $\overline{RE}$ at 0 V or V <sub>CC</sub> , DE at 0 V or V <sub>CC1</sub> , 5-V V <sub>CC1</sub>   |     |     | 10  | mA   |
| I <sub>CC2</sub>                         | Bus-side supply current, $\overline{RE}$ at 0 V or V <sub>CC</sub> , DE at 0 V, No load                                       |     |     | 15  | mA   |

## 6.11 Switching Characteristics: Driver

| PARAMETER                           |   | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|-------------------------------------|---|--|-----|-----|-----|------|
| <b>ALL DEVICES</b>                  |   |  |     |     |     |      |
| t <sub>PHL</sub> , t <sub>PLH</sub> | Propagation delay   | ISO3080/82, See Figure 14  |     | 0.7 | 1.3 | μs   |
|                                     |   | ISO3086/88, See Figure 14  |     | 25  | 45  | ns   |
| PWD                                 | Pulse width distortion <sup>(1)</sup> ,  t <sub>PHL</sub> – t <sub>PLH</sub>                  | ISO3080/82, See Figure 14  |     | 20  | 200 | ns   |
|                                     |   | ISO3086/88, See Figure 14  |     | 3   | 9   | ns   |
| t <sub>r</sub> , t <sub>f</sub>     | Differential output rise time and fall time   | ISO3080/82, See Figure 14  | 0.5 | 0.9 | 1.5 | μs   |
|                                     |   | ISO3086/88, See Figure 14  |     | 7   | 15  | ns   |
| t <sub>PZH</sub> , t <sub>PZL</sub> | Propagation delay, high-impedance-to-high-level output and high-impedance-to-low-level output | ISO3080/82, See Figure 15 and Figure 16, DE at 0 V, 50% V <sub>o</sub> |     | 2.5 | 7   | μs   |
|                                     |   | ISO3080/82, See Figure 15 and Figure 16, DE at 0 V, 90% V <sub>o</sub> |     | 1.8 |     | μs   |
|                                     |   | ISO3086/88, See Figure 15 and 16                                       |     | 25  | 55  | ns   |
| t <sub>PHZ</sub> , t <sub>PLZ</sub> | Propagation delay, high-level-to-highimpedance output and low-level to highimpedance output   | ISO3080/28, See Figure 15 and 16                                       |     | 95  | 225 | ns   |
|                                     |   | ISO3086/88, See Figure 15 and 16                                       |     | 25  | 55  | ns   |

(1) Also known as pulse skew.

## 6.12 Switching Characteristics: Receiver

All typical specs are at V<sub>CC1</sub>=3.3V, V<sub>CC2</sub>=5V, T<sub>A</sub>=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

| PARAMETER                           |  | TEST CONDITIONS          | MIN | TYP | MAX | UNIT |
|-------------------------------------|--|--------------------------|-----|-----|-----|------|
| <b>ALL DEVICES</b>                  |  |                          |     |     |     |      |
| t <sub>r</sub> , t <sub>f</sub>     | Differential output rise time and fall time  | See Figure 18            |     | 1   |     | ns   |
| t <sub>PHL</sub> , t <sub>PLH</sub> | Propagation delay  |                          |     | 90  | 125 | ns   |
| PWD                                 | Pulse width distortion <sup>(1)</sup> ,  t <sub>PHL</sub> – t <sub>PLH</sub>                 | ISO3080/82 See Figure 18 |     | 4   | 20  | ns   |
| PWD                                 | Pulse width distortion <sup>(1)</sup>  t <sub>PHL</sub> – t <sub>PLH</sub>                   | ISO3086/88 See Figure 18 |     | 4   | 12  | ns   |
| t <sub>PHZ</sub> , t <sub>PZH</sub> | Propagation delay, high-level-tohigh-impedance output and highimpedance-to-high-level output | See Figure 19            |     |     | 22  | ns   |
| t <sub>PZL</sub> , t <sub>PLZ</sub> | Propagation delay, highimpedance-to-low-level output and low-level-to-high-impedance output  | See Figure 20            |     |     | 22  | ns   |

(1) Also known as pulse skew

### 6.13 Insulation Characteristics Curves

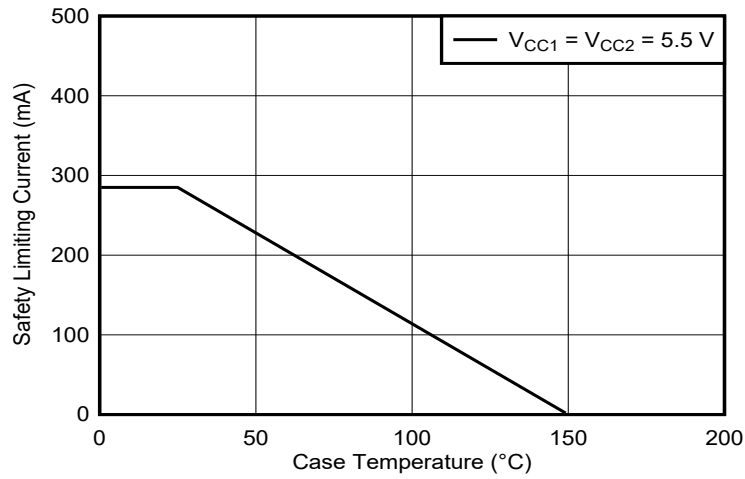


Figure 6-1. Thermal Derating Curve for Limiting Current per VDE

## 6.14 Typical Characteristics

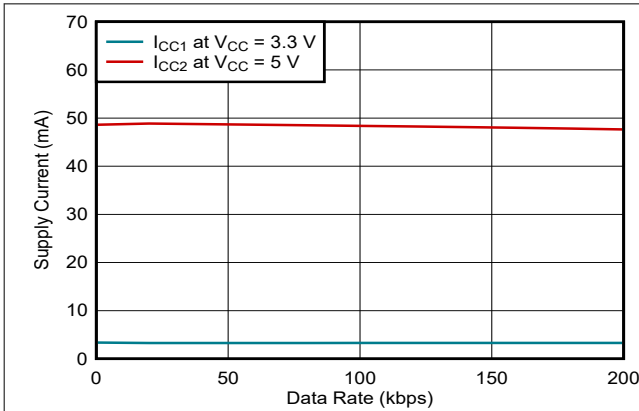


Figure 6-2. ISO3080 Supply Current vs Data Rate With Load

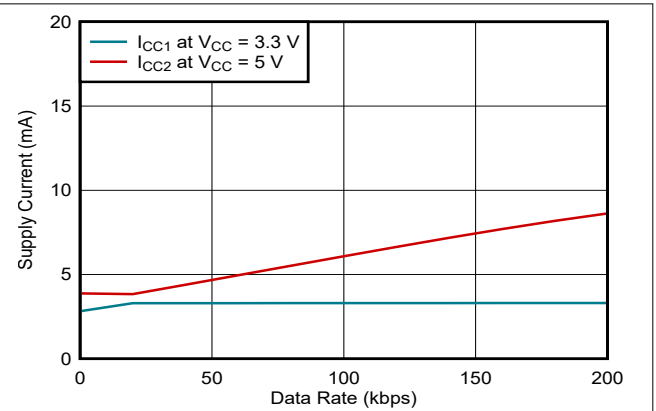


Figure 6-3. ISO3080 Supply Current vs Data Rate With No Load

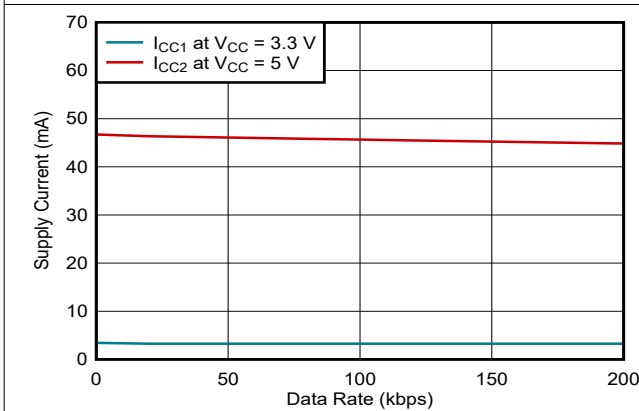


Figure 6-4. ISO3082 Supply Current vs Data Rate With Load

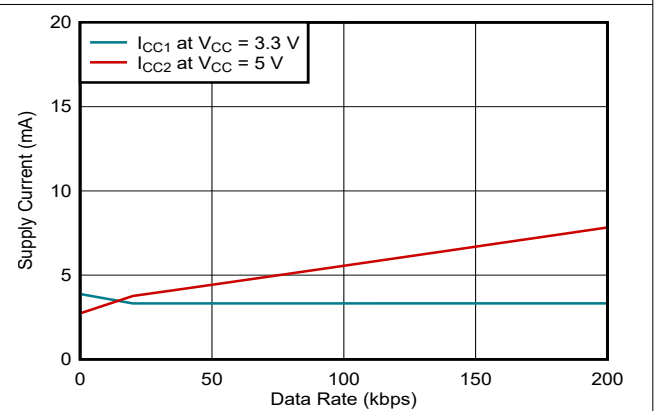


Figure 6-5. ISO3082 Supply Current vs Data Rate With No Load

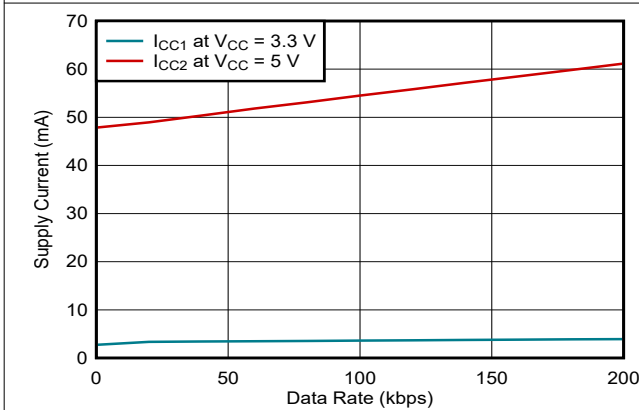


Figure 6-6. ISO3086 Supply Current vs Data Rate With Load

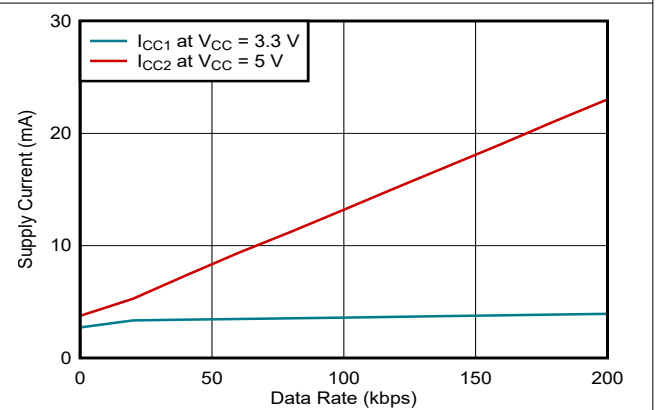


Figure 6-7. ISO3086 Supply Current vs Data Rate With No Load

### 6.14 Typical Characteristics (continued)

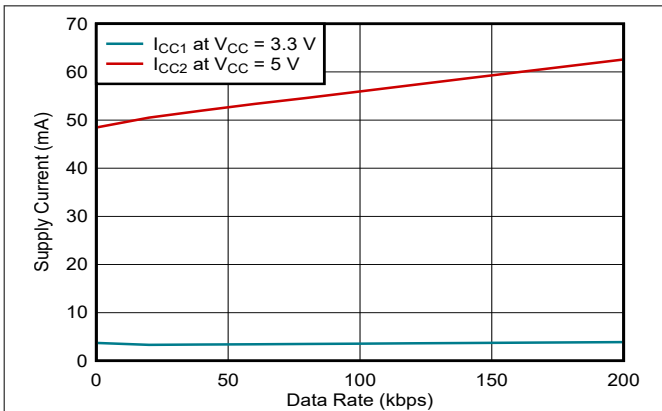


Figure 6-8. ISO3088 Supply Current vs Data Rate With Load

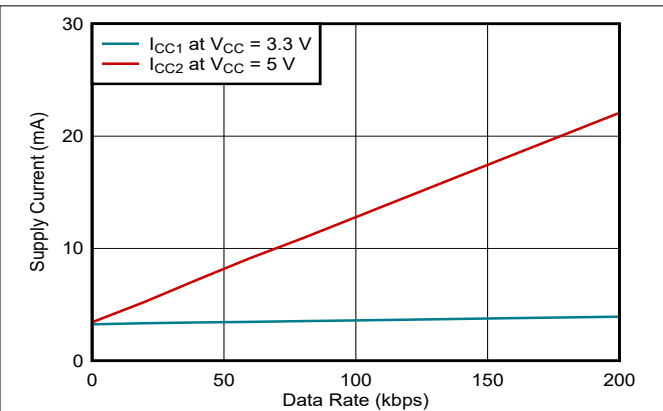


Figure 6-9. ISO3088 Supply Current vs Data Rate With No Load

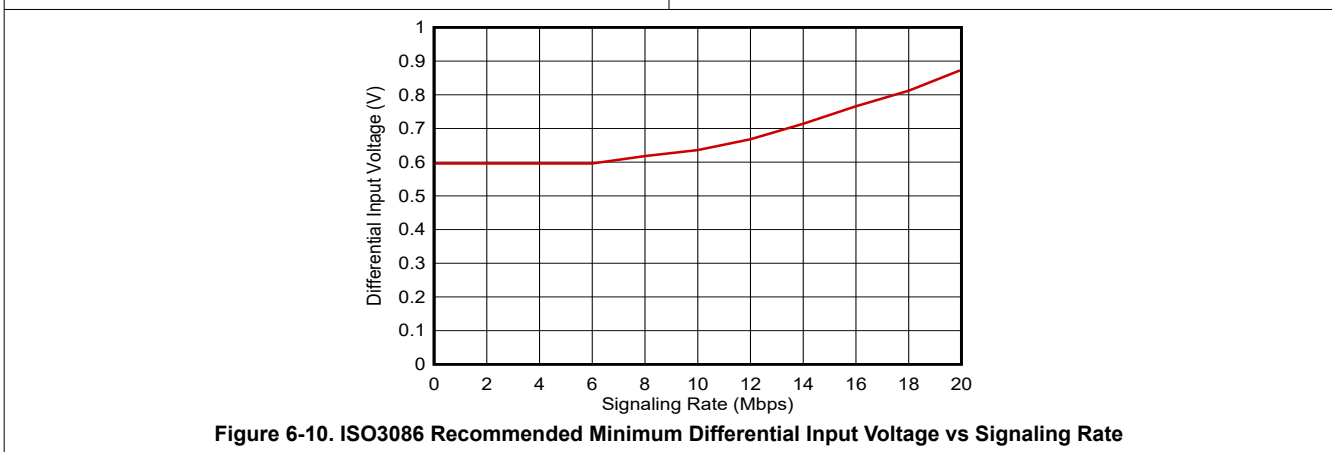


Figure 6-10. ISO3086 Recommended Minimum Differential Input Voltage vs Signaling Rate

## 7 Parameter Measurement Information

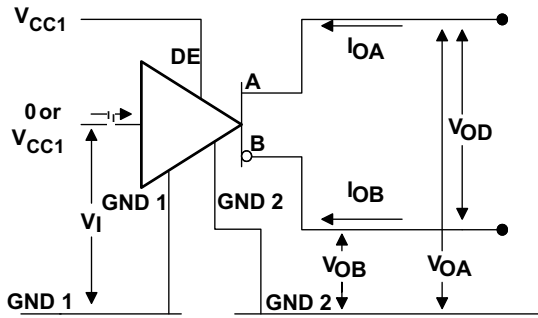


Figure 7-1. Driver  $V_{OD}$  Test and Current Definitions

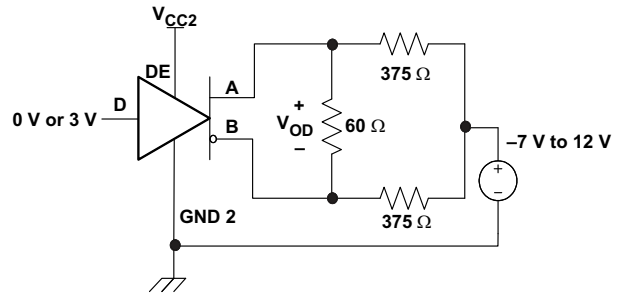


Figure 7-2. Driver  $V_{OD}$  With Common-Mode Loading Test Circuit

### Note

Unless otherwise stated, test circuits are shown for half-duplex devices, ISO3082 and ISO3088. For full-duplex devices, the driver output pins are Y and Z.

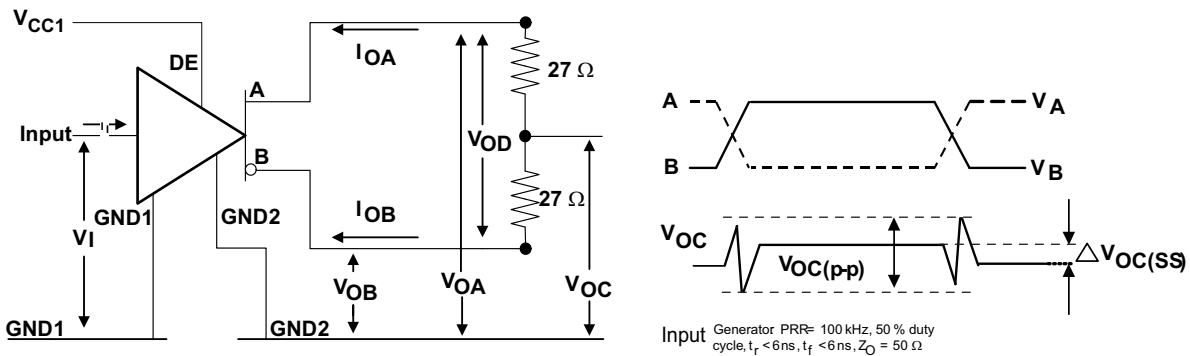


Figure 7-3. Test Circuit and Waveform Definitions For The Driver Common-Mode Output Voltage

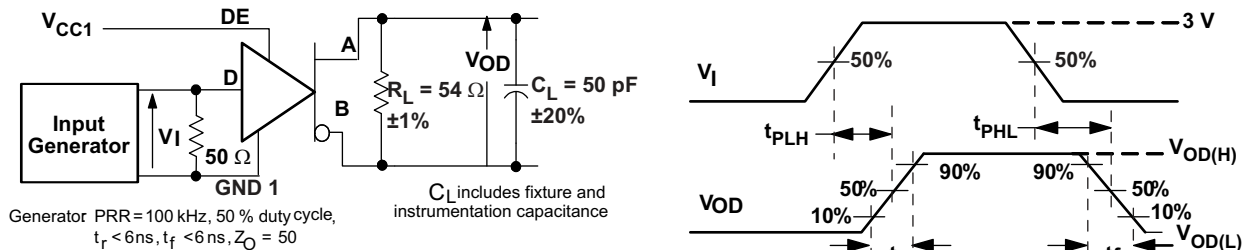


Figure 7-4. Driver Switching Test Circuit and Voltage Waveforms

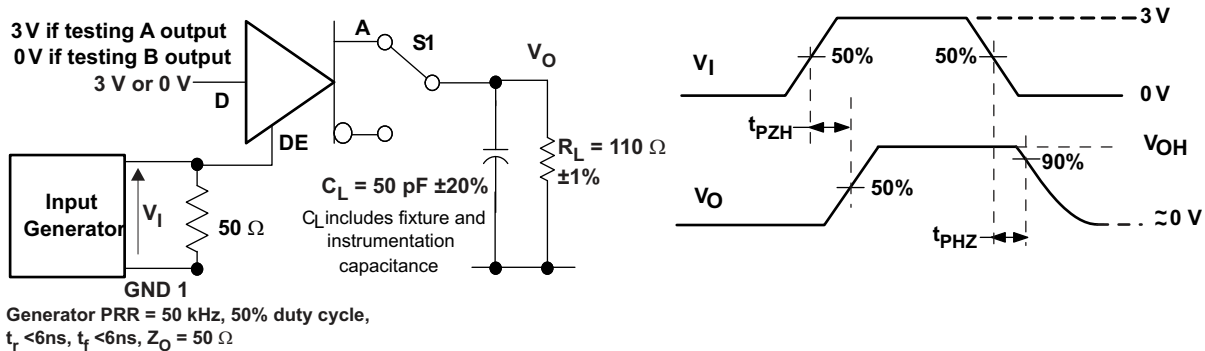


Figure 7-5. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

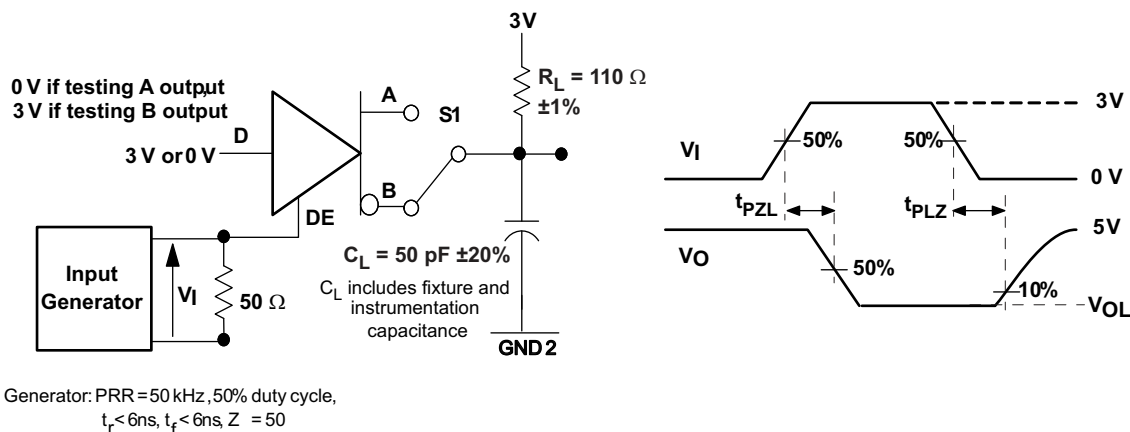


Figure 7-6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveform

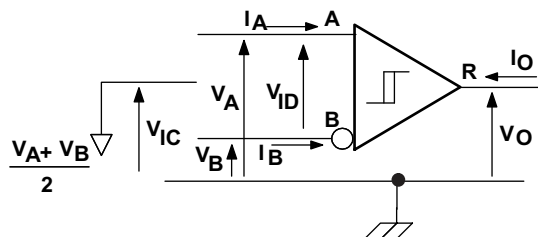


Figure 7-7. Receiver Voltage and Current Definitions

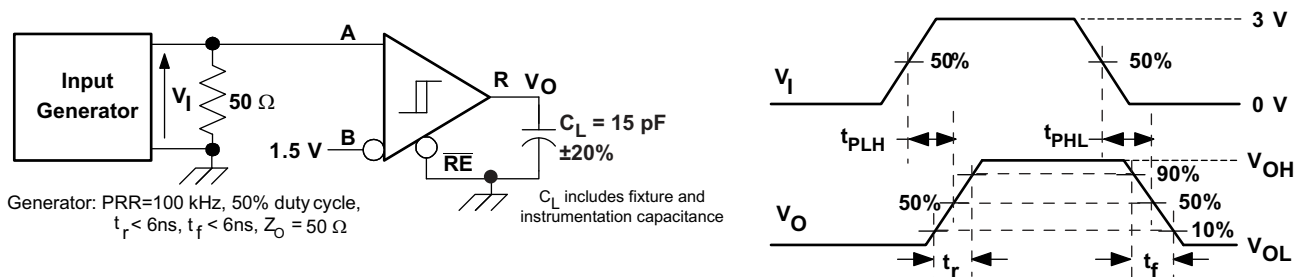


Figure 7-8. Receiver Switching Test Circuit and Waveforms



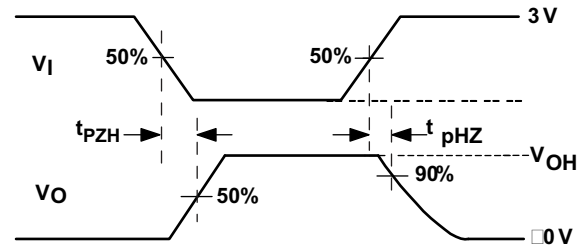
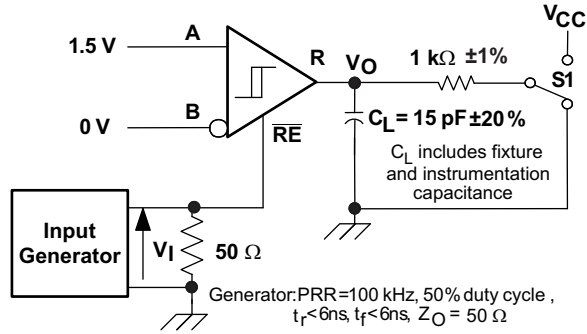


Figure 7-9. Receiver Enable Test Circuit and Waveforms, Data Output High

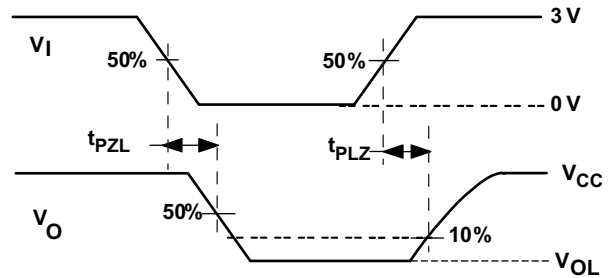
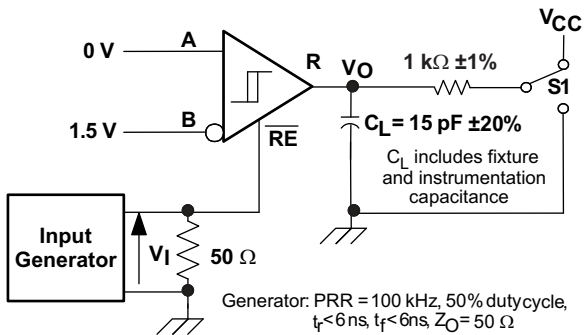
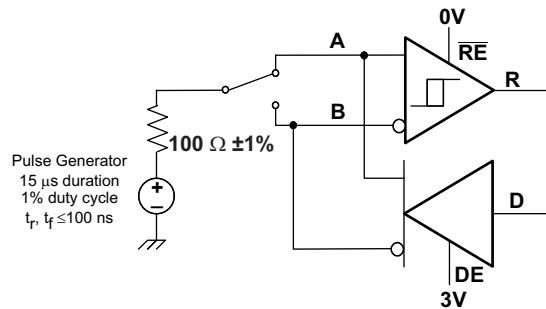


Figure 7-10. Receiver Enable Test Circuit and Waveforms, Data Output Low



Note: This test is conducted to test survivability only.  
Data stability at the R output is not specified.

Figure 7-11. Transient Overvoltage Test Circuit

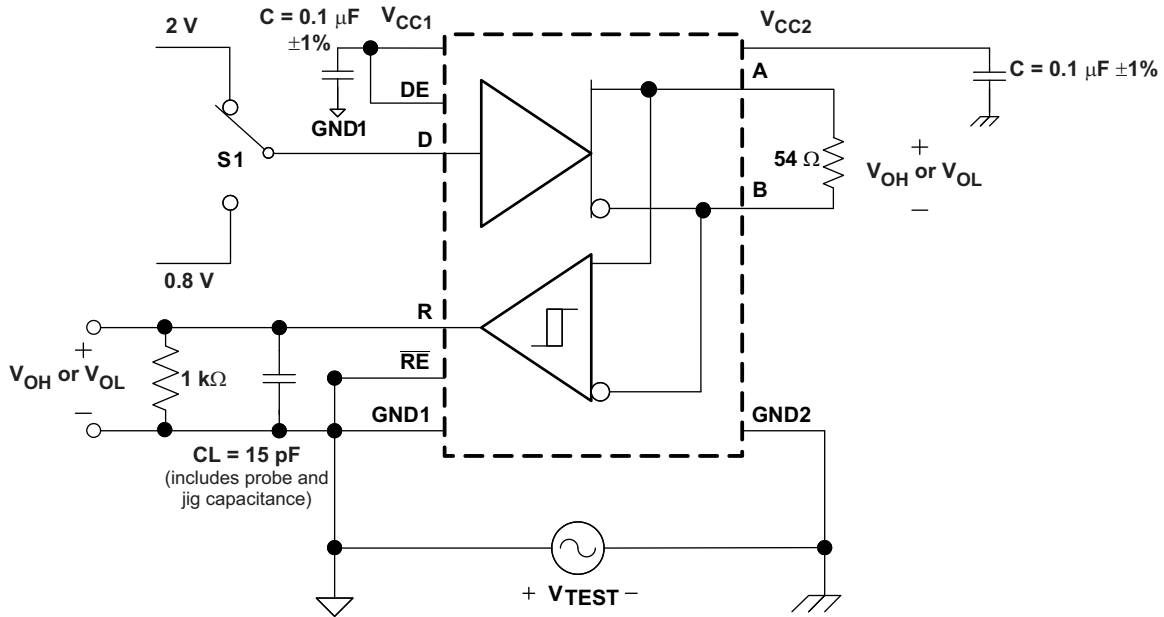


Figure 7-12. Half-Duplex Common-Mode Transient Immunity Test Circuit

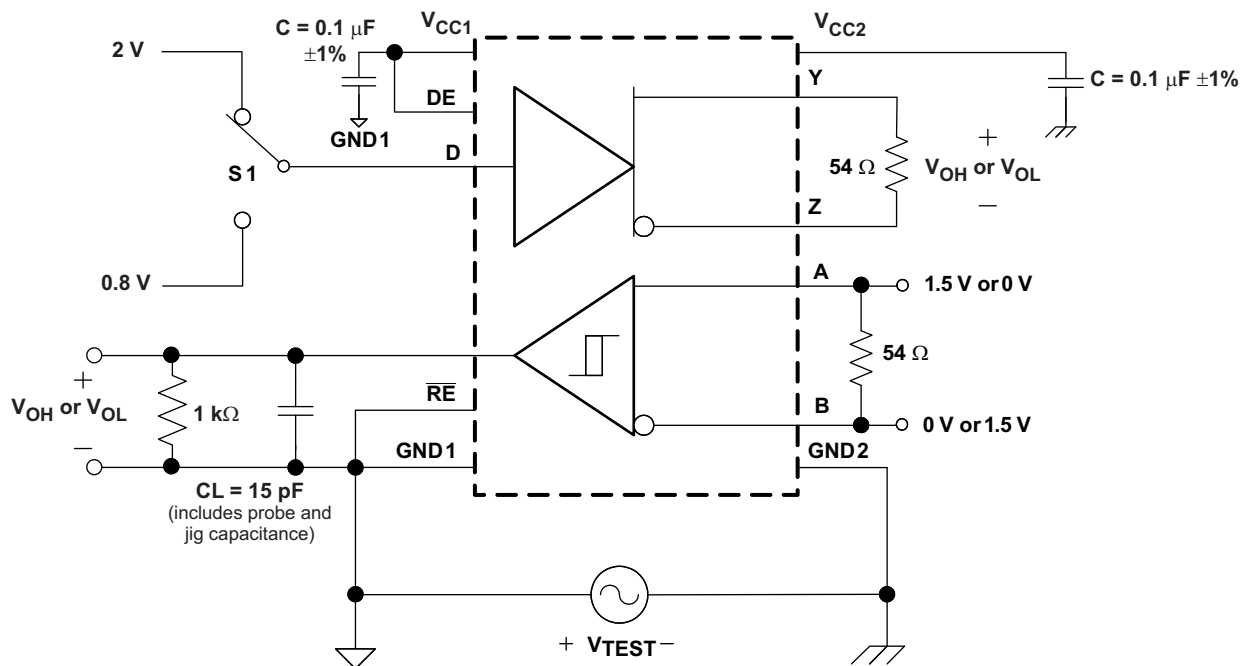


Figure 7-13. Full-Duplex Common-Mode Transient Immunity Test Circuit

## 8 Detailed Description

### 8.1 Overview

The ISO3080 and ISO3086 devices are isolated full-duplex differential line drivers and receivers while the ISO3082 and ISO3088 devices are isolated half-duplex differential line transceivers for TIA/EIA 485/422 applications. They are rated to provide galvanic isolation of up to 2500  $V_{RMS}$  for 60 s as per the standard. They have active-high driver enables and active-low receiver enables to control the data flow. They are available in two speed grades suitable for data transmission up to 200 kbps and 20 Mbps.

When the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as  $V_{OD} = V_{(Y)} - V_{(Z)}$  is positive. When D is low, the output states reverse, Z turns high, Y becomes low, and  $V_{OD}$  is negative. When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to  $V_{CC}$ , thus, when left open while the driver is enabled, output Y turns high and Z turns low.

When the receiver enable pin, RE, is logic low, the receiver is enabled. When the differential input voltage defined as  $V_{ID} = V_{(A)} - V_{(B)}$  is positive and higher than the positive input threshold,  $V_{IT+}$ , the receiver output, R, turns high. When  $V_{ID}$  is negative and less than the negative and lower than the negative input threshold,  $V_{IT-}$ , the receiver output, R, turns low. If  $V_{ID}$  is between  $V_{IT+}$  and  $V_{IT-}$  the output is indeterminate. When RE is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of  $V_{ID}$  are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

### 8.2 Functional Block Diagrams

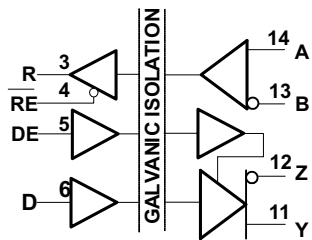


Figure 8-1. ISO3080, IOS3086 Functional Diagram

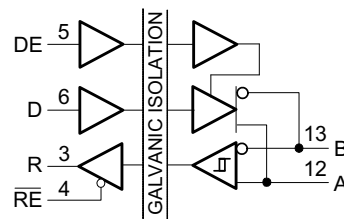


Figure 8-2. ISO3082, IOS3088 Functional Diagram

## 8.3 Feature Description

Table 8-1 provides an overview of the device features.

**Table 8-1. Device Features**

| DEVICE  | RATED ISOLATION <sup>(1)</sup>               | TYPE        | DATA RATE |
|---------|--|-------------|-----------|
| ISO3080 | 4000 V <sub>PK</sub> / 2500 V <sub>RMS</sub> | Full-duplex | 200 kbps  |
| ISO3086 | 4000 V <sub>PK</sub> / 2500 V <sub>RMS</sub> | Full-duplex | 20 Mbps   |
| ISO3082 | 4000 V <sub>PK</sub> / 2500 V <sub>RMS</sub> | Half-duplex | 200 kbps  |
| ISO3088 | 4000 V <sub>PK</sub> / 2500 V <sub>RMS</sub> | Half-duplex | 20 Mbps   |

(1) See *Safety-Related Certifications* table for detailed isolation ratings.

## 8.4 Device Functional Modes

Table 8-2 lists the driver functional modes and Table 8-3 lists the receiver functional modes.

**Table 8-2. Driver Function Table<sup>(1)</sup>**

| V <sub>CC1</sub> | V <sub>CC2</sub> | INPUT (D) | ENABLE INPUT (DE) | OUTPUTS <sup>(1)</sup> |       |
|------------------|------------------|-----------|-------------------|------------------------|-------|
|                  |                  |           |                   | Y / A                  | Z / B |
| PU               | PU               | H         | H                 | H                      | L     |
| PU               | PU               | L         | H                 | L                      | H     |
| PU               | PU               | X         | L                 | Hi-Z                   | Hi-Z  |
| PU               | PU               | X         | OPEN              | Hi-Z                   | Hi-Z  |
| PU               | PU               | OPEN      | H                 | H                      | L     |
| PD               | PU               | X         | X                 | Hi-Z                   | Hi-Z  |
| PU               | PD               | X         | X                 | Hi-Z                   | Hi-Z  |
| PD               | PD               | X         | X                 | Hi-Z                   | Hi-Z  |

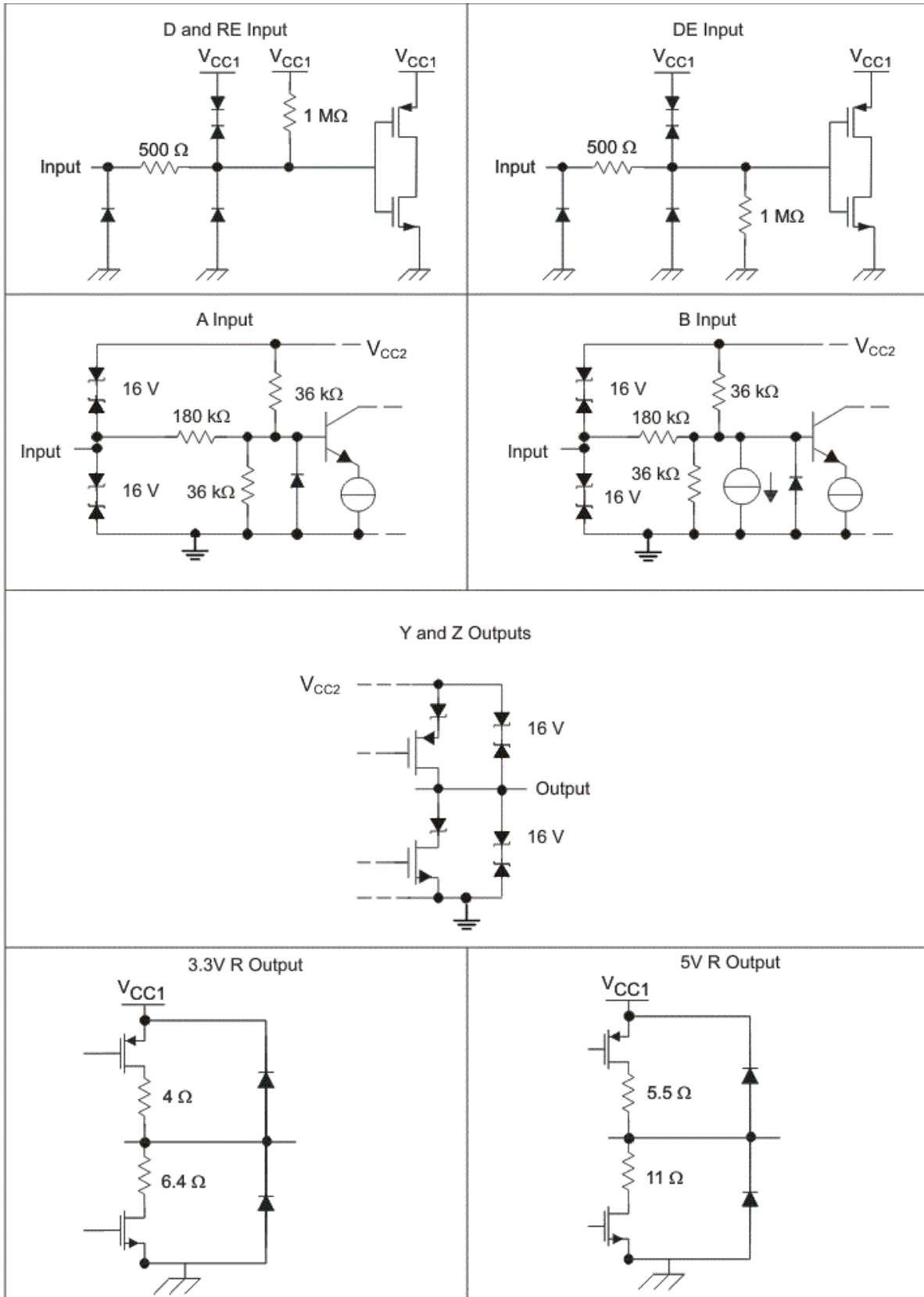
(1) Driver output pins are Y and Z for full-duplex devices and A and B for half-duplex devices.

**Table 8-3. Receiver Function Table<sup>(1)</sup>**

| V <sub>CC1</sub> | V <sub>CC2</sub> | DIFFERENTIAL INPUT<br>V <sub>ID</sub> = (V <sub>A</sub> – V <sub>B</sub> ) | ENABLE (RE) | OUTPUT (R) |
|------------------|------------------|--|-------------|------------|
| PU               | PU               | -0.01 V ≤ V <sub>ID</sub>  | L           | H          |
| PU               | PU               | -0.2 V < V <sub>ID</sub> < -0.01 V   | L           | ?          |
| PU               | PU               | V <sub>ID</sub> ≤ -0.2 V   | L           | L          |
| PU               | PU               | X  | H           | Hi-Z       |
| PU               | PU               | X  | OPEN        | Hi-Z       |
| PU               | PU               | Open circuit   | L           | H          |
| PU               | PU               | Short circuit  | L           | H          |
| PU               | PU               | Idle (terminated) bus  | L           | H          |
| PD               | PU               | X  | X           | Hi-Z       |
| PU               | PD               | X  | L           | H          |

(1) PU = Powered Up; PD = Powered Down; H = Logic High; L = Logic Low; X = Irrelevant, Hi-Z = High Impedance (off), ? = Indeterminate

### 8.4.1 Device I/O Schematics



**Figure 8-3. Device I/O Schematics**

## 9 Application and Implementation

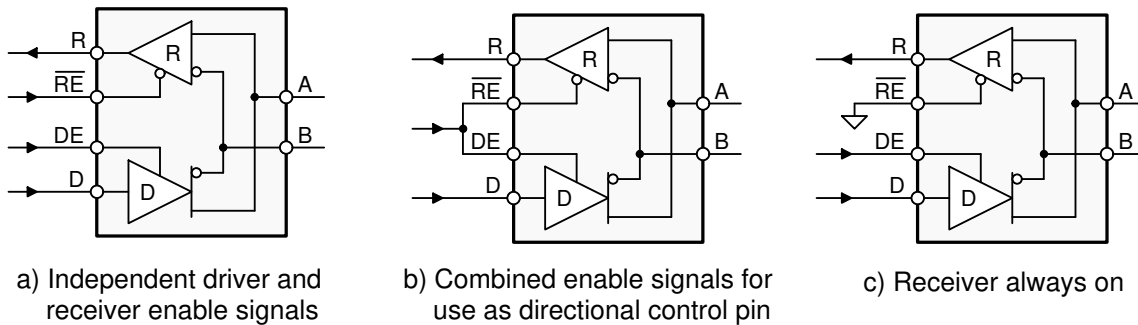
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

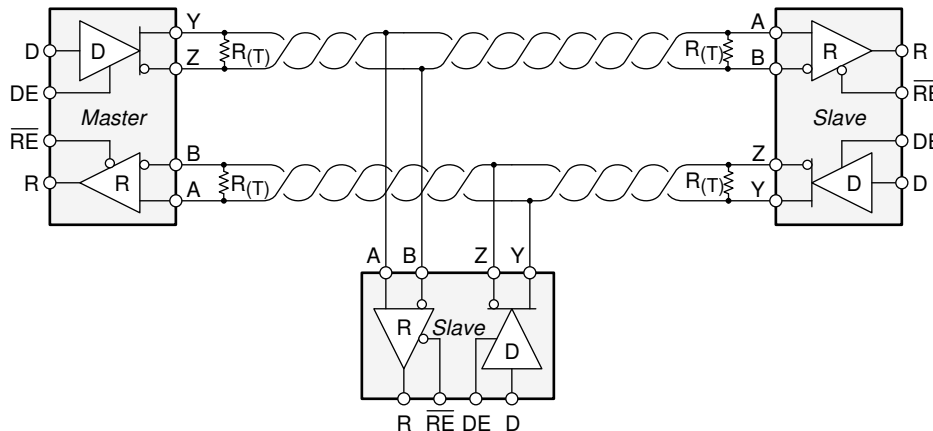
The ISO308x family consists of RS-485 transceivers commonly used for asynchronous data transmissions. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair. For half-duplex transmission, only one pair is shared for both transmission and reception of data. To eliminate line reflections, each cable end is terminated with a termination resistor,  $R_{(T)}$ , whose value matches the characteristic impedance,  $Z_0$ , of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

### 9.2 Typical Application



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**Figure 9-1. Half-Duplex Transceiver Configurations**



**Figure 9-2. Typical RS-485 Network With Full-Duplex Transceivers**

### 9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that can be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes. [Table 9-1](#) lists the design parameters.

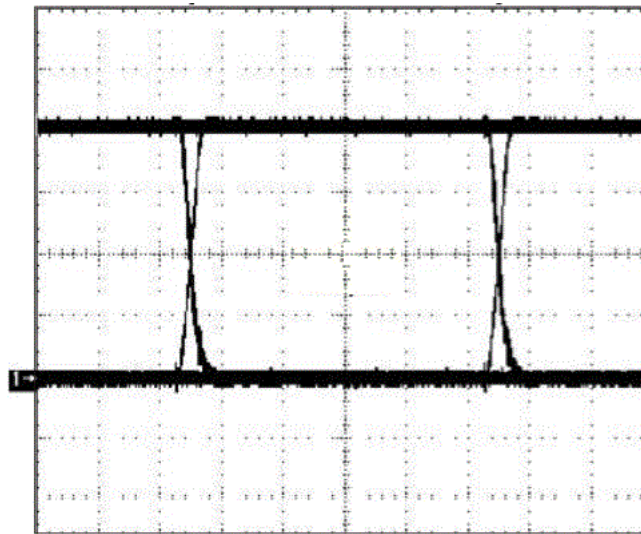
**Table 9-1. Design Parameters**

| PARAMETER                     | VALUE         |
|-------------------------------|---------------|
| Pullup and pulldown resistors | 1 kΩ to 10 kΩ |
| Decoupling capacitors         | 100 nF        |

### 9.2.2 Detailed Design Procedure

The data rate and cable length have an inverse relationship which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a nonterminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver. The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (ULs), where 1 UL represents a load impedance of approximately 12 kΩ. Because the ISO308x family consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

### 9.2.3 Application Curve



**Figure 9-3. ISO308x Output**

## 10 Power Supply Recommendations

To help ensure reliable operation at all data rates and supply voltages, a 0.1- $\mu$ F bypass capacitor is recommended at the input and output supply pins ( $V_{CC1}$  and  $V_{CC2}$ ). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' [SN6501](#). For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501 Transformer Driver for Isolated Power Supplies](#).

## 11 Layout

### 11.1 Layout Guidelines

ON-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design. A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 11-1](#)).

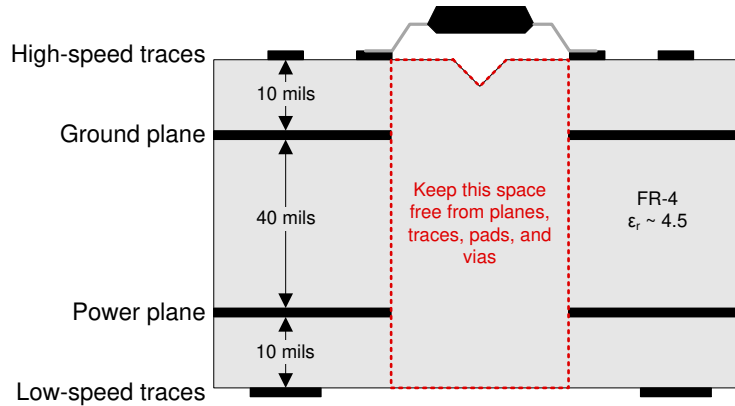
- Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.
- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in<sup>2</sup>.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
- Use  $V_{CC}$  and ground planes to provide low-inductance. High-frequency currents might follow the path of least inductance and not necessarily the path of least resistance.
- Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
- Apply 0.1- $\mu$ F bypass capacitors as close as possible to the  $V_{CC}$ -pins of transceiver, UART, and controller ICs on the board.
- Use at least two vias for  $V_{CC}$  and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
- Use 1-k $\Omega$  to 10-k $\Omega$  pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
- Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.



If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the [Digital Isolator Design Guide](#).

### 11.2 Layout Example



**Figure 11-1. Recommended Layer Stack**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- [Communication Module Reference Design for Functional Isolated RS-485, CAN, and I2C Data Transmission](#)
- [Digital Isolator Design Guide](#)
- [Dual Isolated Half-Duplex RS-485 Repeater](#)
- [Isolation Glossary](#)
- [Programmable Logic Controller \(PLC\) I/O Module Front- End Controller with Tiva C Series ARM®Cortex®-M4 MCU](#)
- [Small Form Factor, Digital Isolator-Based Half-Duplex RS- 485 Interface Module Reference Design](#)
- [SN6501 Transformer Driver for Isolated Power Supplies](#)

#### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

#### 12.4 Trademarks

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#### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

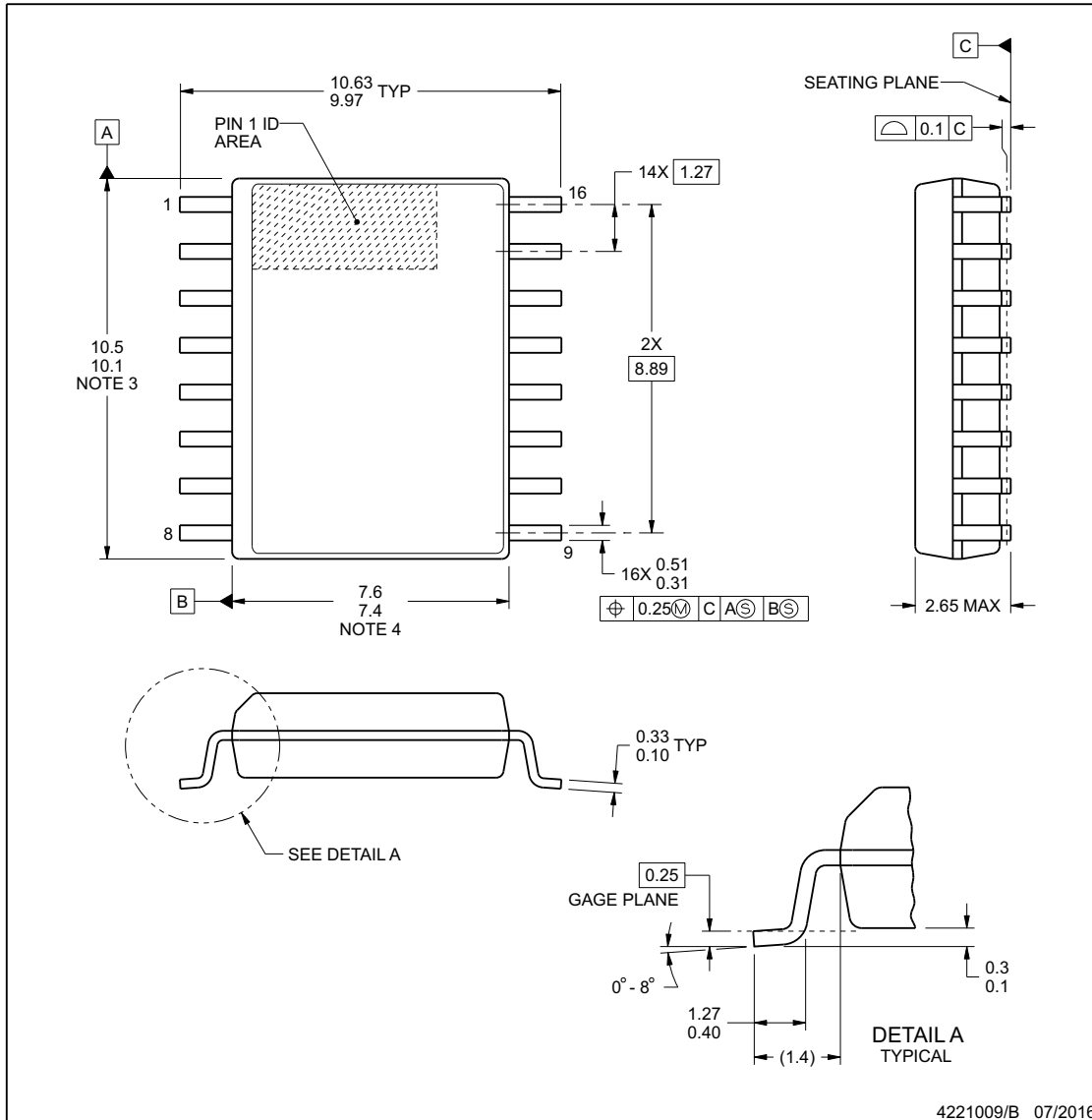
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**DW0016B**

**PACKAGE OUTLINE**  
**SOIC - 2.65 mm max height**

SOIC



**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

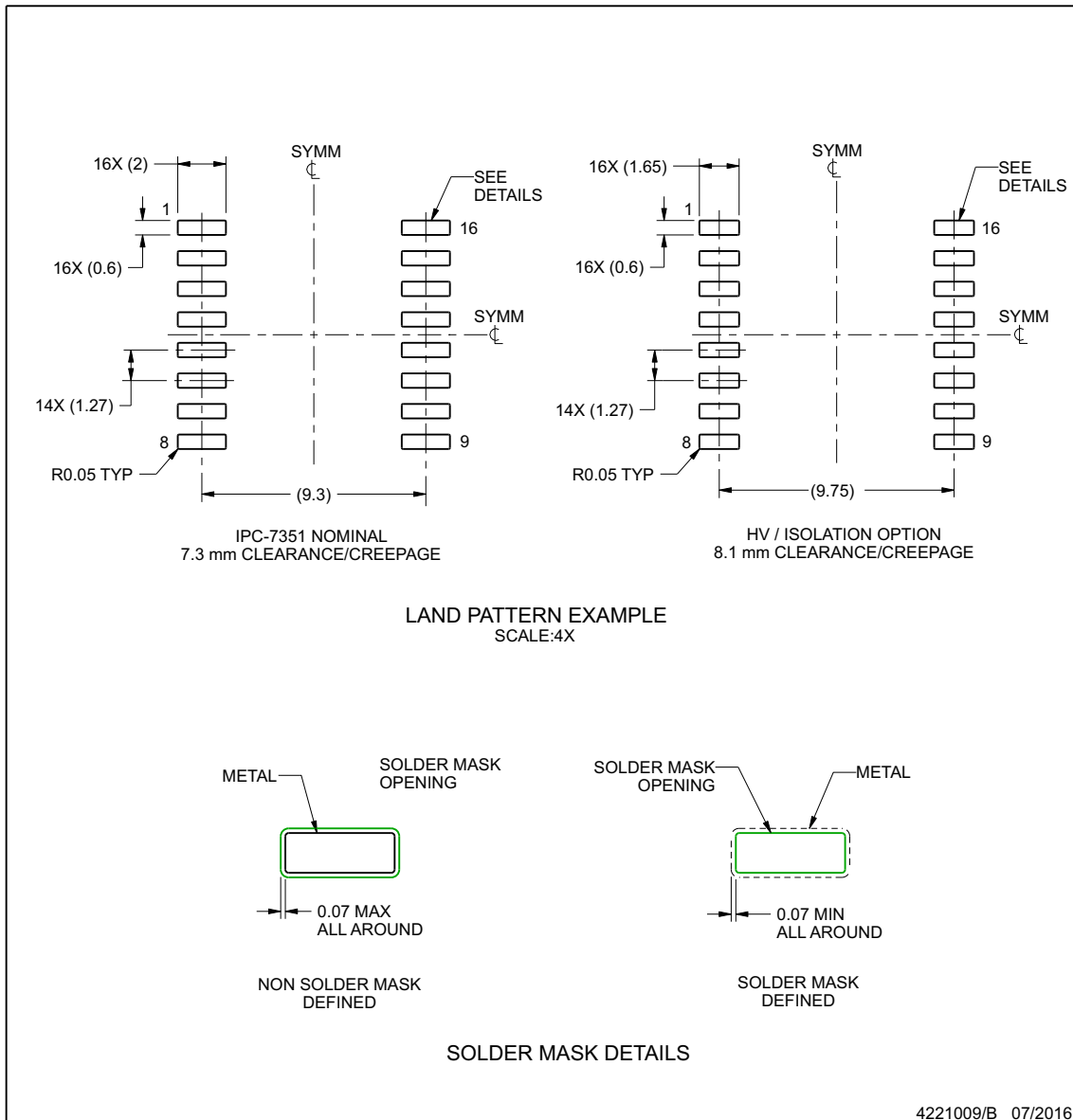
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## EXAMPLE BOARD LAYOUT

**DW0016B**

**SOIC - 2.65 mm max height**

SOIC



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

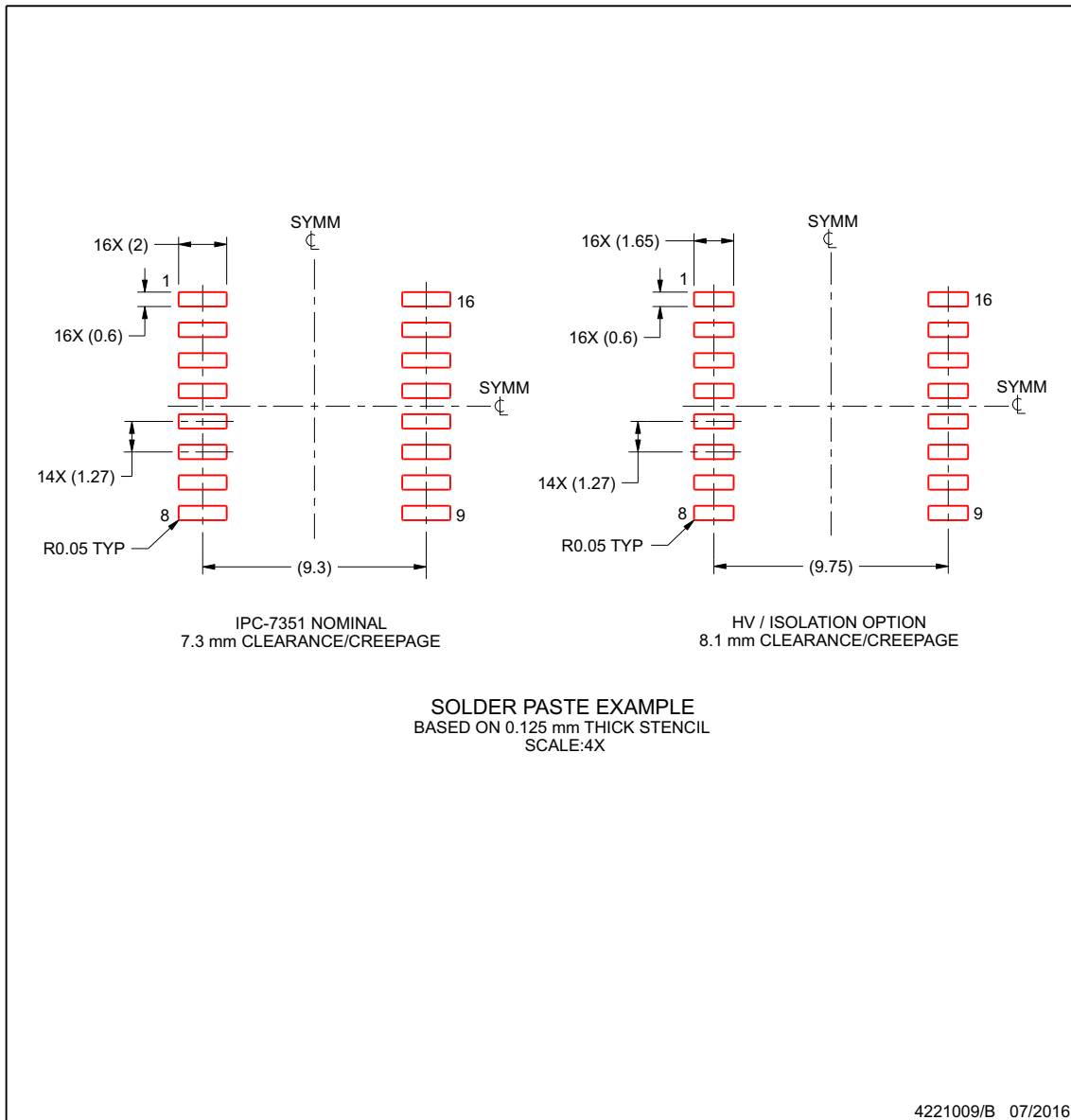
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## EXAMPLE STENCIL DESIGN

**DW0016B**

**SOIC - 2.65 mm max height**

SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| ISO3080DW        | LIFEBUY       | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | ISO3080                 |         |
| ISO3080DWG4      | LIFEBUY       | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | ISO3080                 |         |
| ISO3080DWR       | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | ISO3080                 | Samples |
| ISO3082DW        | LIFEBUY       | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | ISO3082                 |         |
| ISO3082DWG4      | LIFEBUY       | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | ISO3082                 |         |
| ISO3082DWR       | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | ISO3082                 | Samples |
| ISO3082DWRG4     | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | ISO3082                 | Samples |
| ISO3086DW        | LIFEBUY       | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | ISO3086                 |         |
| ISO3086DWG4      | LIFEBUY       | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | ISO3086                 |         |
| ISO3086DWR       | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | ISO3086                 | Samples |
| ISO3088DW        | LIFEBUY       | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | ISO3088                 |         |
| ISO3088DWG4      | LIFEBUY       | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | ISO3088                 |         |
| ISO3088DWR       | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | ISO3088                 | Samples |
| ISO3088DWRG4     | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | ISO3088                 | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

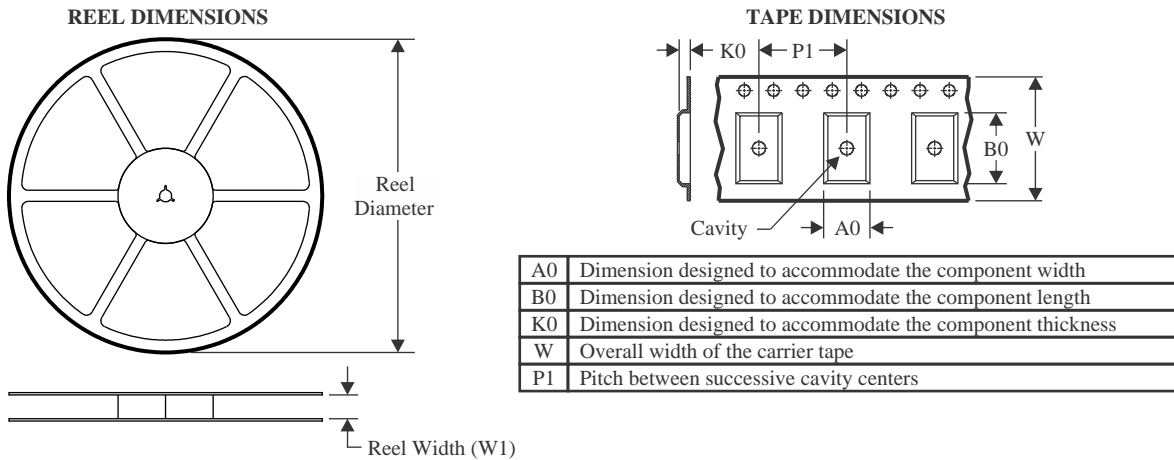
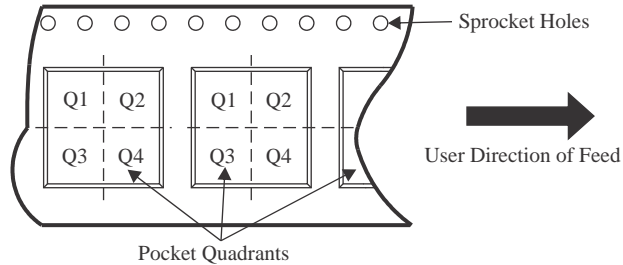
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ISO3080DWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO3082DWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO3086DWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO3088DWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |

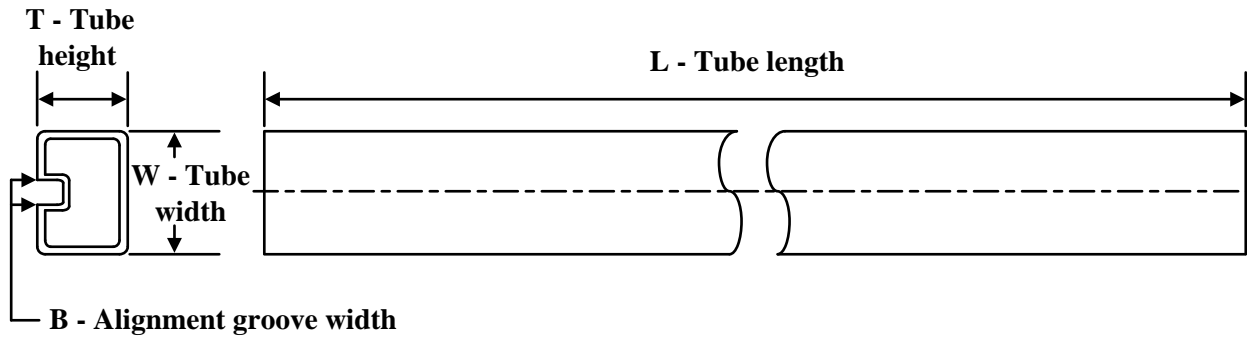


## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ISO3080DWR | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| ISO3082DWR | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| ISO3086DWR | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| ISO3088DWR | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |

**TUBE**


\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| ISO3080DW   | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO3080DWG4 | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO3082DW   | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO3082DWG4 | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO3086DW   | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO3086DWG4 | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO3088DW   | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO3088DWG4 | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |

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