3.5-GHz Integrated Up-Converter

FEATURES

- **Performs Up-Conversion in 3.5-GHz Radios (3300-3800 MHz)**
- **Integrated IF amplifier, Mixer and LO Buffer Amplifier**
- **Provision for external Image Reject / Band-Pass Filter**
- **TTL Switched Attenuator For Gain Control**
- **TTL Controlled Amplifier Power Down**

KEY SPECIFICATIONS

- **RF Frequency Range: 3300-3800 MHz**
- **18 dB of Gain with 16-dB Digital Attenuator**
- **Output P-1dB: +14 dBm, Typical**
- **Output IP3: +24 dBm, Typical**
- **LO Drive Level = 0 dBm, Typical**

DESCRIPTION

The TRF1222 up-converts a UHF IF signal to an RF signal in the 3300 to 3800 MHz range for 3.5-GHz radio applications. The TRF1222 has 18 dB of gain and an output P-1dB of 14 dBm, typical. A TTL compatible, 1-bit 16-dB digital attenuator is provided for gain control and the IF and RF amplifiers can be shut off via a TTL control signal for power critical or TDD applications. In order to provide system requirements for LO/spurious rejection, the TRF1222 offers a signal path to an off-chip band-pass filter. Specifications are provided assuming an in-band 2-dB insertion loss filter.

The TRF1222 is designed to complete the second up-conversion in Texas Instruments complete 3.5-GHz chip set. The linear nature of the up-converter makes it ideal for complex modulations schemes such as high order QAM or OFDM.

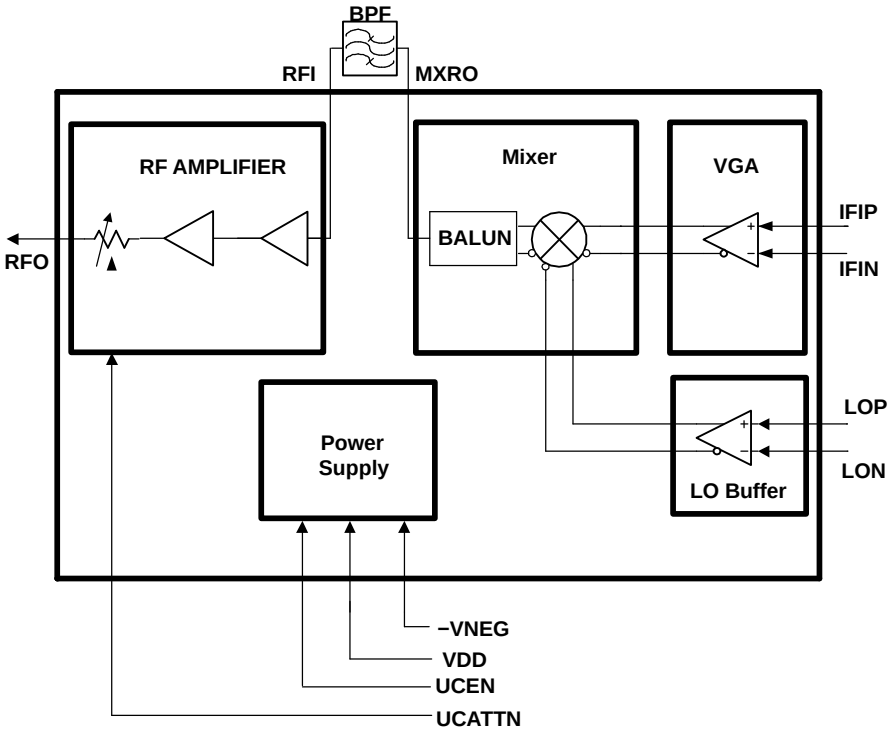

Figure 1. Block Diagram

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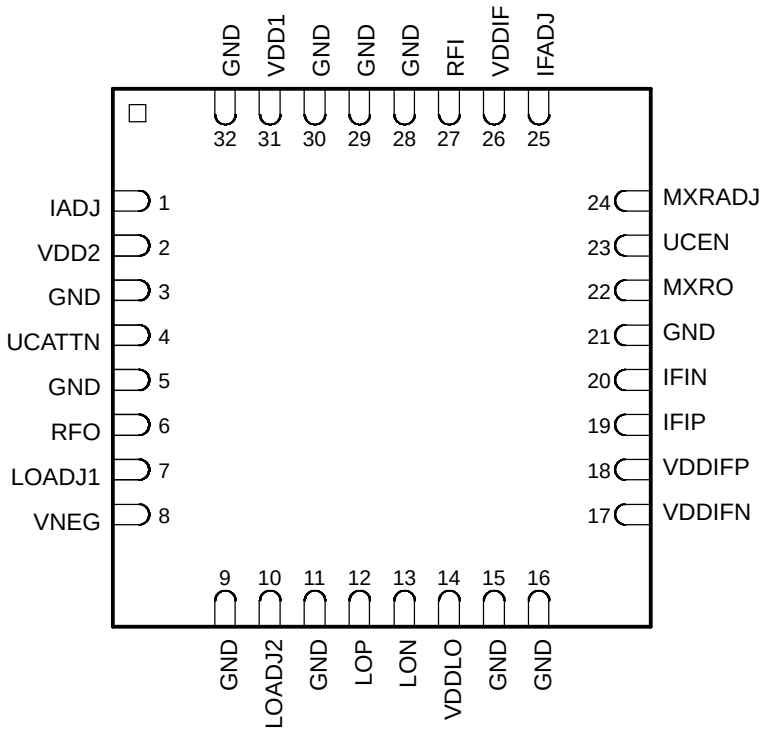
DEVICE INFORMATION

LPCC–32 PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	TYPE	DESCRIPTION
NO.	NAME			
1	IADJ			Not connected for normal operation. Amplifier bias adjustment. Do not ground this pin or connect to any other pin.
2	VDD2	I	Power	RF amplifier bias 5 V
3, 5, 9, 11, 15, 16, 21, 28,29, 30, 32	GND			Ground
4	UCATTN	I	Digital	Logic high is high gain; logic low reduces gain by 16 dB. Normally set high.
6	RFO	O	Analog	RF output from RF amplifier
7	LOADJ1			Not connected for normal operation. LO common gate bias adjustment. Do not ground this pin or connect to any other pin.
8	VNEG	I	Power	Negative bias used for enable circuitry -5 V. This pin can be grounded if the user does not use the UCEN pin to turnoff the amplifier. If the VNEG is grounded the UCEN pin should be tied high.
10	LOADJ2			Not connected for normal operation. LO amplifier bias adjustment. Do not ground this pin or connect to any other pin.
12	LOP	I	Analog	LO input, positive, internally ac-coupled
13	LON	I	Analog	LO input, negative, internally ac-coupled
14	VDDLO	I	Power	Positive power for LO amplifier, 5 V
17	VDDIFN	I	Analog	VDD supply for IF amplifier, negative, 5 V
18	VDDIFP	I	Analog	VDD supply for IF amplifier, positive, 5 V
19	IFI P	I	Analog	IF input, positive, dc-coupled, typical dc voltage is 1.2 V

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	TYPE	DESCRIPTION
NO.	NAME			
20	IFI N	I	Analog	IF input, negative, dc-coupled typical dc voltage is 1.2 V
22	MXRO	O	Analog	Output of mixer (after balun) 50-Ω impedance with high impedance dc ground.
23	UCEN	I	Digital	Set high to enable IF amplifier and RF amplifiers
24	MXRADJ	O	Analog	Normally grounded. Provide 0-Ω jumper to ground.
25	IFADJ			Not connected for normal operation. IF amplifier bias adjustment. Do not ground this pin or connect to any other pin.
26	VDDIF	I	Power	Positive supply for IF bias circuitry 5 V
27	RFI	I	Analog	Input to RF amplifier, 50-Ω impedance, internally ac-coupled
31	VDD1	I	Power	RF amplifier bias 5 V
Back	GND			Back of package has metal base that must be grounded for thermal and RF performance.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
VDD	Positive dc supply voltage	0 to 5.5	V
-VDD	Negative dc supply voltage	-5.5 to 0	V
P_{IN}	RF input power	10	dBm
T_J	Junction temperature	200	°C
P_D	Power dissipation	1	W
	Digital input pins	-0.3 to 5.5	V
θ_{jc}	Thermal resistance junction-to-case(1)	9.01	°C/W
T_{stg}	Storage temperature	-40 to 105	°C
T_{op}	Operating temperature	-40 to 85	°C
	Lead temperature (40 Sec Max)	260	°C

(1) Thermal resistance is junction to ambient assuming thermal pad with 16 thermal vias under package metal base. See the recommended PCB layout.

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
V_{DD}	Positive supply voltage		4.75	5	5.25	V
I_{DD}	Positive supply current (total)			175	200	mA
V_{NEG}	Negative supply voltage		-5.25	-5	-4.75	V
I_{NEG}	Negative supply current			3	6	mA
I_{VDD2}	Supply current RF 2, pin 2			50		mA
I_{LO}	Supply current, LO, pin 14			50		mA
I_{IF}	Supply current, IF	Pin 17, 18, and 26 combined		47		mA
I_{VDD1}	Supply current RF1, pin 31			28		mA
V_{IH}	Input high voltage		2.5	5		V
V_{IL}	Input low voltage				0.8	V
I_{IH}	Input high current				300	µA
I_{IL}	Input low current				–50	µA

ELECTRICAL CHARACTERISTICS

Unless otherwise stated V_{DD} = 5 V, FRF = 3500 MHz, I_{DD} = 160 mA, VNEG = -5 V, FRF = 3.5 GHz, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{IF}	IF input frequency			325		MHz
IRF	RF output frequency		3300		3800	MHz
G	Gain	UCATTN = TTL high, input IF impedance is 100-Ω differential		22		dB
Δ_{ATTN}	Switched attenuator range	UCATTN from high-to-low		16		dB
G_{NB}	Gain flatness / 6 MHz				0.2	dB
OP-1dB	Output power at 1-dB compression, high gain	UCATTN = TTL high		14		dBm
OIP3	Output 3rd order intercept point, high gain	UCATTN = TTL high		24		dBm
	Gain - IF to MXRO	UCATTN = TTL high		1		dB
	Gain - RFI to RFO	UCATTN = TTL high		21		dB
P_{LO}	LO input power	Referenced to 100-Ω differential	-3	0	3	dB
	LO to RFO leakage(1)	LO input = 0 dBm		-5		dBm

(1) Performance is sensitive to impedance termination and board layout.

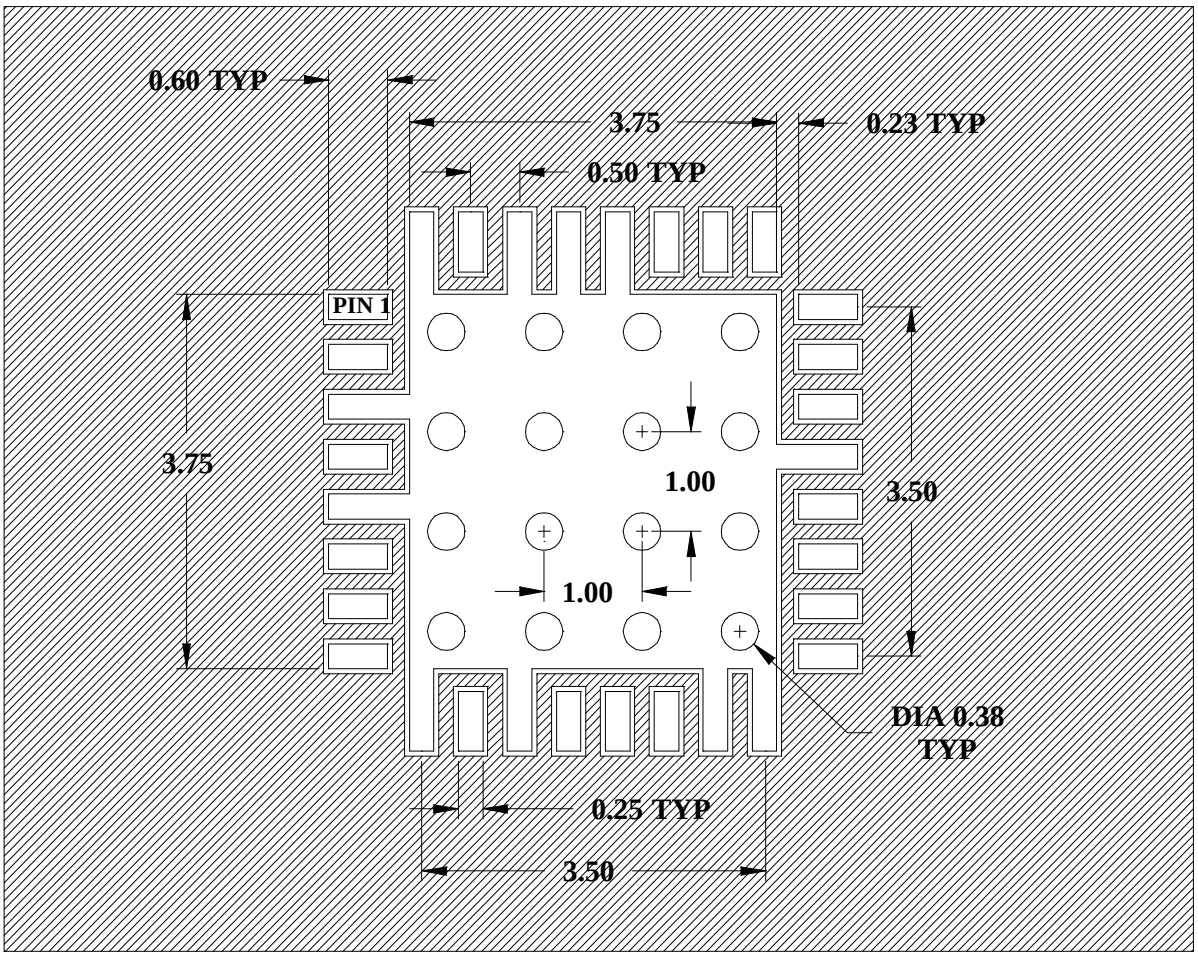
APPLICATION INFORMATION

A typical application schematic is shown in Figure 3.

The PCB material recommendations are shown in Table 1 and Figure 2.

Table 1. PCB Recommendations

Board Material	FR4
Board Material Core Thickness	10 mil
Copper Thickness (starting)	1 oz
Prepreg Thickness	8 mil
Recommended Number of Layers	4
Via Plating Thickness	½ oz
Final Plate	White immersion tin
Final Board Thickness	33–37 mil



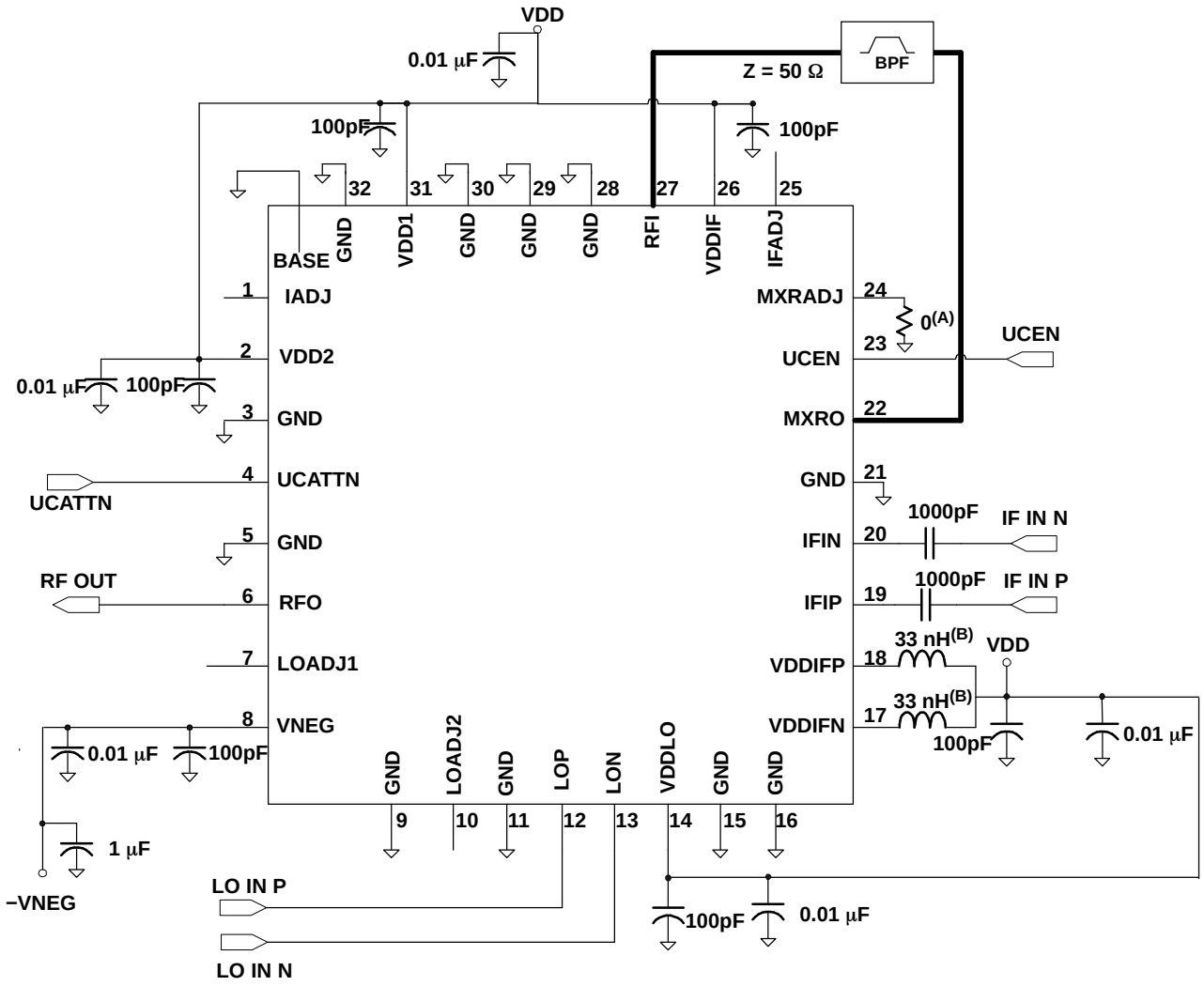
SOLDER MASK: NO SOLDERMASK UNDER CHIP, ON LEAD PADS OR ON GROUND CONNECTIONS.

16 VIA HOLES, EACH 0.38 mm.

DIMENSIONS in mm

NOTE: Top and bottom surface finish: copper flash with 50–70 µin white tin immersion.

Figure 2. PCB Construction and Via Cross Section



Place 100pF capacitors as close as possible to package pins.

A. Connect pin 24 to ground through a 0-Ω resistor.

B. Place 33-nH inductors close to package pins.

C. Place 100-pF capacitors close as possible to package pins.

Figure 3. Recommended Application Schematic

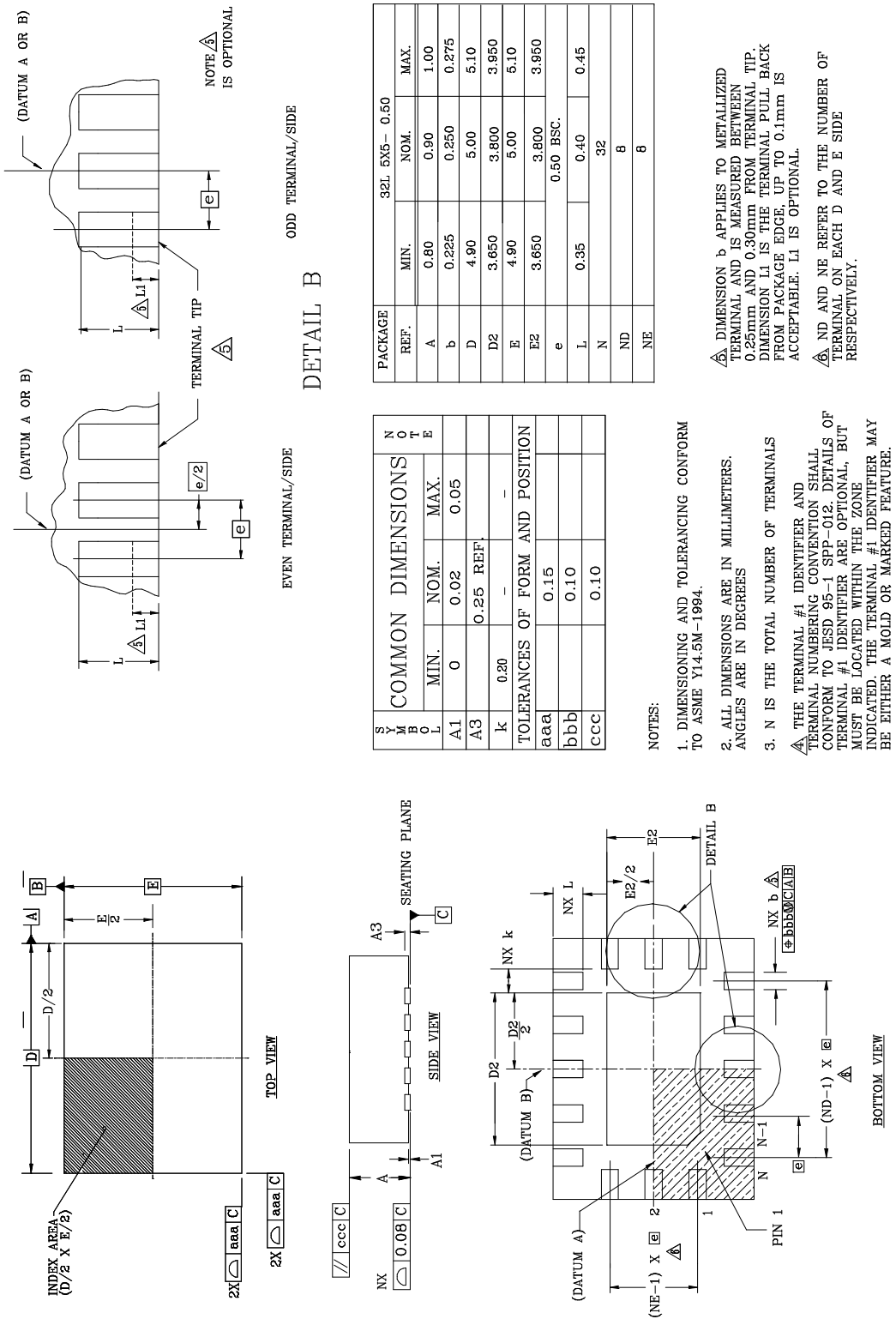
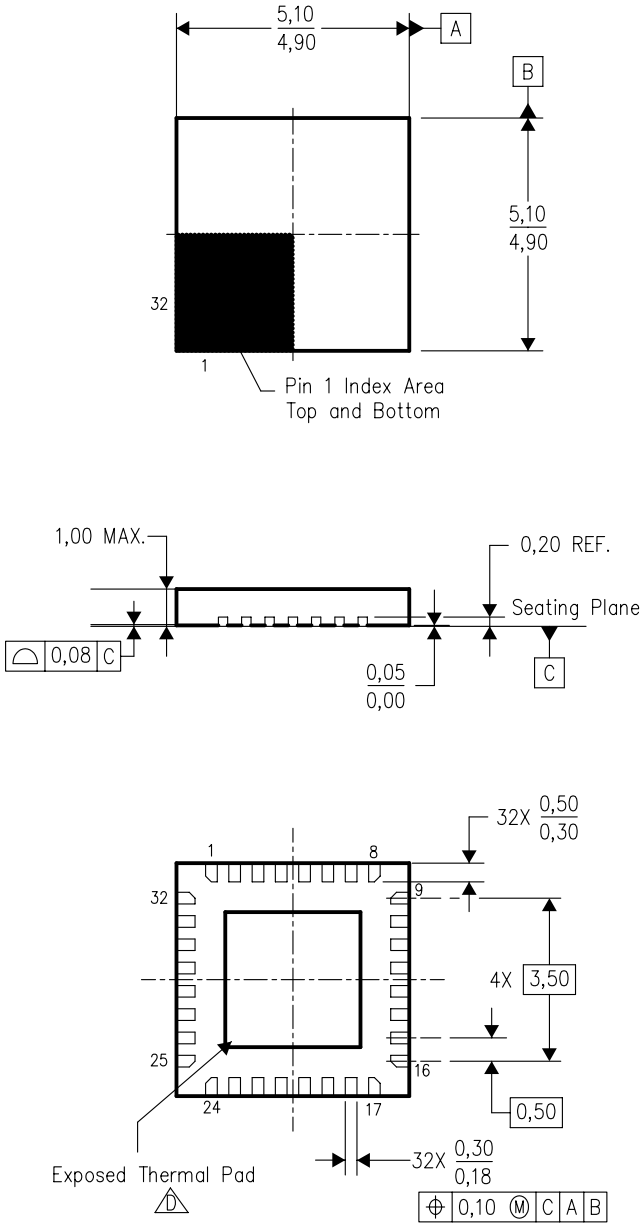


Figure 4. Package Outline 5 mm x 5 mm LPCC 32-Pin Leadless Package

RTM (S–PQFP–N32) PLASTIC QUAD FLATPACK



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–220.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF1222IRTMR	ACTIVE	VQFN	RTM	32	3000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	TRF 1222	Samples
TRF1222IRTMT	ACTIVE	VQFN	RTM	32	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	TRF 1222	Samples
TRF1222IRTMTG3	ACTIVE	VQFN	RTM	32	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	TRF 1222	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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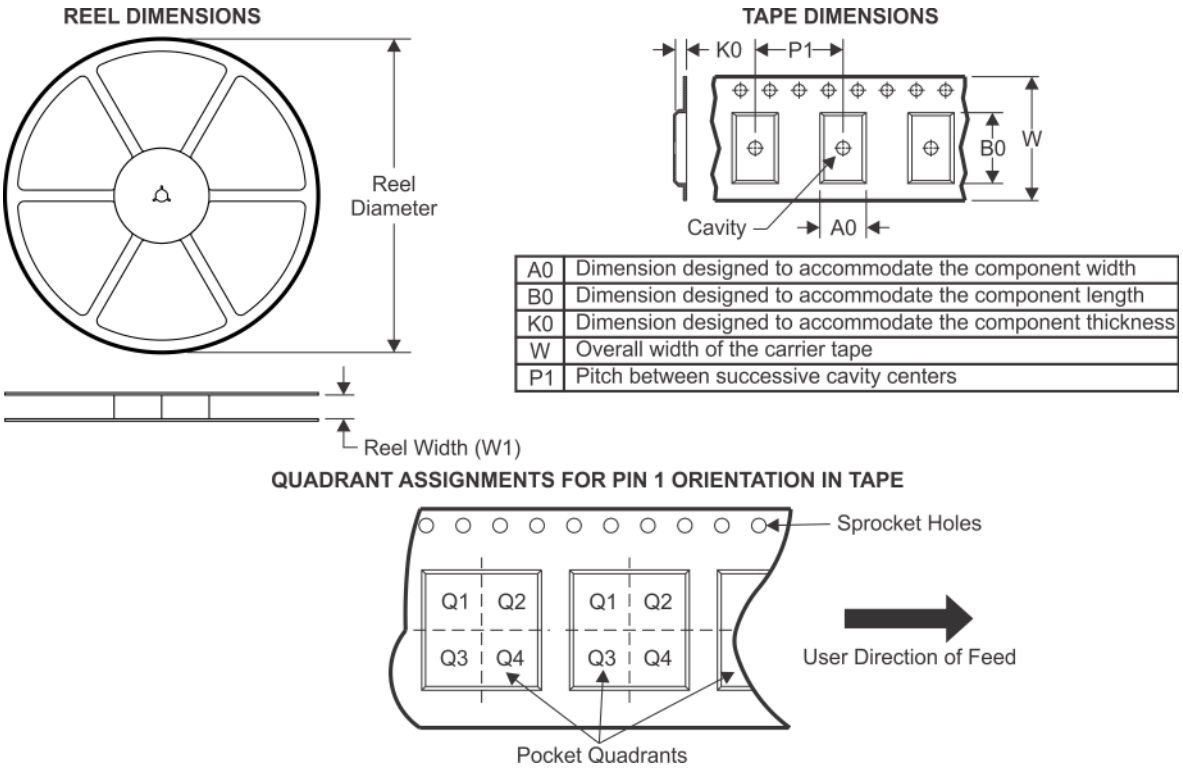
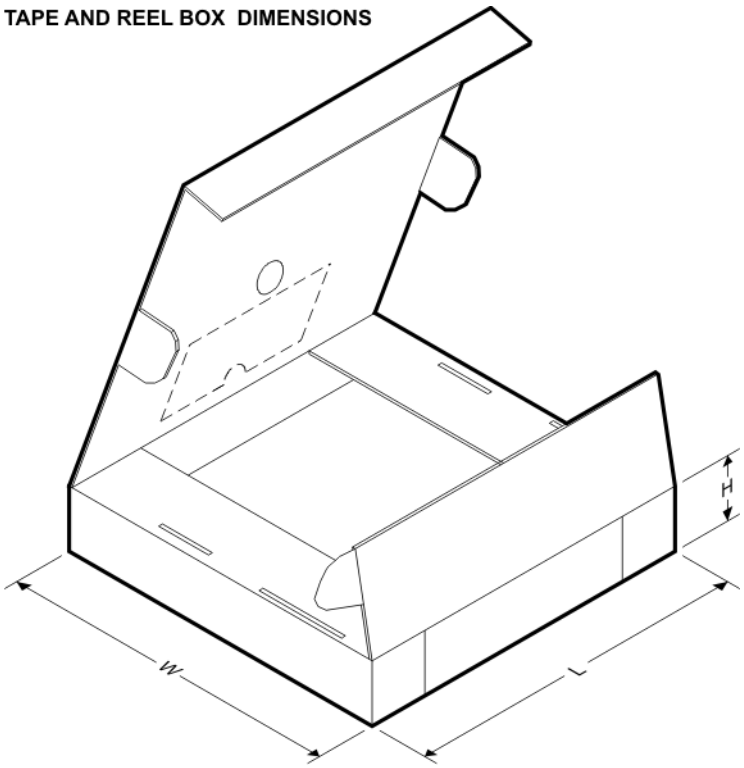


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF1222IRTMR	VQFN	RTM	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TRF1222IRTMT	VQFN	RTM	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

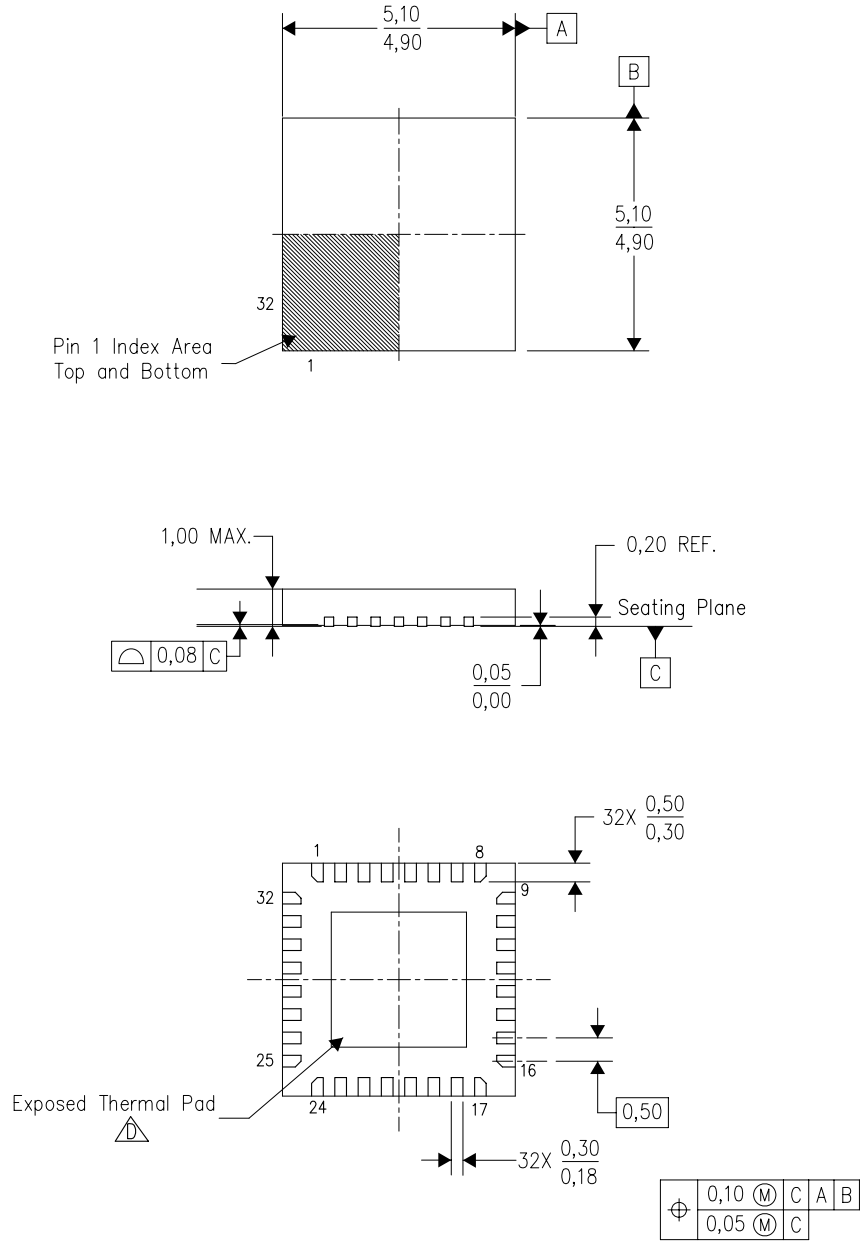
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF1222IRTMR	VQFN	RTM	32	3000	338.1	338.1	20.6
TRF1222IRTMT	VQFN	RTM	32	250	210.0	185.0	35.0

RTM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–220.

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