DEM-OPA-SO-2E Demonstration Fixture

1 Description

The DEM-OPA-SO-2E demonstration fixture is a generic, unpopulated printed circuit board (PCB) for high-speed dual operational amplifiers in an SO-8 package with a flow-through pinout. Figure 1 shows the package pinouts supported by this PCB. For more information on specific op amps, as well as good PCB layout techniques, see the individual amplifier data sheets.

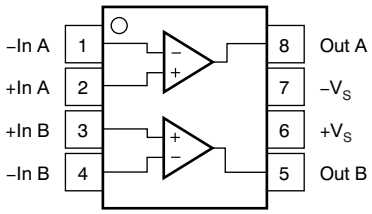
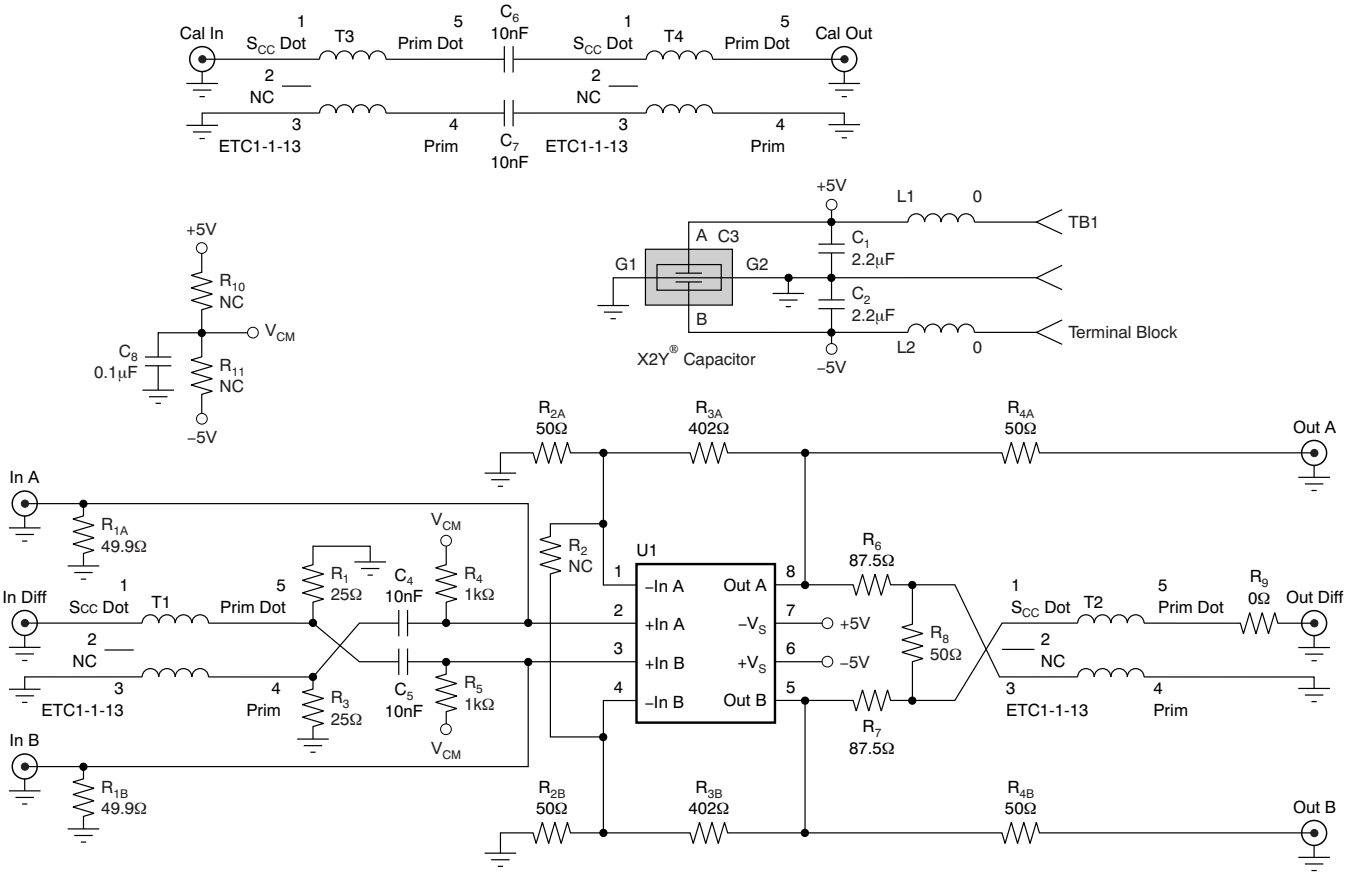


Figure 1. SO-8 Package Pinout, Top View

2 Circuit

The circuit schematic in Figure 2 shows the connections for all possible components. Each configuration uses only some of the components.



NOTE: The positive and negative power-supply connections to pins 6 and 7 of the DUT have been reversed erroneously. To rectify this error, reverse the power-supply connections to the terminal block, TB1. If using tantalum capacitors for C1 and C2, make sure that the polarity of the capacitors match the power-supply connections.

Figure 2. Schematic for DEM-OPA-SO-2E

3 Components

Components that have RF performance similar to the ones listed in Table 1 may be substituted. C_1 and C_2 need a larger voltage rating for ±15V dual supplies.

Table 1. Component Descriptions

PART	DESCRIPTION
C_1, C_2	Tantalum Chip Capacitor, SMD EIA Size 3216, 20V
C_3	X2Y® capacitor, (Yageo X0603MRX7R6BB104)
C_4, C_5, C_6, C_7, C_8	Multilayer Ceramic Chip Capacitor, SMD 0402, 10V
In A, In B, In Diff, Out A, Out B, Out C	SMA or SMB Board Jack (Amphenol 901-144-8)
L_1, L_2	EMI-Suppression Ferrite Chip, SMD 0805 (Steward LI 0805 B 900 R)
TB_1	Terminal Block, 3.5mm Centers (On-Shore Technology ED555/3DS)
R_X, except R_{10} and R_{11}	Metal Film Chip Resistor, SMD 0402, 1/16W
R_{10}, R_{11}	Metal Film Chip Resistor, SMD 0806, 1/8W
T_1, T_2, T_3, T_4	Transformer, (MA\COM ETC1-1-13)

For a single-ended configuration, R_{1X}, R_{2X}, R_{3X}, and R_{4X} are used for the signal path. For a differential configuration, R_1 through R_9 are used to set the input and output impedance conditions. C_1, C_2, and C_3 are supply bypass capacitors. L_1 and L_2 are ferrite chips that can reduce interactions with the power supply at high frequencies. If not desired, they can be replaced with 0Ω resistors.

For the differential configuration, a common dc voltage can be generated using R_{10}, R_{11}, and the bypass capacitor, C_8. The transformers T_3 and T_4 provide a path to calibrate the transformers out of the signal path, if necessary.

4 Board Layout

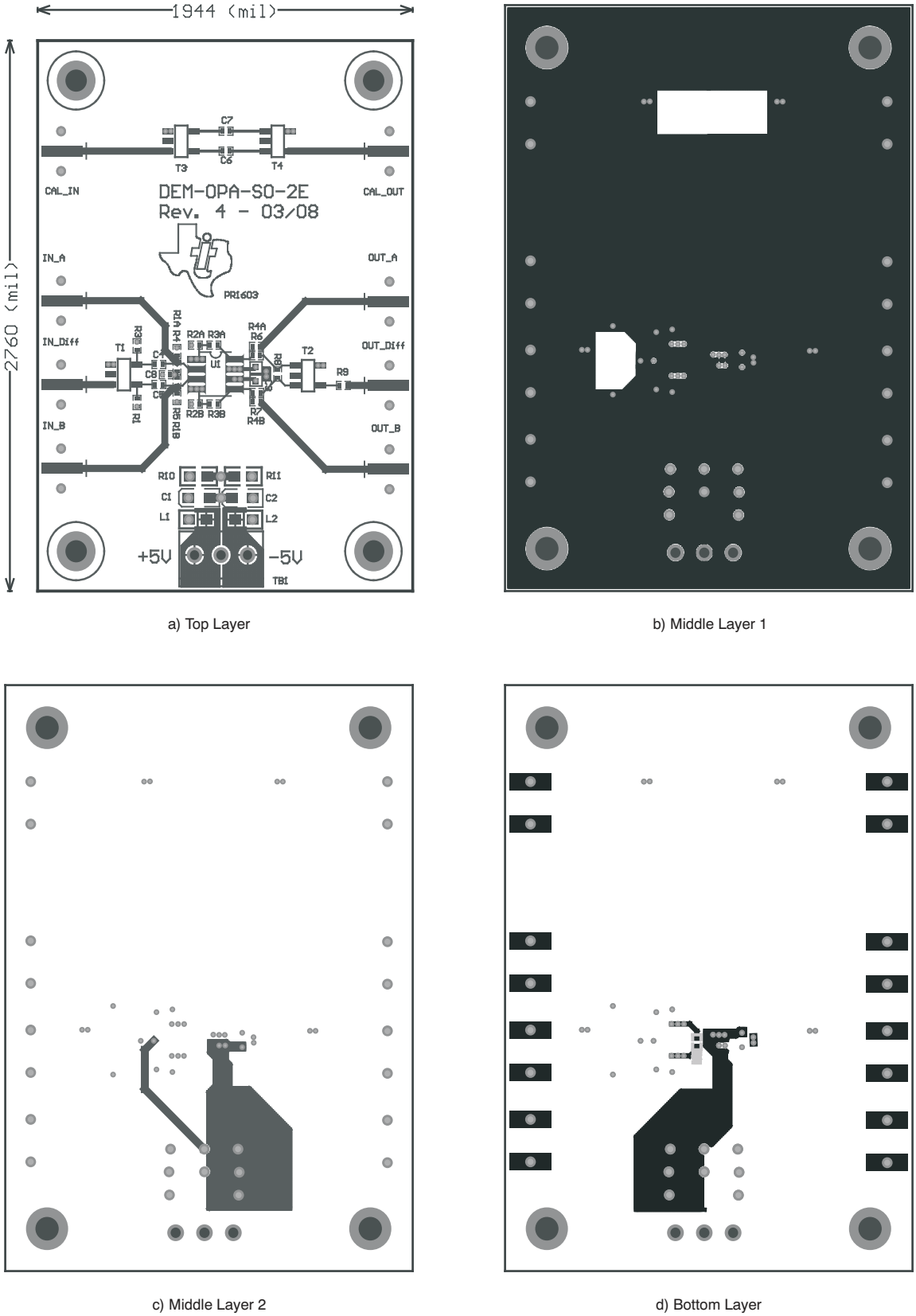
This demonstration fixture is a four-layer PCB. (See Figure 3.) It uses a ground plane located underneath the signal traces to provide 50Ω characteristic impedance transmission lines. The ground plane has been opened up around op amp pins sensitive to capacitive loading. Power-supply traces are laid out to keep current loop areas to a minimum. Power-supply traces are found on the two lower layers. The SMA (or SMB) connectors can be mounted as edge mount connectors.

The location and type of capacitors used for power-supply bypassing are crucial to high-frequency amplifiers. The tantalum capacitors, C_1 and C_2, do not need to be as close to pins 7 and 4 on the PCB, and may be shared with other amplifiers.

See the individual op amp data sheet for more information on proper PCB layout techniques and component selection.

5 Measurement Tips

This demonstration fixture, with the component values shown, is designed to operate in a 50Ω environment; most data sheet plots are obtained under these conditions. It is easy to change the component values for different input and output impedance levels. However, do not use high-impedance probes; they represent a heavy capacitive load to the op amp, and alter the amplifier response. Instead, use low-impedance (≤ 500Ω) probes with adequate bandwidth. The probe input capacitance and resistance set an upper limit on the measurement bandwidth. If a high-impedance probe must be used, place a 100Ω resistor on the probe tip to isolate its capacitance from the circuit.



a) Top Layer

b) Middle Layer 1

c) Middle Layer 2

d) Bottom Layer

Figure 3. DEM-OPA-SO-2E Demonstration Board Layout

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2008) to A Revision	Page
• Added note to Figure 2	2

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