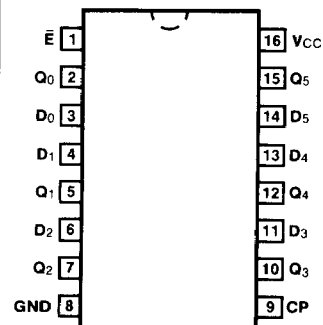


54LS/74LS378

PARALLEL D REGISTER (With Enable)

CONNECTION DIAGRAM PINOUT A



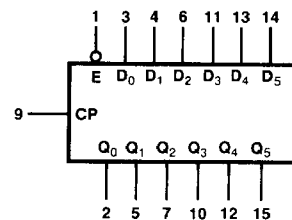
DESCRIPTION — The '378 is a 6-bit register with a buffered common enable. This device is similar to the '174, but with common Enable rather than common Master Reset.

- 6-BIT HIGH SPEED PARALLEL REGISTER
- POSITIVE EDGE-TRIGGERED D-TYPE INPUTS
- FULLY BUFFERED COMMON CLOCK AND ENABLE INPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULL TTL AND CMOS COMPATIBLE

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	74LS378PC		9B
Ceramic DIP (D)	A	74LS378DC	54LS378DM	6B
Flatpak (F)	A	74LS378FC	54LS378FM	4L

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
\bar{E}	Enable Input (Active LOW)	
$D_0 - D_5$	Data Inputs	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$Q_0 - Q_5$	Flip-flop Outputs	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '378 consists of eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable (\bar{E}) inputs are common to all flip-flops.

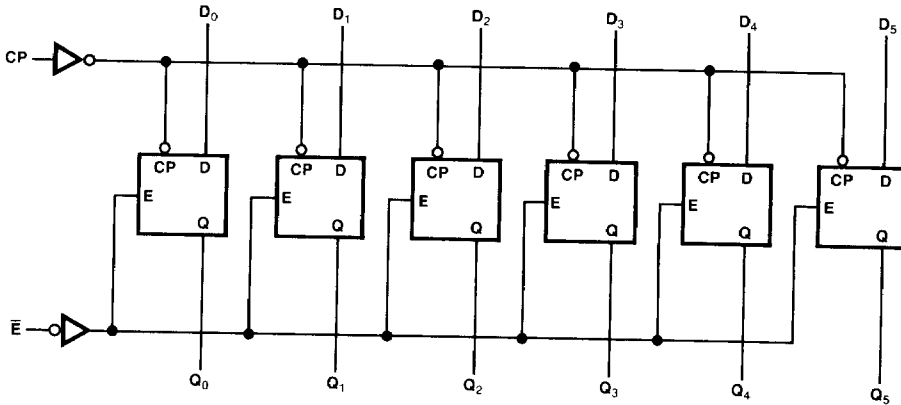
When the \bar{E} input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the \bar{E} input is HIGH the register will retain the present data independent of the CP input.

TRUTH TABLE

INPUTS			OUTPUT
\bar{E}	CP	D_n	Q_n
H		X	No change
L		H	H
L		L	L


H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

LOGIC DIAGRAM



4

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		22	mA	$V_{CC} = \text{Max}, D_n = \bar{E} = \text{Gnd}$ CP = 

AC CHARACTERISTICS: $V_{CC} = +5.0 \text{ V}, T_A = +25^\circ\text{C}$ (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		$C_L = 15 \text{ pF}$			
		Min	Max		
f_{max}	Maximum Clock Frequency	30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		27 27	ns	Figs. 3-1, 3-8

AC OPERATING REQUIREMENTS: $V_{CC} = +5.0 \text{ V}, T_A = +25^\circ\text{C}$

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H)	Setup Time HIGH, D_n to CP	20		ns	Fig. 3-6
t_h (H)	Hold Time HIGH, D_n to CP	5.0		ns	Fig. 3-6
t_s (L)	Setup Time LOW, D_n to CP	20		ns	Fig. 3-6
t_h (L)	Hold Time LOW, D_n to CP	5.0		ns	Fig. 3-6
t_s (H)	Setup Time HIGH, \bar{E} to CP	30		ns	Fig. 3-6
t_h (H)	Hold Time HIGH, \bar{E} to CP	5.0		ns	Fig. 3-6
t_s (L)	Setup Time LOW, \bar{E} to CP	30		ns	Fig. 3-6
t_h (L)	Hold Time LOW, \bar{E} to CP	5.0		ns	Fig. 3-6
t_w (H)	CP Pulse Width HIGH	20		ns	Fig. 3-8