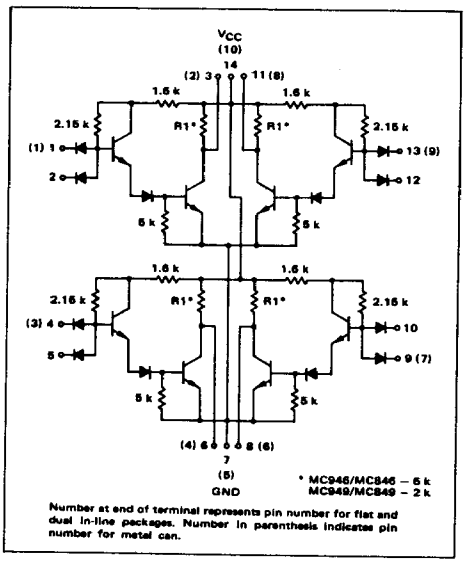
QUAD 2-INPUT "NAND" POWER GATE

MC946F · MC846F, P
MC949F · MC849F, P

QUAD INVERTER

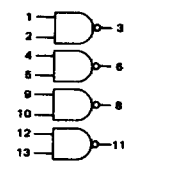
MC946G · MC846G
MC949G · MC849G

This gate element, in the 14-pin flat and dual in-line packages, consists of four 2-input NAND gate circuits. This circuit can be used as a dual 2-input non-inverting gate, or as two bistable circuits when two dual 2-input gates are cross-coupled. Since the metal can (G suffix) has only 10 pins, that circuit consists of four inverters.



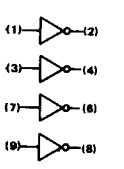
Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.

MC946F/MC846F, P
MC949F/MC849F, P



Positive Logic: $3 = \overline{1 + 2}$
Negative Logic: $3 = \overline{1 + 2}$

MC946G/MC846G
MC949G/MC849G



Positive Logic: $2 = \overline{1}$
Negative Logic: $2 = \overline{1}$

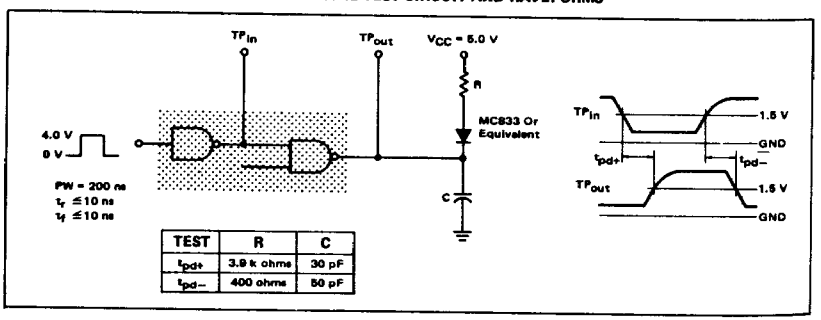
Input Loading Factor = 1
Output Loading Factor:
MC946/MC846 = 8
MC949/MC849 = 7

Total Power Dissipation:

	MC946 MC846	MC949 MC849
Inputs Low	24 mW	24 mW
Inputs High	82 mW	84 mW
50% Duty Cycle	38 mW	84 mW

Propagation Delay Time:
MC946/MC846 = 30 ns typ
MC949/MC849 = 25 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

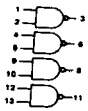


TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	50 pF

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner.

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.



PACKAGE	PIN NUMBER												
Flat/Dual In-Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Metal Can	1	–	2	3	–	4	5	6	7	–	8	–	9	10

Characteristic	Symbol	Pin Under Test	MC946, MC949 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC846, MC849 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Output Voltage	V_{OL}	3	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc
	V_{OH}	3	2.50	-	2.60	-	2.50	-	↓	2.60	-	2.60	-	2.50	-	↓
		3	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-	
Short-Circuit Current MC946/MC846 MC949/MC849	I_{SC}	3	-	-1.34	-	-1.34	-	-1.30	mAdc	-	-1.30	-	-1.30	-	-1.25	mAdc
		3	-	-4.00	-	-4.00	-	-3.90	mAdc	-	-3.90	-	-3.90	-	-3.75	mAdc
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc
		2	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc
Output Leakage Current	I_{CEX}	3	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc
		2	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc
Power Drain Current (Total Device) MC946, MC846	I_{PDH}	14	-	-	-	13	-	-	mAdc	-	-	-	16	-	-	mAdc
MC949, MC849	I_{PDH}	14	-	-	-	21.4	-	-	↓	-	-	-	26.2	-	-	↓
All Types	I_{max}	14	-	-	-	11	-	-		-	-	-	16	-	-	
Switching Times																
MC946, MC846	t_{pd+}	1, 3	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns
	t_{pd-}	1, 3	-	-	10	30	-	-	↓	-	-	10	30	-	-	↓
MC949, MC849	t_{pd+}	1, 3	-	-	15	60	-	-		-	-	15	60	-	-	
	t_{pd-}	1, 3	-	-	10	30	-	-		-	-	10	30	-	-	

Pins not listed are left open.

@ Test Temperature	TEST CURRENT / VOLTAGE VALUES mA I_{OL}		mA I_{OH}		Volts V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}
	MC946	MC949	MC946	MC949									
MC946, MC949 −55°C	11.4	10.4	-0.12	-0.5	1.40	2.10	0	4.00	-	-	4.50	5.50	-
MC946, MC949 +25°C	12.0	11.0	-0.12	-0.5	1.10	2.00	0	4.00	-	-	4.50	5.50	8.00
MC946, MC949 +125°C	10.8	9.8	-0.12	-0.5	0.80	2.00	0	4.00	-	-	4.50	5.50	-
	MC846	MC849	MC846	MC849									
MC846, MC849 0°C	12.0	11.0	-0.12	-0.5	1.20	2.00	0.45	4.00	-	-	5.00	5.00	-
MC846, MC849 +25°C	12.0	11.0	-0.12	-0.5	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	8.00
MC846, MC849 +75°C	11.4	10.4	-0.12	-0.5	0.95	1.80	0.50	4.00	-	-	5.00	5.00	-

TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_R	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
3	-	-	1,2	-	-	-	-	14	-	-	7
-	3	1	-	-	-	-	-	↓	-	-	↓
-	3	2	-	-	-	-	-		-	-	
-	-	-	-	-	-	-	-	14	-	-	1,3,7
-	-	-	-	-	-	-	-	14	-	-	1,3,7
-	-	-	-	-	1	-	-	14	-	-	2,7
-	-	-	-	-	2	-	-	14	-	-	1,7
-	-	-	-	-	-	3,14	-	-	-	-	1,7
-	-	-	1	2	-	-	-	14	-	-	7
-	-	-	2	1	-	-	-	14	-	-	7
-	-	-	-	-	-	-	-	14	-	-	7
-	-	-	-	-	-	-	-	14	-	-	7
-	-	-	-	-	-	-	-	-	14	-	1,4,7,9,12
Pulse In	Pulse Out										
1	3	-	-	-	-	-	14	-	-	-	7
		-	-	-	-	-		-	-	-	
		-	-	-	-	-		-	-	-	

PRODUCT DOCUMENTATION

The three documents listed in the following table are required for a complete description of the DSP56301 and are necessary to design properly with the part. Documentation is available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

See the **Additional Support** section of the *DSP56300 Family Manual* for detailed information on the multiple support options available to you.

Table 1 DSP56301 Documentation

Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD
DSP56301 User's Manual	Detailed functional description of the DSP56301 memory configuration, operation, and register programming	DSP56301UM/AD
DSP56301 Technical Data	DSP56301 features list and physical, electrical, timing, and package specifications	DSP56301/D