

# CBTD3384

10-bit level shifting bus switch with 5-bit output enables

Rev. 10 — 12 March 2021

Product data sheet

## 1. General description

The CBTD3384 provides ten bits of high-speed TTL-compatible bus switching. The low ON resistance of the switch allows connections to be made with minimal propagation delay.

The CBTD3384 device is organized as two 5-bit bus switches with two separate output enable ( $1\overline{OE}$ ,  $2\overline{OE}$ ) inputs. When  $n\overline{OE}$  is LOW, the switch is on and port A is connected to the B port. When  $n\overline{OE}$  is HIGH, each switch is disabled.

## 2. Features and benefits

- Designed to be used in 5 V to 3.3 V level shifting applications with internal diode
- 5  $\Omega$  switch connection between two ports
- TTL-compatible control input levels
- Latch-up protection exceeds 100 mA per JESD78
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - CDM JESD22-C101C exceeds 1000 V
- Specified from -40 °C to +85 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
CBTD3384D	-40 °C to +85 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
CBTD3384PW	-40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

## 4. Functional diagram

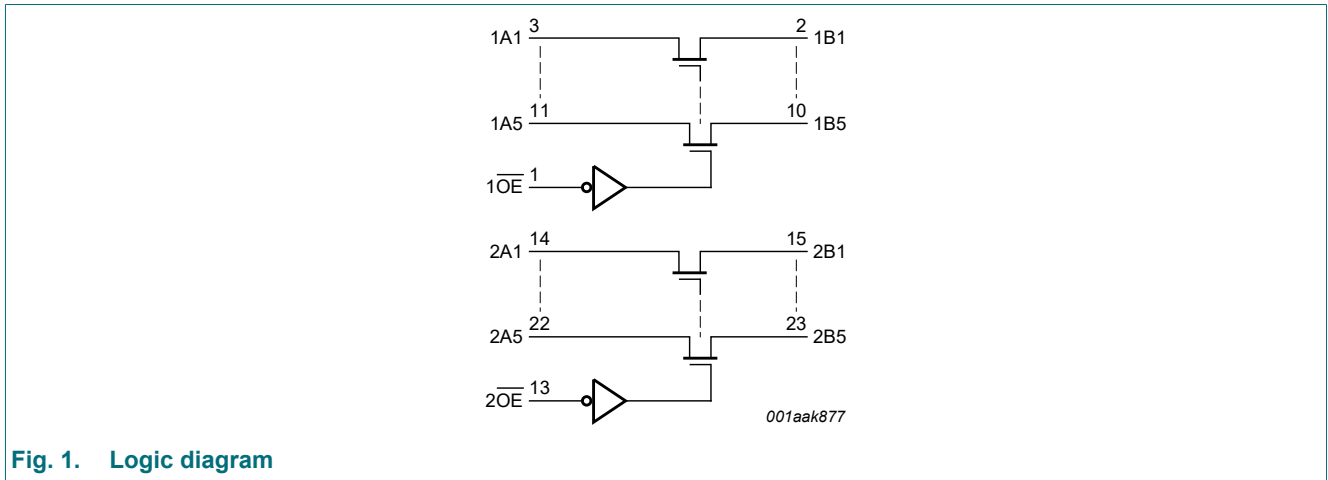


Fig. 1. Logic diagram

## 5. Pinning information

### 5.1. Pinning

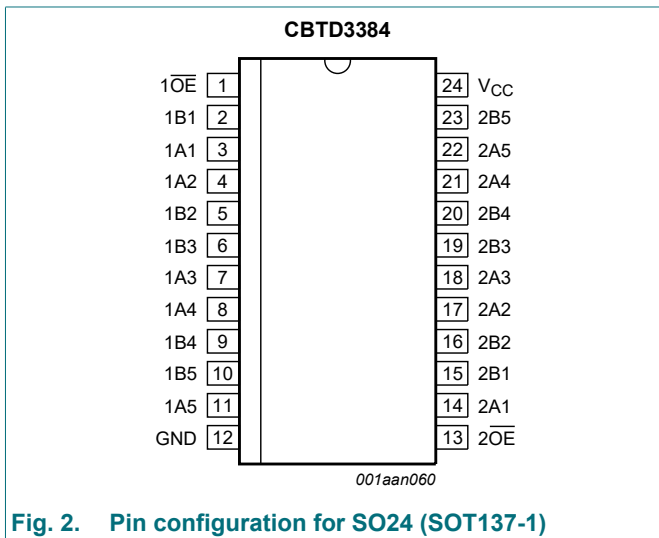


Fig. 2. Pin configuration for SO24 (SOT137-1)

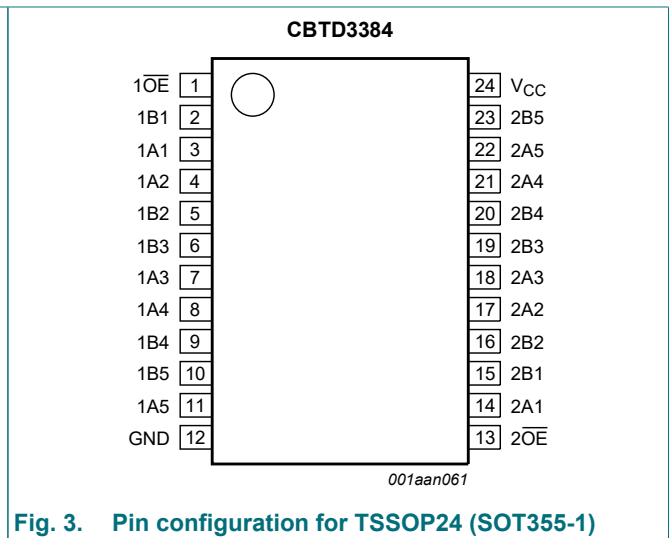


Fig. 3. Pin configuration for TSSOP24 (SOT355-1)

### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 13	output enable input (active LOW)
1A1, 1A2, 1A3, 1A4, 1A5	3, 4, 7, 8, 11	data input/output (A port)
2A1, 2A2, 2A3, 2A4, 2A5	14, 17, 18, 21, 22	data input/output (A port)
1B1, 1B2, 1B3, 1B4, 1B5	2, 5, 6, 9, 10	data input/output (B port)
2B1, 2B2, 2B3, 2B4, 2B5	15, 16, 19, 20, 23	data input/output (B port)
GND	12	ground (0 V)
VCC	24	positive supply voltage

## 6. Functional description

**Table 3. Function selection**

*H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.*

Input		Input/output	
1OE	2OE	1An, 1Bn	2An, 2Bn
L	L	1An = 1Bn	2An = 2Bn
L	H	1An = 1Bn	Z
H	L	Z	2An = 2Bn
H	H	Z	Z

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

*T<sub>amb</sub> = -40 °C to +85 °C, unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage	[1]	-0.5	+7.0	V
I <sub>O</sub>	output current	V <sub>O</sub> < 0 V	-	±128	mA
I <sub>IK</sub>	input clamping current	V <sub>I/O</sub> = 0 V	-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C

[1] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

*All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		4.5	-	5.5	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.8	V
T <sub>amb</sub>	ambient temperature	operating in free air	-40	-	+85	°C

## 9. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

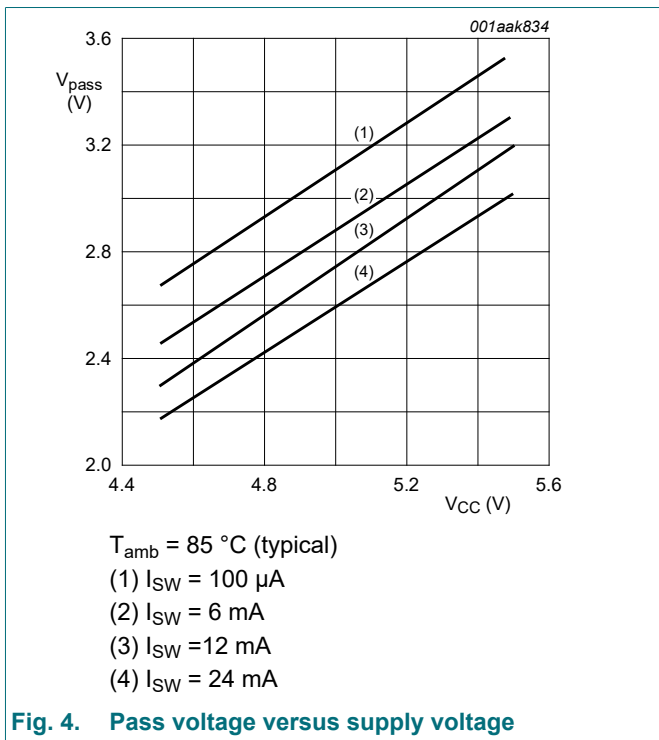
Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V <sub>IK</sub>	input clamping voltage	V <sub>CC</sub> = 4.5 V; I <sub>I</sub> = -18 mA	-	-	-1.2	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V	-	-	±1	µA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 0 mA; V <sub>I</sub> = V <sub>CC</sub> or GND	-	-	1.5	mA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 5.5 V; one input at 3.4 V, other inputs at V <sub>CC</sub> or GND [2]	-	-	2.5	mA
V <sub>pass</sub>	pass voltage	see Fig. 4 to Fig. 8	-	-	-	V
C <sub>I</sub>	input capacitance	control pins; V <sub>I</sub> = 3 V or 0 V	-	3.2	-	pF
C <sub>io(off)</sub>	off-state input/output capacitance	port off; V <sub>I</sub> = 3 V or 0 V; n $\overline{OE}$ = V <sub>CC</sub>	-	6.0	-	pF
R <sub>ON</sub>	ON resistance	V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 0 V; I <sub>I</sub> = 64 mA [3]	-	5	7	Ω
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 0 V; I <sub>I</sub> = 30 mA [3]	-	5	7	Ω
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 2.4 V; I <sub>I</sub> = -15 mA [3]	-	17	50	Ω

[1] All typical values are at V<sub>CC</sub> = 5 V, T<sub>amb</sub> = 25 °C.

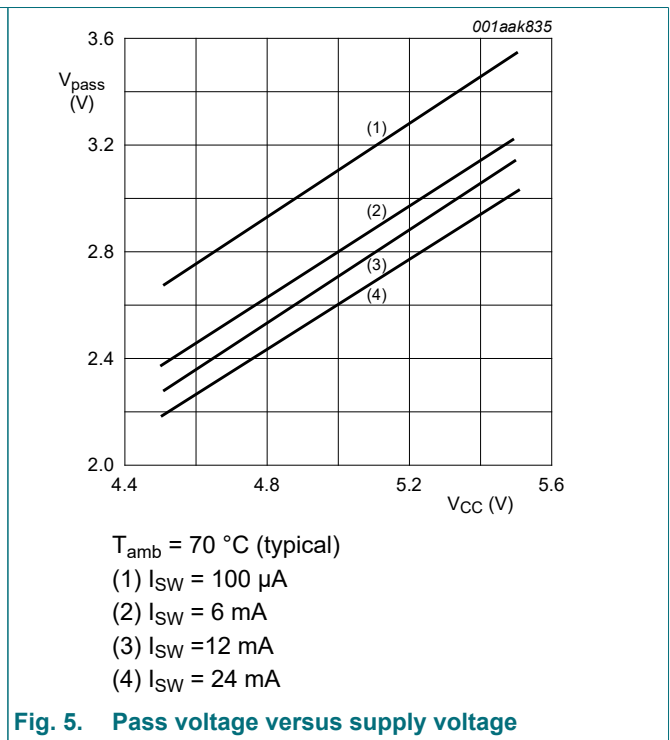
[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

[3] Measured by the voltage drop between the nAn and the nBn terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (nAn or nBn) terminals.

### 9.1. Typical pass voltage graphs



**Fig. 4. Pass voltage versus supply voltage**



**Fig. 5. Pass voltage versus supply voltage**

10-bit level shifting bus switch with 5-bit output enables

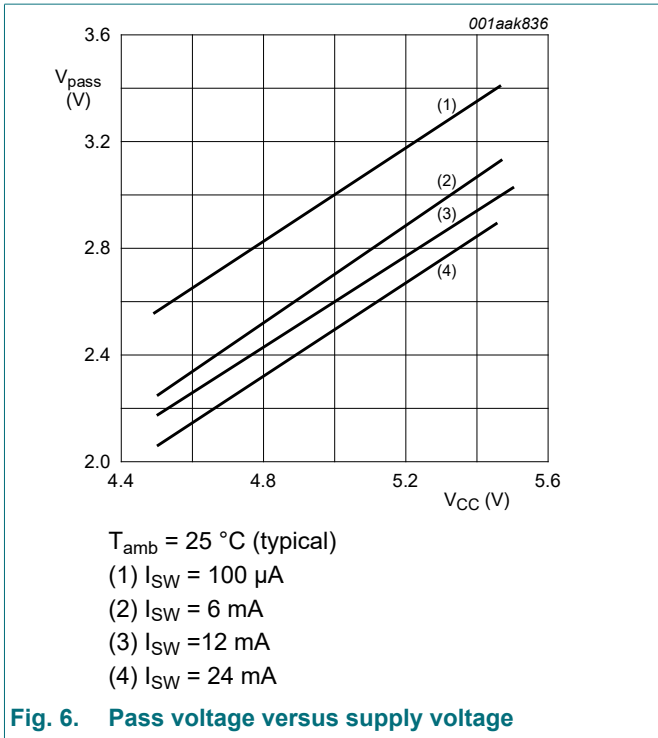


Fig. 6. Pass voltage versus supply voltage

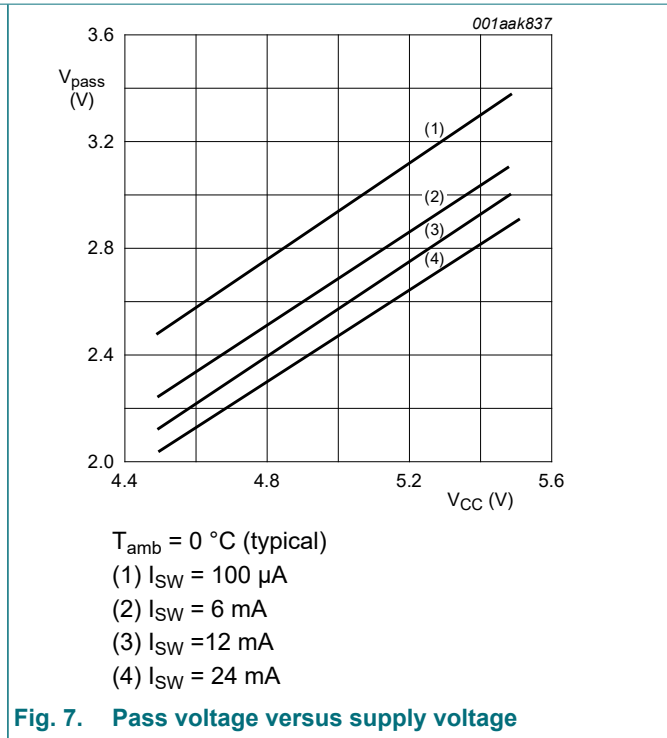


Fig. 7. Pass voltage versus supply voltage

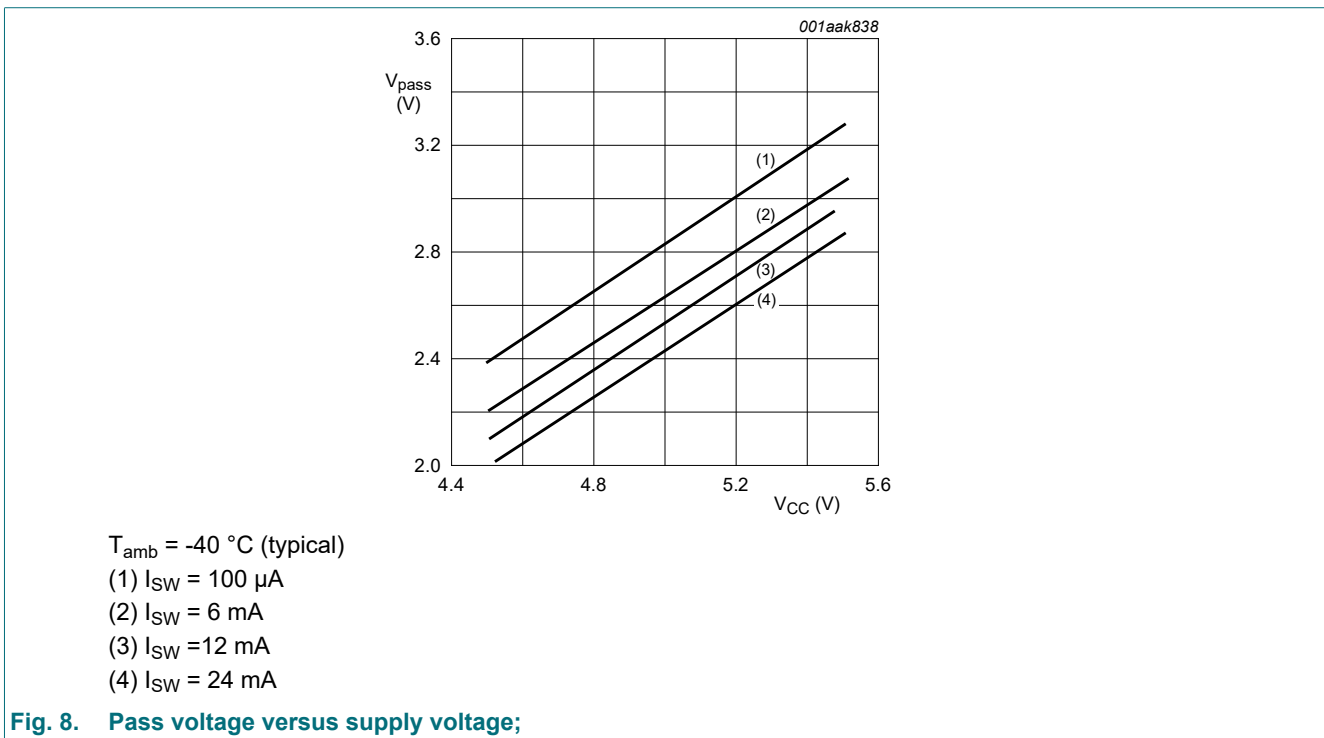


Fig. 8. Pass voltage versus supply voltage;

## 10. Dynamic characteristics

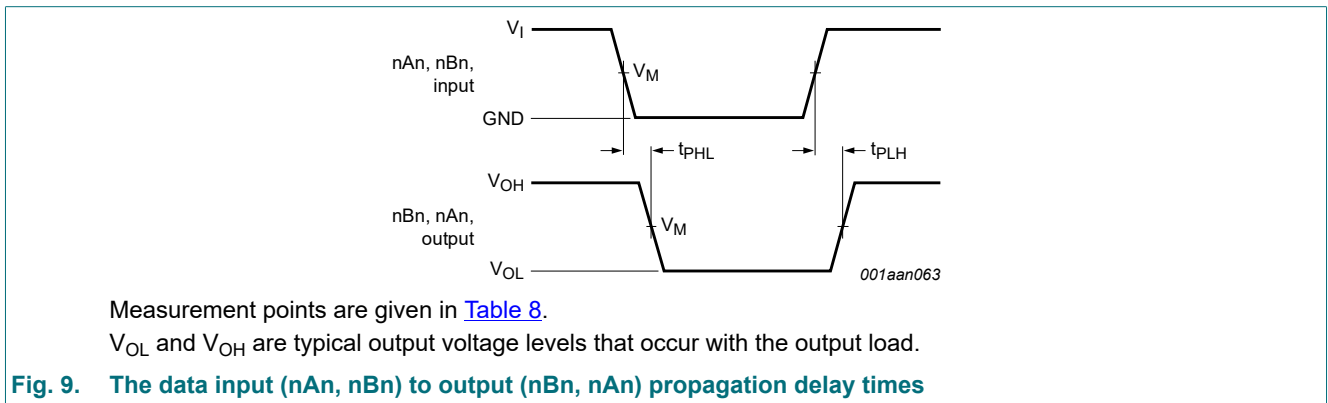
**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 11.

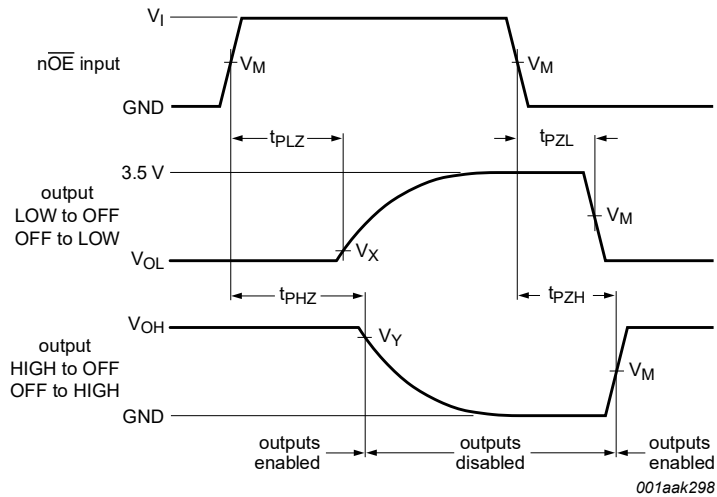
Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ	Max	
t <sub>pd</sub>	propagation delay	nAn, nBn to nBn, nAn; see Fig. 9 [1] [2]				
		V <sub>CC</sub> = 5.0 V ± 0.5 V	-	-	0.25	ns
t <sub>en</sub>	enable time	n $\overline{O}E$ to nAn or nBn; see Fig. 10 [2]				
		V <sub>CC</sub> = 5.0 V ± 0.5 V	1.2	4.3	7.0	ns
t <sub>dis</sub>	disable time	n $\overline{O}E$ to nAn or nBn; see Fig. 10 [2]				
		V <sub>CC</sub> = 5.0 V ± 0.5 V	1.7	3.0	5.3	ns

- [1] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

### 10.1. Waveforms and test circuit



10-bit level shifting bus switch with 5-bit output enables



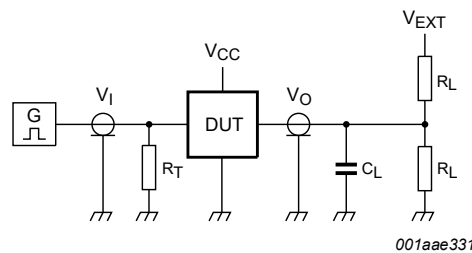
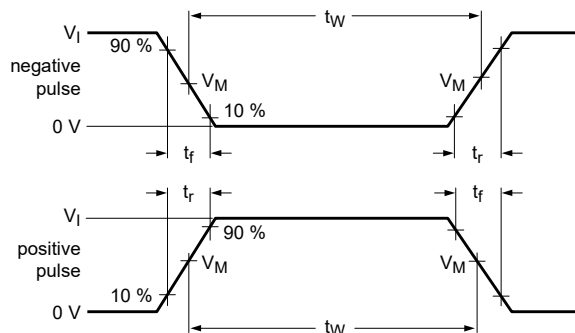
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 10. Enable and disable times**

**Table 8. Measurement points**

Supply voltage	Input		Output		
$V_{CC}$	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$	GND to 3.0 V	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$



Test data is given in [Table 9](#).

All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ;  $Z_o = 50\ \Omega$ .

The outputs are measured one at a time with one transition per measurement.

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 11. Test circuit for measuring switching times**

## 10-bit level shifting bus switch with 5-bit output enables

Table 9. Test data

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	GND to 3.0 V	$\leq 2.5 \text{ ns}$	50 pF	500 $\Omega$	open	7.0 V	open



### 11. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

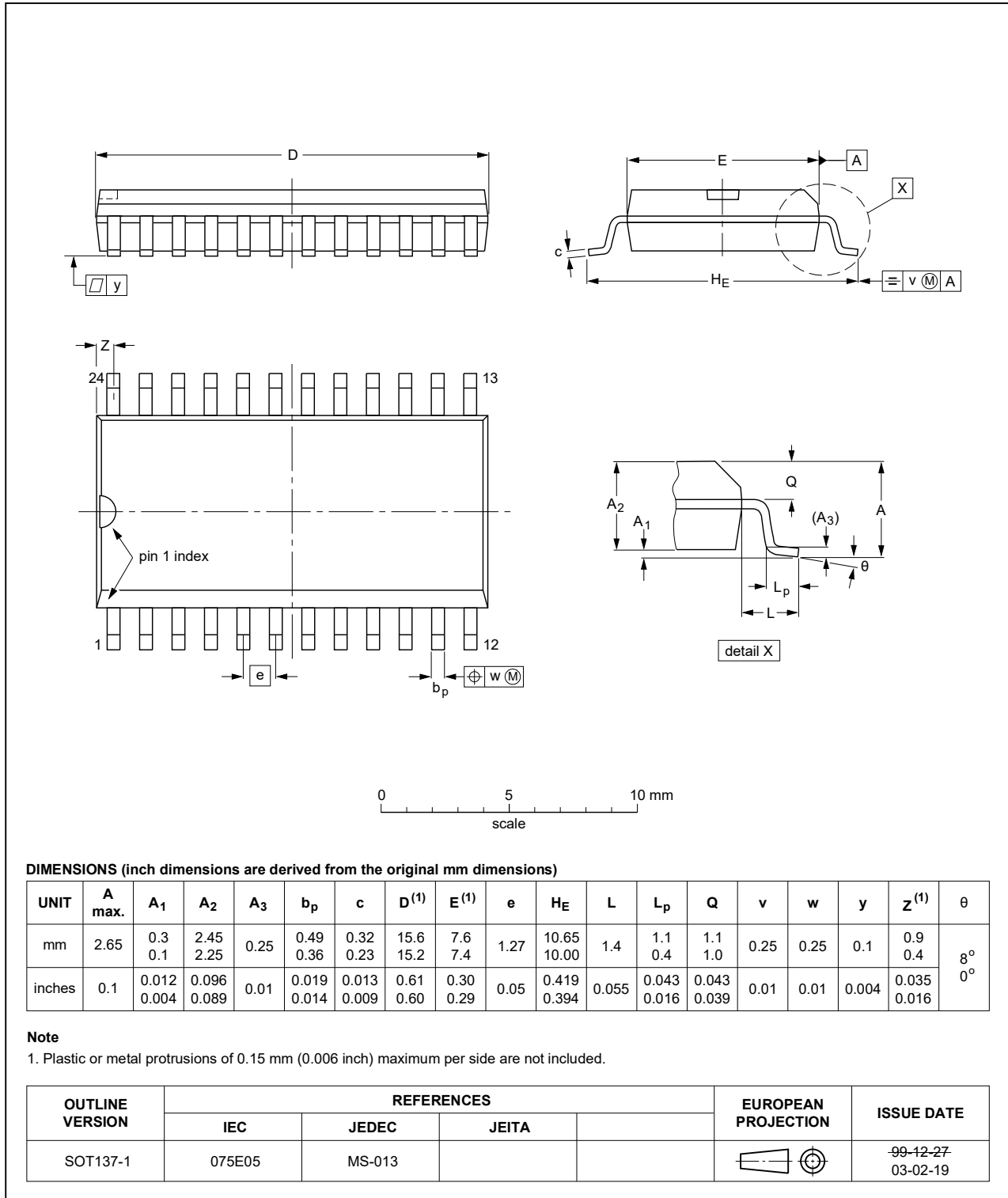


Fig. 12. Package outline SOT137-1 (SO24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

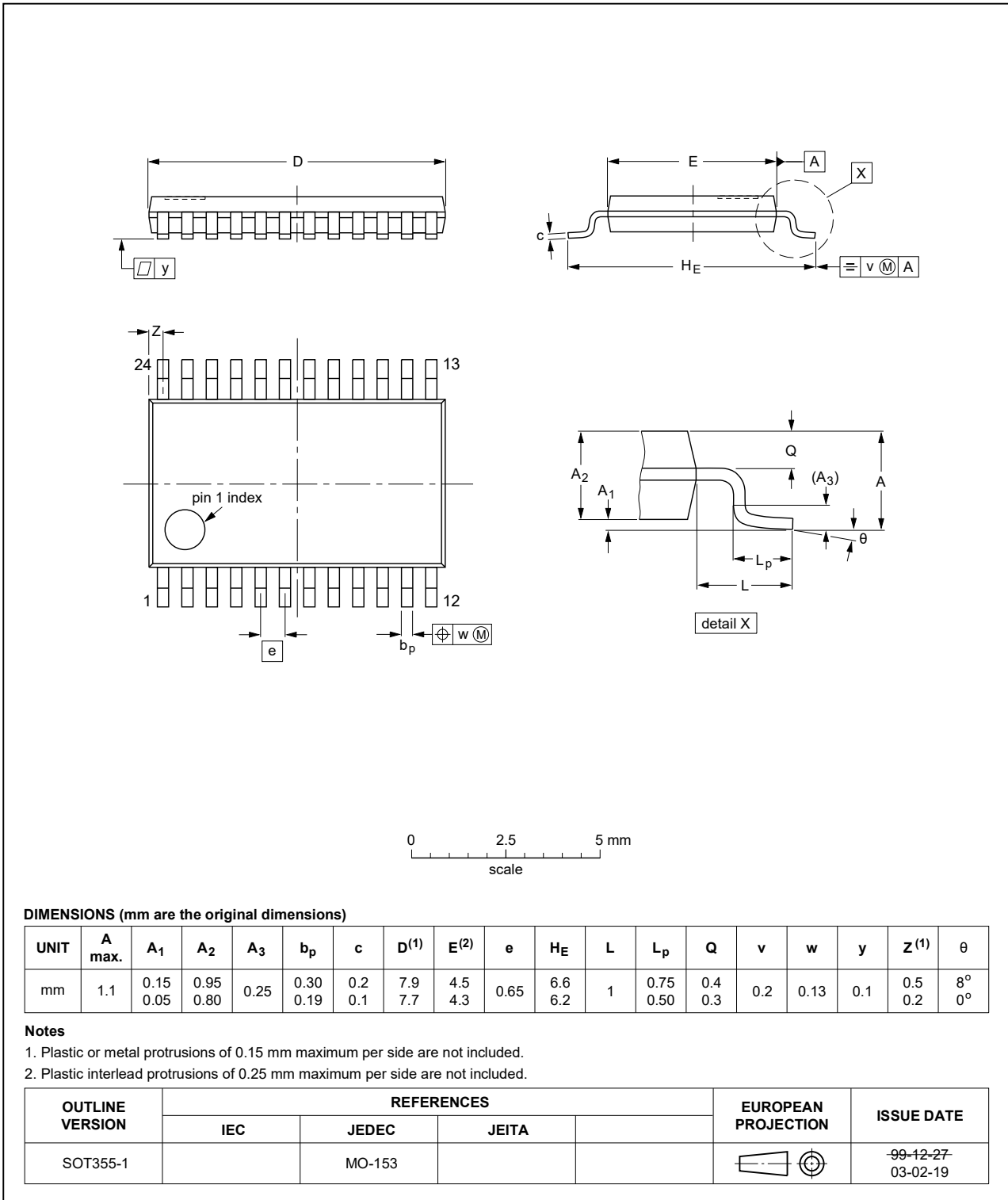


Fig. 13. Package outline SOT355-1 (TSSOP24)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTD3384 v.10	20210312	Product data sheet	-	CBTD3384 v.9
Modifications:	<ul style="list-style-type: none"> <li>Type number CBTD3384DB (SOT340-1 / SSOP24) removed.</li> </ul>			
CBTD3384 v.9	20190306	Product data sheet	-	CBT3384 v.8
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number CBTD3384DK (SOT556-1) removed.</li> </ul>			
CBTD3384 v.8	20121212	Product data sheet	-	CBT3384 v.7
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 1</a>: changed +125 °C into +85 °C (errata).</li> </ul>			
CBTD3384 v.7	20121119	Product data sheet	-	CBT3384 v.6
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 1</a>: changed +85 °C into +125 °C (errata).</li> </ul>			
CBTD3384 v.6	20111121	Product data sheet	-	CBTD3384 v.5
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
CBTD3384 v.5	20101119	Product data sheet	-	CBTD3384 v.4
CBTD3384 v.4	20011220	Product specification		CBTD3384 v.3
CBTD3384 v.3	20000830	Product specification	-	CBTD3384 v.2
CBTD3384 v.2	20000830	Product specification	-	-

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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