**Low Noise, Low Cost, High End Features,
Dual Audio Log Potentiometer**

New Feature

Zero Amplitude
Wiper Switching

XICOR

X9460

Dual Audio Control Digitally Controlled Potentiometer (XDCP™)

FEATURES

- **Dual audio control – Two 32 taps Log pots**
- **Zero Amplitude Wiper Switching**
- **2-wire serial interface**
  4 cascadable slave byte addresses [A1,A0]
- **Total resistance: 33KΩ each XDCP (Typical)**
- **Dual Voltage Operation**
  V+/V- = ±2.7 to ±5.5V
- **Temp Range = -40ºC to +85 ºC**
- **Package Options**
  14-Lead TSSOP

AUDIO PERFORMANCE

- **0 to - 62dB volume control**
- **-92dB Mute**
  —Power up to mute position
- **SNR -96dB**
- **THD+N: -95dB @1k HZ**
- **Crosstalk rejection: -102dB @ 1k HZ**
- **Channel-to-channel variation: ± 0.1dB**
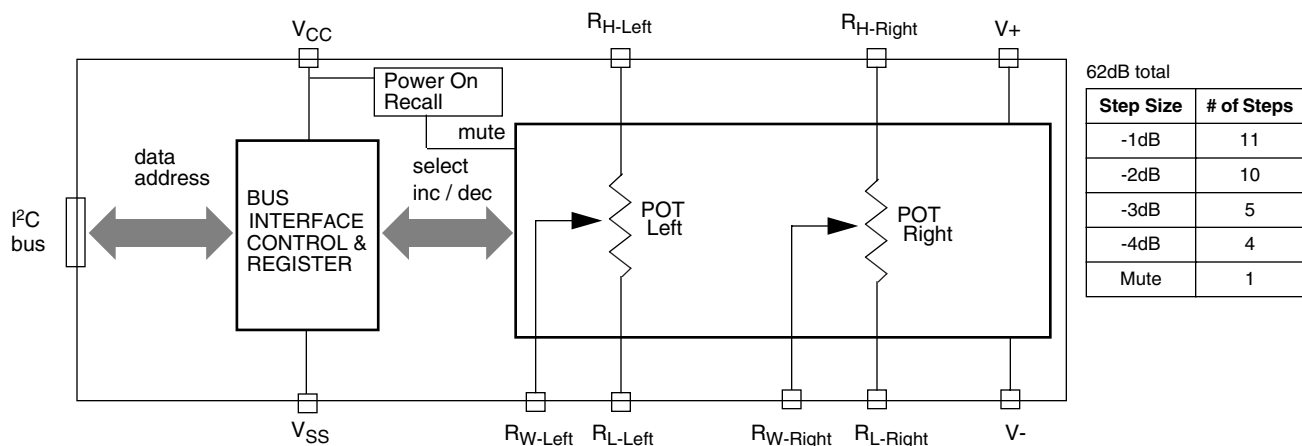- **3dB-cutoff: 100kHz**

DESCRIPTION

The X9460 integrates two digitally controlled potentiometer (XDCP) on a monolithic CMOS integrated circuit. The two XDCPs can be used as stereo gain controls in audio applications. Read/Write operations can directly access each channel independently or both channels simultaneously. Increment/ Decrement can adjust each channel independently or both channels simultaneously.

The X9460 contains a zero amplitude wiper switching circuit that delays wiper changes until the next zero crossing of the audio signal.

The digitally controlled potentiometer is implemented using 31 polysilicon resistors in a log array. Between each of the resistors are tap points connected to the wiper terminal through switches. The XDCPs are designed to minimize wiper noise to avoid pops and clicks during audio volume transitions. The position of the wiper on the array is controlled by the user through the 2-wire serial bus interface.
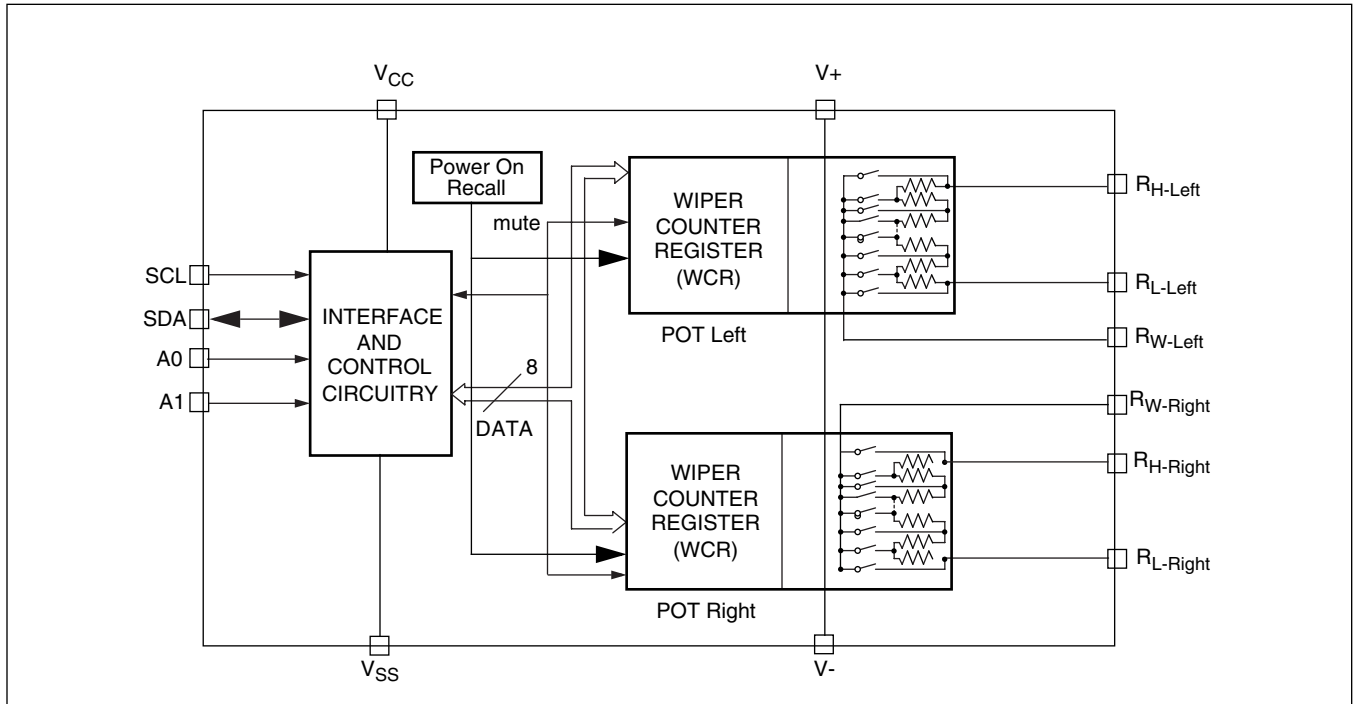
Power up reset the wiper to the mute position.
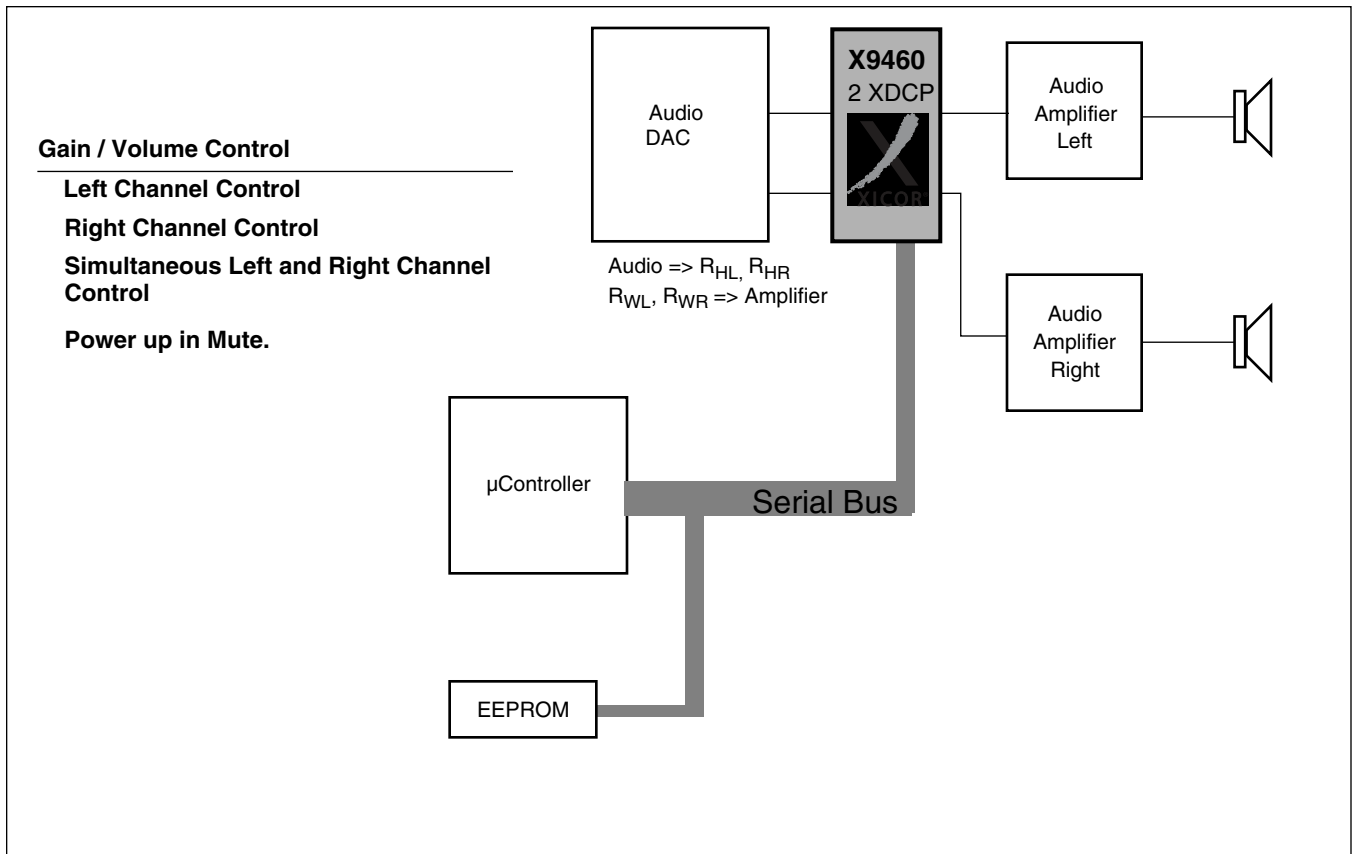
**SIMPLIFIED
FUNCTIONAL DIAGRAM**

Step Size	# of Steps
-1dB	11
-2dB	10
-3dB	5
-4dB	4
Mute	1

62dB total

X9460

DETAILED FUNCTIONAL DIAGRAM

TYPICAL APPLICATION

Gain / Volume Control

Left Channel Control

Right Channel Control

Simultaneous Left and Right Channel Control

Power up in Mute.

Audio => R_{HL}, R_{HR}
R_{WL}, R_{WR} => Amplifier

X9460

PIN CONFIGURATION

```
                    TSSOP

SDA  ⊏  1       14  ⊐  V-
SCL  ⊏  2       13  ⊐  R_H-right
V_CC ⊏  3       12  ⊐  R_L-right
V+   ⊏  4  X9460 11  ⊐  R_W-right
V_SS ⊏  5       10  ⊐  R_H-left
A1   ⊏  6        9  ⊐  R_L-left
A0   ⊏  7        8  ⊐  R_W-left
```
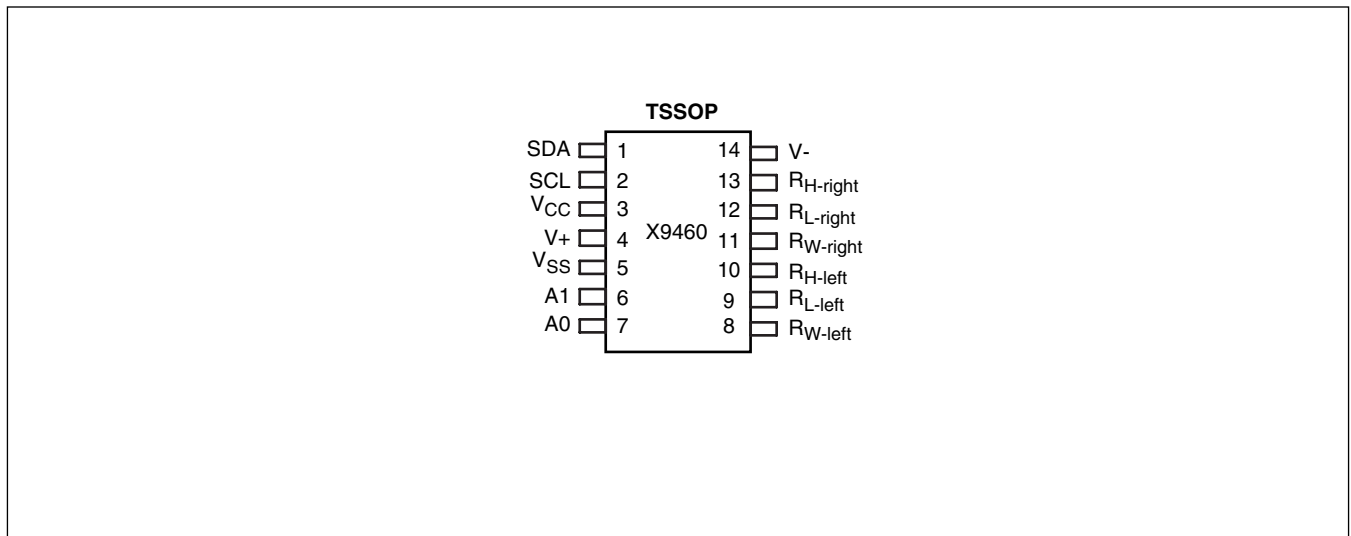
PIN ASSIGNMENTS

Pin (TSSOP)	Symbol	Function
1	SDA	Serial Data
2	SCL	Serial Clock
3	V_{CC}	System Supply Voltage
4	V+	Positive Analog Supply
5	V_{SS}	System Ground
6	A1	Device Address
7	A0	Device Address
8	$R_{W\text{-left}}$	Wiper terminal of the Left Potentiometer
9	$R_{L\text{-left}}$	Negative terminal of the Left Potentiometer
10	$R_{H\text{-left}}$	Positive terminal of the Left Potentiometer
11	$R_{W\text{-right}}$	Wiper terminal of the Right Potentiometer
12	$R_{L\text{-right}}$	Negative terminal of the Right Potentiometer
13	$R_{H\text{-right}}$	Positive terminal of the Right Potentiometer
14	V-	Negative Analog Supply

DETAILED PIN DESCRIPTION:

Host Interface Pins

SERIAL CLOCK **(SCL)**

The SCL input clocks data into and out of the X9460.

SERIAL DATA **(SDA)**

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the guidelines for calculating typical values on the bus pull-up resistors graph.

DEVICE ADDRESS **(A$_1$- A$_0$)**

The Address inputs are used to set the least significant 2 bits of the 8-bit Slave Byte Address. A match in the slave address serial data stream must be made with the Address input in order to initiate communication with the X9460. Up to 4 X9460s may be directly connected to a single I2C serial bus. If left floating, these pins are internally pulled to ground.

Slave Byte (bits, MSB-LSB) = 0101 0 A$_1$ A$_0$ R/W

Potentiometer Pins

R$_{H\text{-LEFT}}$, R$_{L\text{-LEFT}}$, R$_{H\text{-RIGHT}}$, R$_{L\text{-RIGHT}}$

The R$_H$ and R$_L$ inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

R$_{W\text{-LEFT}}$, R$_{W\text{-RIGHT}}$

The wiper outputs are equivalent to the wiper output of a mechanical potentiometer.

Supply Pins

ANALOG SUPPLY **V- AND V+**

The positive power supply for the DCP analog control section is connected to V+. The negative power supply for the DCP analog control section is connected to V-.

Digital Supplies V$_{CC}$, V$_{SS}$

The power supplies for the digital control sections.

Power Up and Down Recommendations

There are no restrictions on the power-up condition of V$_{CC}$, V+ and V- and the voltages applied to the potentiometer pins provided that the Vcc and V+ are more positive or equal to the voltage at RH, RL , and Rw, ie. Vcc, V+ > RH, RL, Rw. At all times, the voltages on the potentiometer pins must be less than V+ and more than V-.

The following V$_{CC}$ ramp rate spec is always in effect.

$$0.2 \text{ V/ms} < V_{CC} \text{ ramp} < 50 \text{ V/ms}$$

The V$_{SS}$ pin is always connected to the system common or ground. V$_H$, V$_L$, V$_W$ are the voltages on the R$_H$, R$_L$, and R$_W$ potentiometer pins.

X9460 PRINCIPLES OF OPERATION

The X9460 is a highly integrated microcircuit incorporating two resistor arrays with their associated registers, counters and the serial interface logic providing direct communication between the host and the DCP potentiometers. This section provides detailed description as following:

– Resistor Array Description
– Serial Interface Description
– Command Set and Register Information Description

RESISTOR ARRAY DESCRIPTION

The X9460 is comprised of two resistor arrays. Each array contains 31 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R$_H$ and R$_L$ inputs). Tables 1 and 2 provide a description of the step size and tap positions.

At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper (R$_W$) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by the Wiper Counter Register (WCR). The five bits of the WCR are decoded to select, and enable, one of thirty-two switches.

Table 1. Total -62dB range Plus Mute Position

Step Size	# of Steps
-1 dB	11 steps
- 2 dB	10 steps
- 3 dB	5 steps
- 4 dB	4 steps
Mute	1 step

Table 2. Wiper Tap Position vs dB.

Tap Position, n	dB	Min/Max dB
for n = 20 to 31	n - 31	-11 / 0
for n = 10 to 19	2n-51	-31 / -13
for n = 5 to 9	3n-61	-46 / -34
for n = 1 to 4	4n-66	-62 / -50
n = 0	-92	-92

SERIAL INTERFACE DESCRIPTION

Serial Interface

The X9460 supports a bidirectional bus oriented proto-col. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and pro-vide the clock for both transmit and receive operations. The X9460 is a slave device in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating start and stop condi-tions.

Start Condition

All commands to the X9460 are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The X9460 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

Stop Condition

All communications must be terminated by a stop con-dition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

Acknowledge

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting eight bits. The master generates a ninth clock cycle and dur-ing this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data.

The X9460 will respond with an acknowledge: 1) after recognition of a start condition and after an identifica-tion and slave address byte, and 2) again after each successful receipt of the instruction or databyte. See Figure 1.

Invalid Commands

For any invalid commands or unrecognizable addresses, the X9460 will NOT acknowledge and return the X9460 to the idle state.

## Figure 1. Acknowledge Response from Receiver
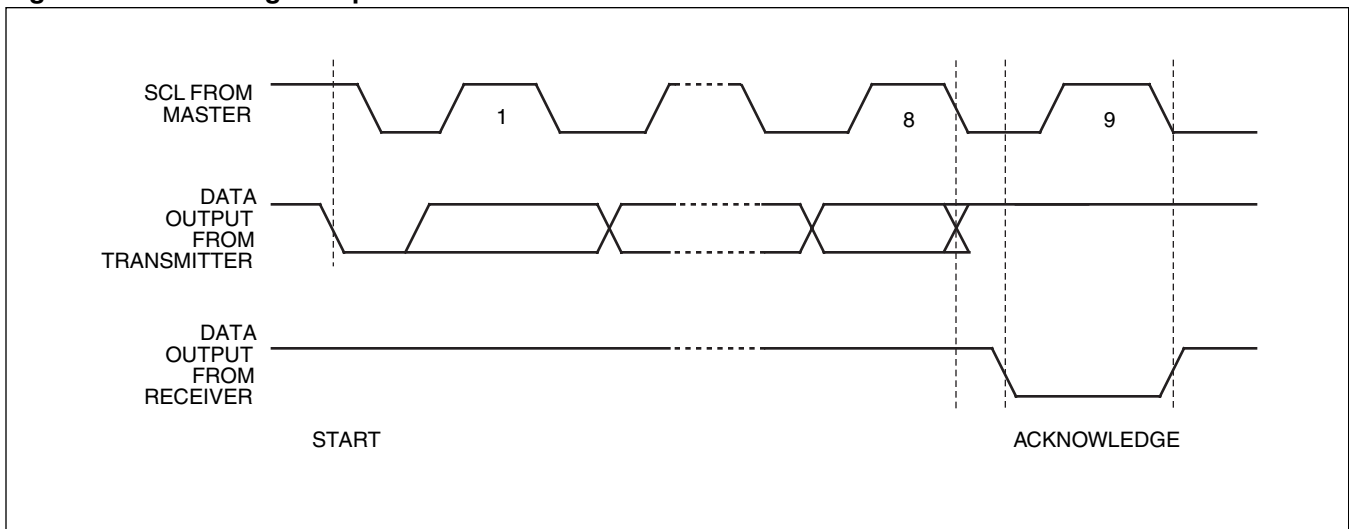
COMMAND SET AND REGISTER DESCRIPTION

DEVICE ADDRESSING

Following a start condition the master must output the Slave Byte Address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (refer to Figure 2 below). For the X9460 this is fixed as 0101.

Figure 2. Slave Byte Address

DEVICE TYPE IDENTIFIER					DEVICE ADDRESS		
0	1	0	1	0	A1	A0	R/$\overline{W}$
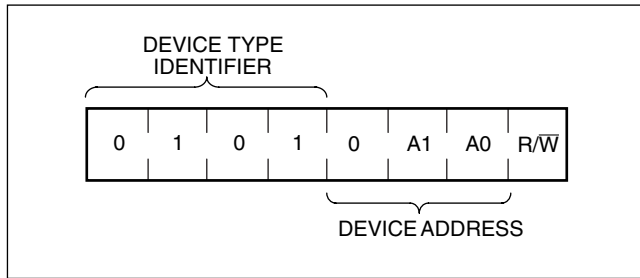
The next three bits of the Slave Byte Address are the device address. The device address is defined by the A_1–A_0 inputs. The X9460 compares the serial data stream with the Slave Byte Address; a successful compare is required for the X9460 to respond with an acknowledge. The A_1–A_0 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}. The R/$\overline{W}$ bit sets the device for read or write operations.

Command Set

After a Slave Byte Address match, the next byte sent contains the Command and register pointer information. The four most significant bits are the Command. The next bit is a "X" (don't care) set to zero.

Figure 3. Command Byte Format

this bit not used, set to 0

I3	I2	I1	I0	0	Z_D	RT	LT
INSTRUCTIONS					WIPER COUNTER SELECT		
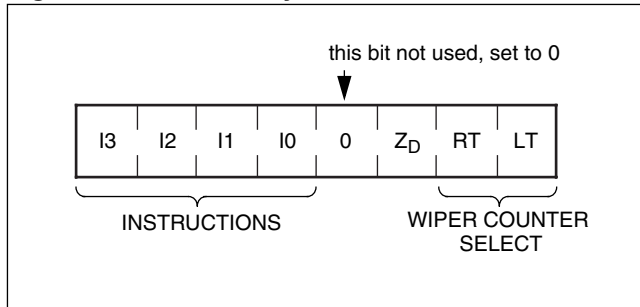
The Z_D bit enables and disables the Zero Amplitude Wiper Switching circuit. When Z_D=1, the wiper switches will turn on when close-to-zero amplitude is detected across the potentiometer pins. When Z_D=0, this circuit is disabled. The last two bits, LT (left POT enable) and RT (right POT enable), select which of the two potentiometers is affected by the instruction.

Several instructions require a three-byte sequence to complete. These instructions transfer data between the host and the X9460. These instructions are: Read Wiper Counter Register, Write Wiper Counter Register. The sequence of operations is shown in Figure 4 and 5. The four-byte command is used for write command for both right and left pots (Figure 6).

Special Commands

Increment / Decrement Instruction. The Increment/ Decrement command is different from the other commands. Once the command is issued and the X9460 has responded with an acknowledge, the master can clock the selected wiper up and/or down. For each SCL clock pulse (t_{HIGH}) while SDA is HIGH, the selected wiper will move one resistor segment towards the R_H terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the R_L terminal. A detailed illustration of the sequence and timing for this operation are shown in Figures 7 and 8 respectively.

Wiper Counter Register

The X9460 contains two Wiper Counter Registers. The Wiper Counter Register output is decoded to select one of thirty-two switches along its resistor array. The Write Wiper Counter Register command directly sets the WCR to a value. The Increment/Decrement instruction steps the register value up or down one to multiple times.

The WCR is a volatile register (Table 3) and is reset to the mute position (tap 0, "zero") at power-up.

Table 3. Wiper Counter Registers, 5-bit - volatile:

WCR4	WCR3	WCR2	WCR1	WCR0
(MSB)				(LSB)

The X9460 contains one 5-bit Wiper Counter Register for each DCP. (Two 5-bit registers in total.)

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Table 2a. Command Set

Instruction	Instruction Set								Operation
	I_3	I_2	I_1	I_0	X	Z_D	RT	LT	
Read Wiper									LSB of Slave Byte=1, no command required Slave will return Left then Right Data
Write Left Wiper Counter	1	0	1	0	0	1/0	0	1	Write new value to the Wiper Counter Register
Write Right Wiper Counter	1	0	1	0	0	1/0	1	0	Write new value to the Wiper Counter Register
Write Both Wiper Counters	1	0	1	0	0	1/0	1	1	Write new value to the Wiper Counter Register
Inc/Dec Left Wiper Counter	0	0	1	0	0	1/0	0	1	Enable Increment/decrement of the Control Latch
Inc/Dec Right Wiper Counter	0	0	1	0	0	1/0	1	0	Enable Increment/decrement of the Control Latch
Inc/Dec Both Wiper Counters	0	0	1	0	0	1/0	1	1	Enable Increment/decrement of the Control Latch

Notes: "1/0" = data is one or zero

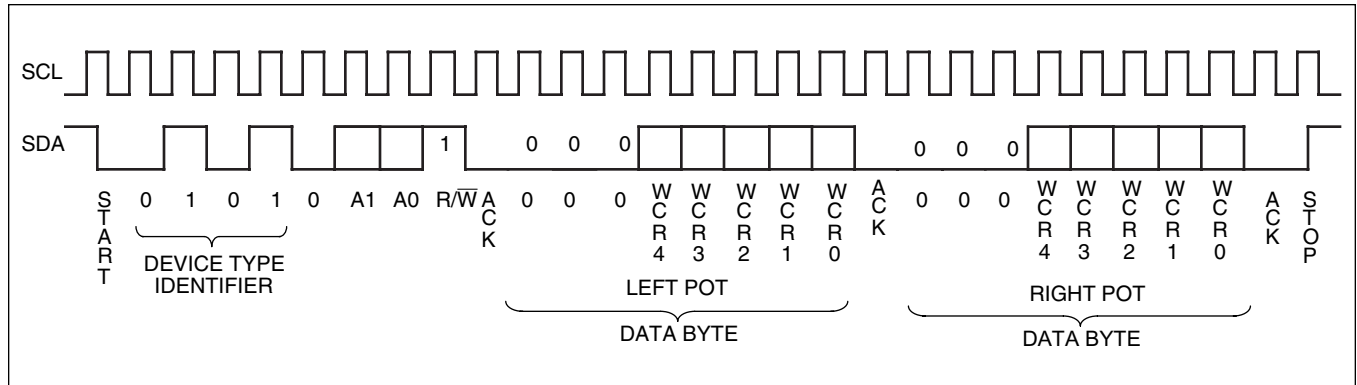## Figure 4. Three-Byte Command Sequence (Read)
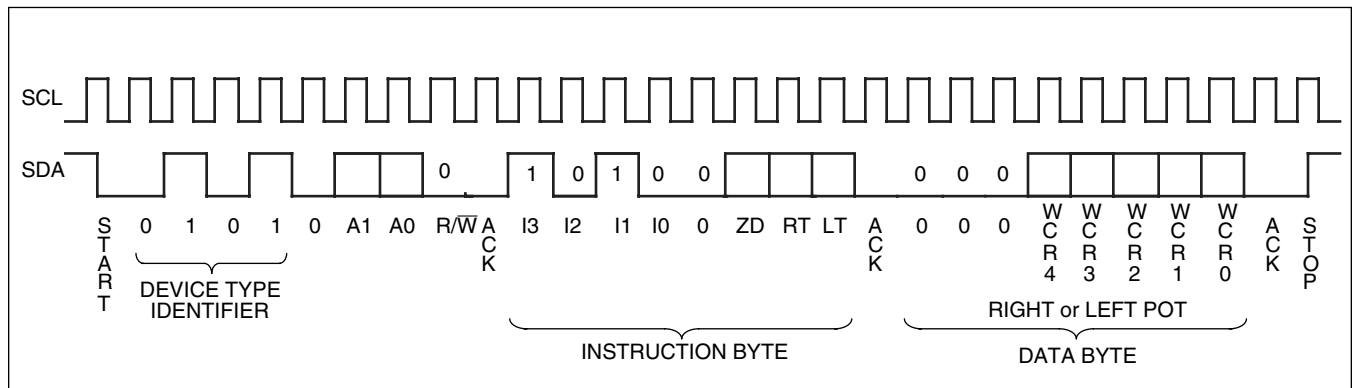

Figure 5. Three-Byte Command Sequence (Write)

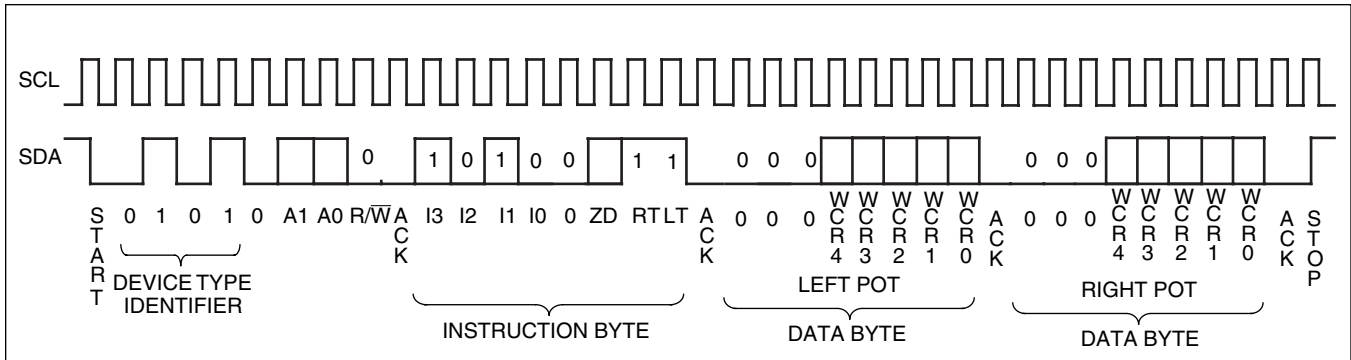**Figure 6. Four-Byte Command Sequence (Write)**

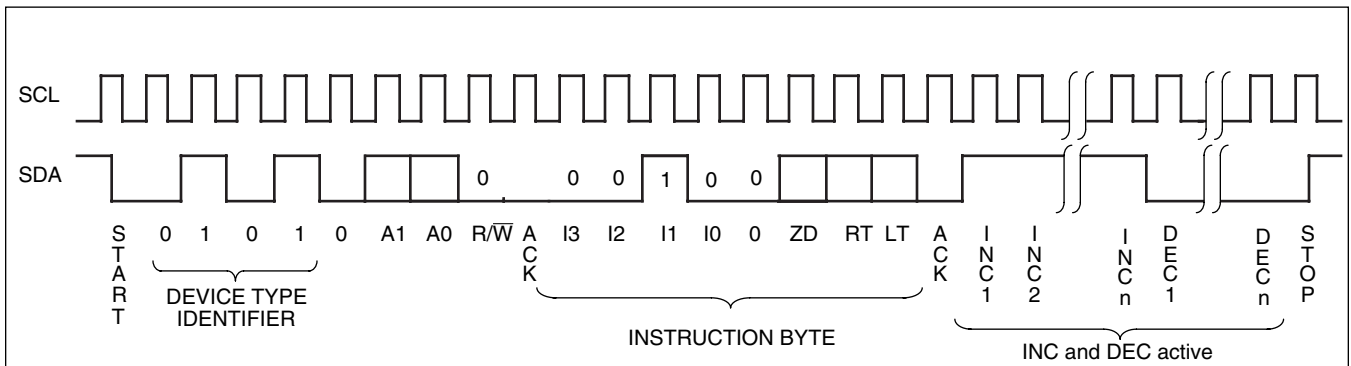**Figure 7. Increment/Decrement Command Sequence (Write)**

Figure 8. Increment/Decrement Timing Limits

Wiper can move within 10µsecs after the falling edge of SCL
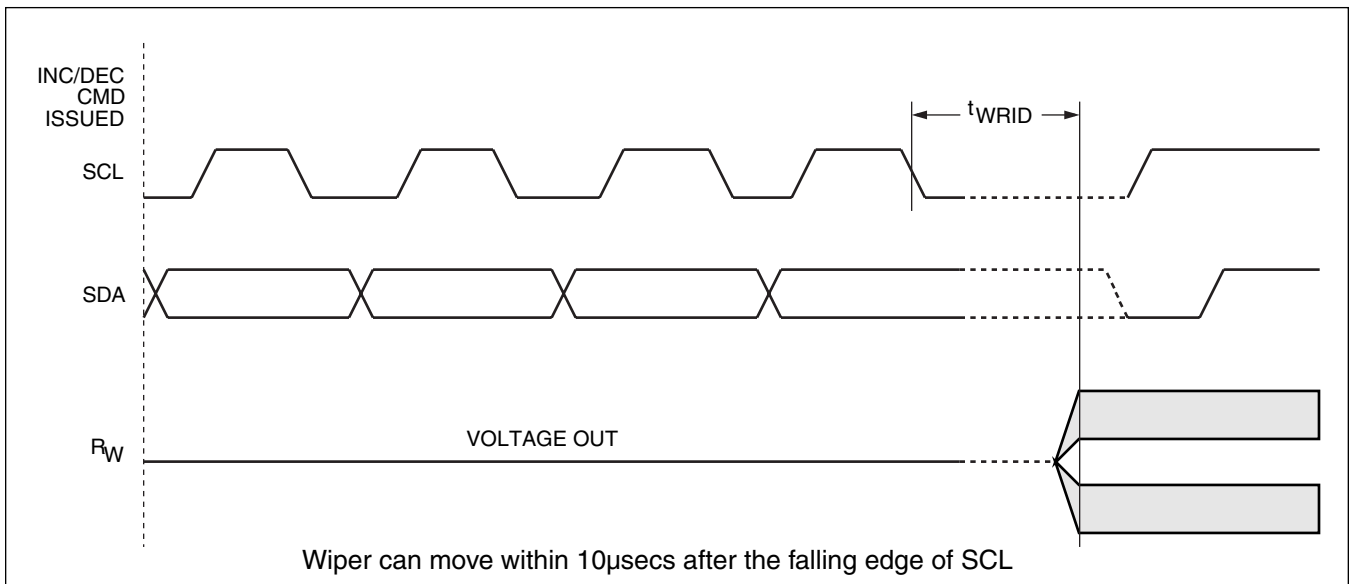
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INSTRUCTION FORMATS

Read Wiper Counter Register

START	device type identifier					device addresses			SACK	Left wiper position (sent by slave on SDA)								MACK	Right wiper position (sent by slave on SDA)								MACK	STOP
START	0	1	0	1	0	A1	A0	R/$\overline{W}$=1	SACK	0	0	0	LD4	LD3	LD2	LD1	LD0	MACK	0	0	0	RD4	RD3	RD2	RD1	RD0	MACK	STOP

Write Wiper Counter Register

START	device type identifier					device addresses			SACK	instruction opcode					wiper addresses			SACK	Left or Right wiper position (sent by master on SDA)								SACK	STOP
START	0	1	0	1	0	A1	A0	R/$\overline{W}$=0	SACK	1	0	1	0	0	ZD	RT	LT	SACK	0	0	0	D4	D3	D2	D1	D0	SACK	STOP

Write Both Wiper Counter Registers

START	device type identifier					device addresses			SACK	instruction opcode					wiper addresses			SACK	Left wiper position (sent by master on SDA)								SACK	Right wiper position (sent by master on SDA)								SACK	STOP
START	0	1	0	1	0	A1	A0	R/$\overline{W}$=0	SACK	1	0	1	0	0	ZD	1	1	SACK	0	0	0	LD4	LD3	LD2	LD1	LD0	SACK	0	0	0	RD4	RD3	RD2	RD1	RD0	SACK	STOP

Increment/Decrement Wiper Counter Register

START	device type identifier					device addresses			SACK	instruction opcode					wiper addresses			SACK	increment/decrement (sent by master on SDA)						STOP
START	0	1	0	1	0	A1	A0	R/$\overline{W}$=0	SACK	0	0	1	0	0	ZD	RT	LT	SACK	I/$\overline{D}$	I/$\overline{D}$	. . . .	I/$\overline{D}$	I/$\overline{D}$			STOP

Definitions:

(1) "MACK"/"SACK": stands for the acknowledge sent by the master/slave.
(2) "A1 ~ A0": stands for the device addresses sent by the master.
(3) "I": stands for the increment operation, SDA held high during active SCL phase (high).
(4) "D": stands for the decrement operation, SDA held low during active SCL phase (high).

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ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias .... -65°C to +135°C
Storage Temperature.........................–65°C to +150°C
Voltage on SDA, SCL or any Address Input
    with Respect to V_{SS} ....–1V to +6V
Voltage on V+ (referenced to V_{SS})........................ +6V
Voltage on V- (referenced to V_{SS})........................... -6V
(V+) – (V-)... 12V
Any R_H .... V+
Any R_L .... V-
Lead Temperature (Soldering, 10 seconds) ...... 300°C
I_W max (10 secs)... ± 3mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Industrial	–40°C	+85°C

Device	Supply Voltage (V_{CC})	V- Limits	V+ Limits
X9460V14–2.7	2.7V to 5.5V	-5.5V to -2.7V	+2.7V to +5.5V

ANALOG CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
Dynamic Performance[2][3]						
	Control Range	-62		0	dB	
	Mute Mode		-92		dB	@1V rms
SNR	Signal Noise Ratios (Unweighted)		-96		dB	@1V rms @ 1kHz, Tap = -6dB
THD + N	Total Harmonic Distortion + Noise		-95		dB	@1V rms @ 1kHz, Tap = -6dB
XTalk	DCP Isolation		-102		dB	@1kHz, tap = -6dB
	Digital Feedthrough (Peak Component)		-105		dB	tap = -6dB
	-3db Cutoff Frequency		100		kHz	
DC Accuracy						
	Step Size	-1		-4	dB	Steps of -1, -2, -3, -4 dB
	Step Size Error	-0.2		+0.2	dB	For -1dB steps
	Step Size Error	-0.4		+0.4	dB	For -2dB steps
	Step Size Error	-0.6		+0.6	dB	For -3dB steps
	Step Size Error	-0.8		+0.8	dB	For -4dB steps
	DCP to DCP Matching	-0.1		0.1	dB	

Notes: (1) V_{CC} = | V- |
    V_{CC} Ramp up timing 0.2 V/ms < Vcc Ramp Rate < 50 V/ms
(2) This parameter is guaranteed by design and characterization
(3) T_A = 25°C, V_{CC} = 5.0V; 20 Hz to 20kHz Measurement Bandwidth with 80kHZ filter, input signal 1Vrms, 1kHz Sine Wave.

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ANALOG CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)[1]

	ANALOG INPUTS					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test Conditions**
V_{TERM}	Voltage on R_L, R_W, and R_H pins	V-		V+	V	
R_{TOTAL}	End to End Resistance	-20		+20	%	Typical 33KΩ
Cin[4]	Input Capacitance R_L, R_H, R_W		25		pF	T_A = 25ºC
I_W[2]	Wiper Current	-3		+3	mA	
R_W	Wiper Resistance		100	200	Ω	Wiper Current = ± 3mA
V-	Voltage on V- pin	-5.5		-2.7	V	
V+	Voltage on V+ pin	+2.7		+5.5	V	
	Noise		2		μVrms	20 HZ to 20KHZ, Grounded Input @ -6dB tap
TC_R[2]	Temperature Coefficient of resistance		-300		PPM/°C	

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)[1]

		Limits				
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
I_{CC1}	V_{CC} Supply Current (Move Wiper, Write, Read)		200	300	μA	f_{SCL} = 400kHz, SDA = Open, Other Inputs = V_{SS}
I_{SB}	V_{CC} Current (Standby)		3		μA	SCL = SDA = V_{CC}, Addr. = V_{SS}
I_{LI}	Input Leakage Current		1	10	μA	V_{IN} = V_{SS} to V_{CC}
Iai	Analog Input Leakage		0.1		μA	V_{IN} = V- to V+ with all other analog inputs floating
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = V_{SS} to V_{CC}
V_{IH}	Input HIGH Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{IL}	Input LOW Voltage	−0.5		V_{CC} x 0.1	V	
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3mA

CAPACITANCE

Symbol	**Test**	**Max.**	**Units**	**Test Conditions**
$C_{I/O}$[4]	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}[4]	Input Capacitance (A0, A1, A2 and SCL)	6	pF	V_{IN} = 0V

Notes: (4) This parameter is not 100% tested.

A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

EQUIVALENT A.C. LOAD CIRCUIT
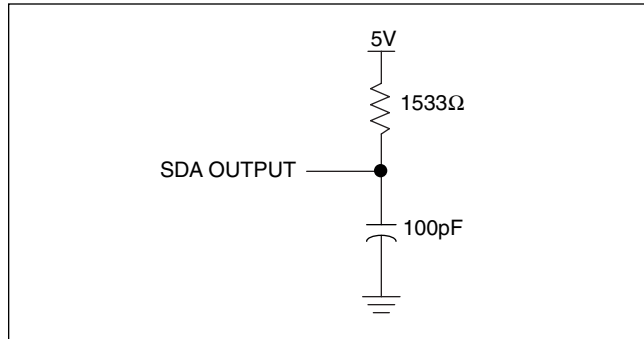
AC TIMING (Over recommended operating conditions)

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	Clock Frequency		400	kHz
t_{CYC}	Clock Cycle Time	2500		ns
t_{HIGH}	Clock High Time	600		ns
t_{LOW}	Clock Low Time	1300		ns
$t_{SU:STA}$	Start Setup Time	600		ns
$t_{HD:STA}$	Start Hold Time	600		ns
$t_{SU:STO}$	Stop Setup Time	600		ns
$t_{SU:DAT}$	SDA Data Input Setup Time	500		ns
$t_{HD:DAT}$	SDA Data Input Hold Time	50		ns
t_R[2]	SCL and SDA Rise Time		300	ns
t_F[2]	SCL and SDA Fall Time		300	ns
t_{AA}[2]	SCL Low to SDA Data Output Valid Time		900	ns
t_{DH}[2]	SDA Data Output Hold Time	50		ns
T_I[2]	Noise Suppression Time Constant at SCL and SDA inputs	50		ns
t_{BUF}[2]	Bus Free Time (Prior to Any Transmission)	1300		ns
$t_{SU:WPA}$	A0, A1[2]	0		ns
$t_{HD:WPA}$	A0, A1[2]	0		ns

DCP TIMING[2]

Symbol	Parameter	Min.	Max.	Units
t_{WRPO}	Wiper Response Time After The Third (Last) Power Supply Is Stable		10	µs
t_{WRL}	Wiper Response Time After Instruction Issued (All Load Instructions)		10	µs
t_{WRID}	Wiper Response Time From An Active SCL Edge (Increment/Decrement Instruction)		10	µs

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TIMING DIAGRAMS

Figure 9. START and STOP Timing
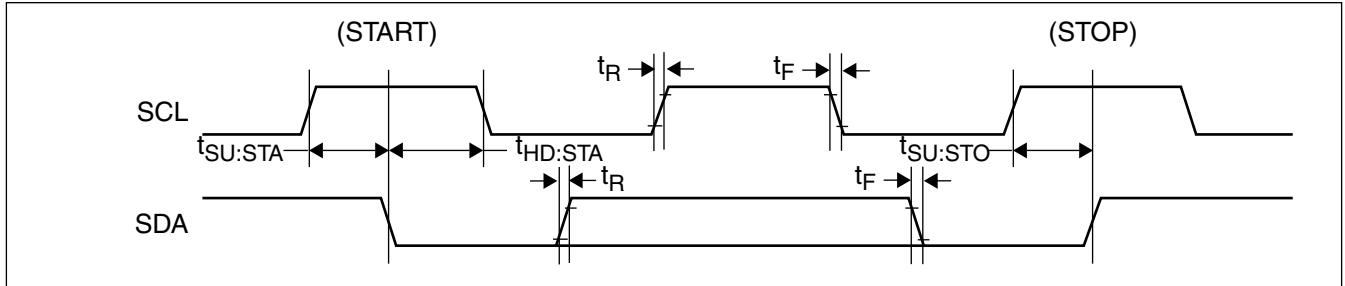
Figure 10. Input Timing
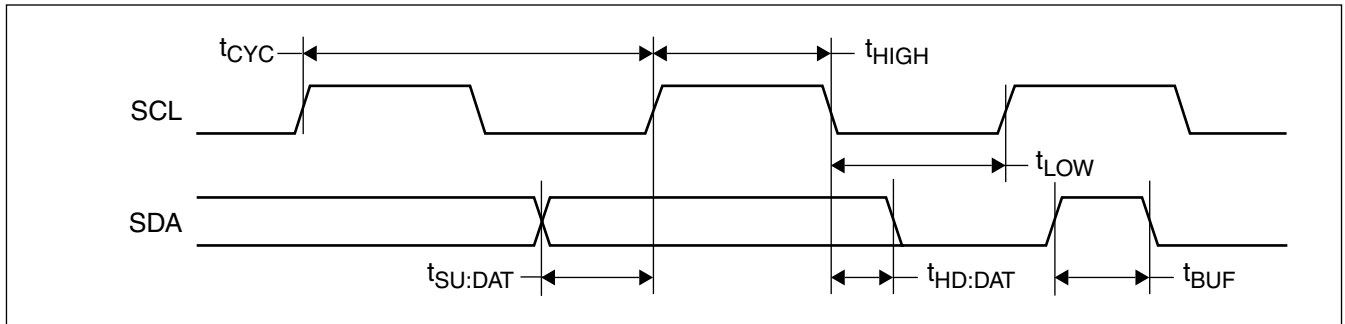
Figure 11. Output Timing
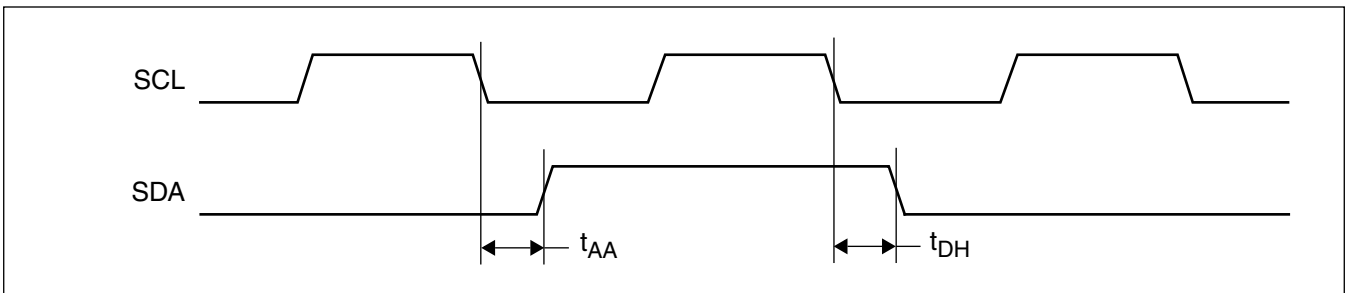
Figure 12. DCP Timing (for All Load Instructions)
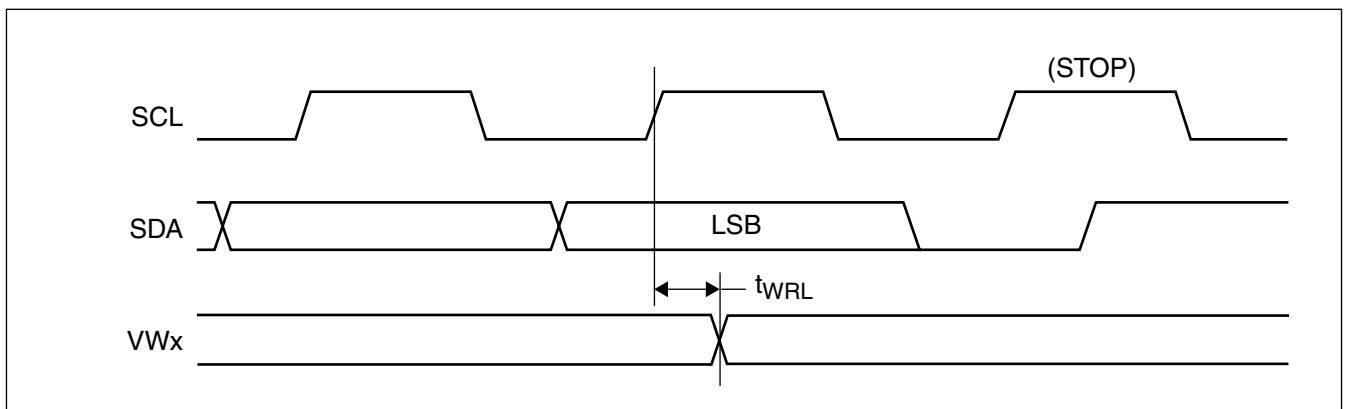
X9460

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{CC},V+ = 5.0V,V- = -5.0V, T_A = + 25 °C, unless otherwise noted)

FFT Spectrum
(with 1kHz 1Vrms input, tap = -6dB)
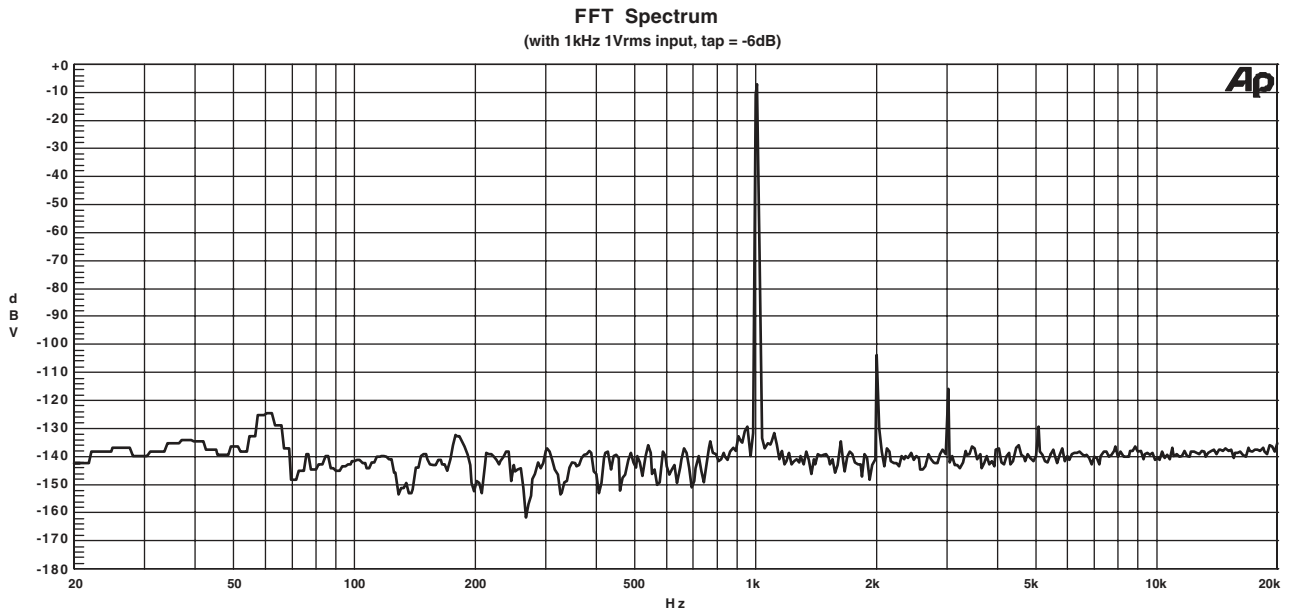
Figure 13. Single Tone Frequency Response

THD+N vs Frequency
(with 80kHz low-pass filter, tap = -6dB)
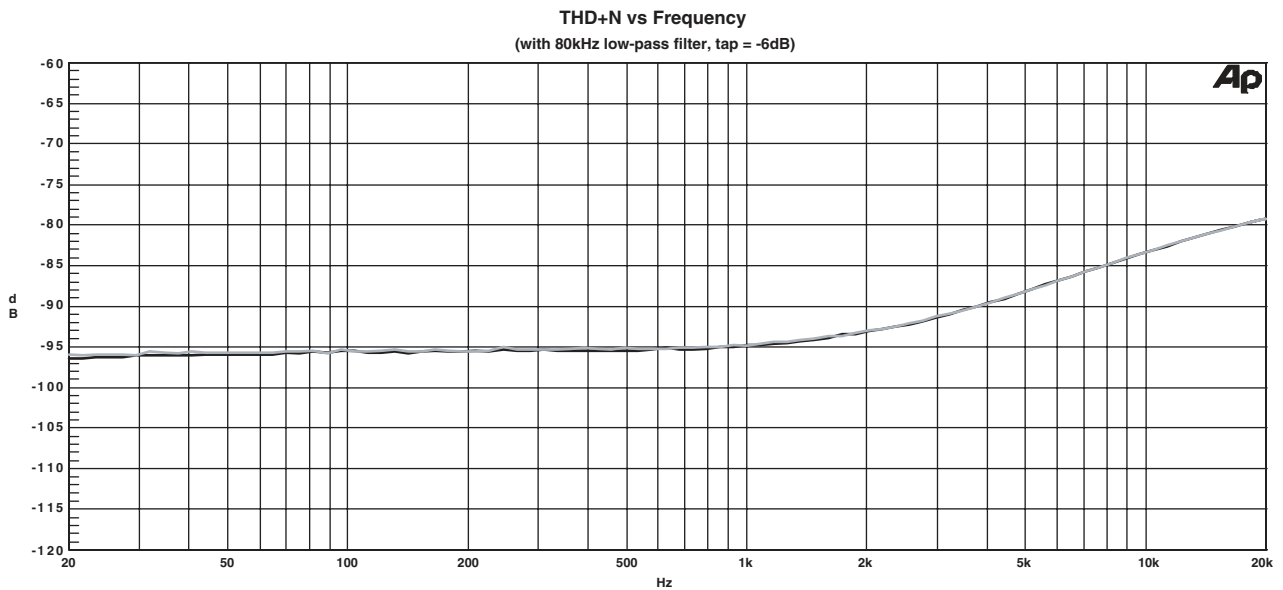
Figure 14. THD + N

X9460

TYPICAL PERFORMANCE CHARACTERISTICS
(V_{CC},V+ = 5.0V,V- = -5.0V, T_A = + 25 °C, unless otherwise noted)

Mute Mode
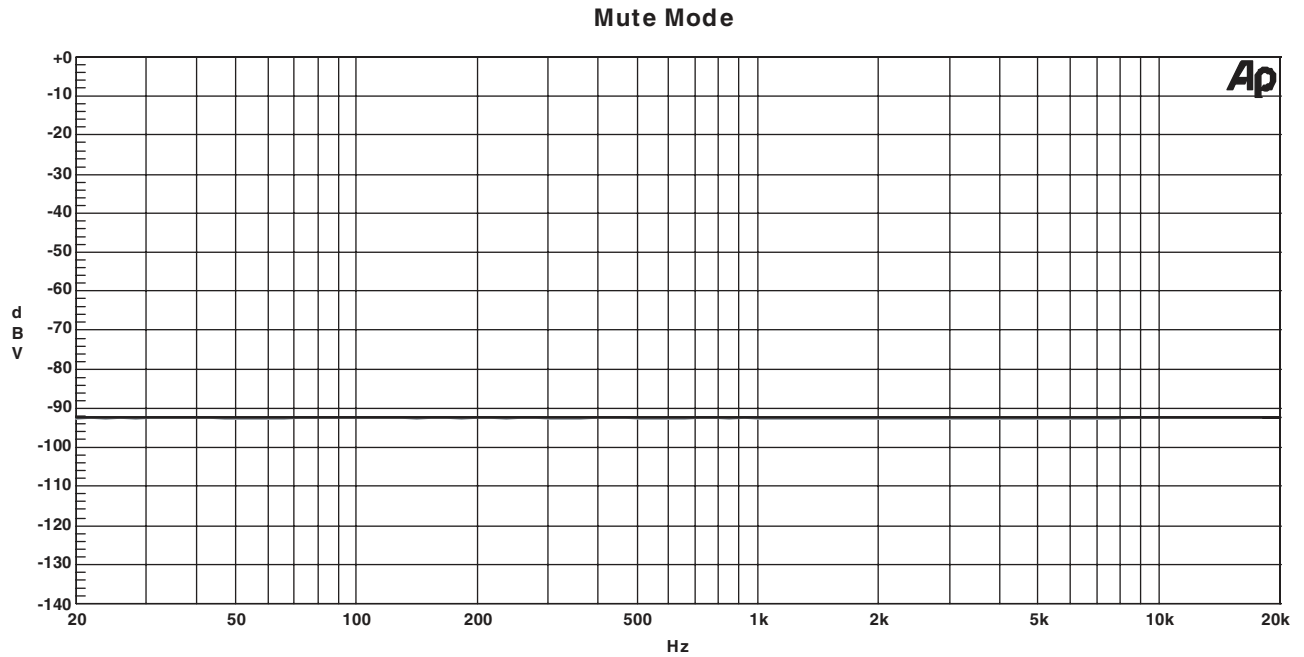
Figure 15. Mute

PACKAGING INFORMATION

14-Lead Plastic, TSSOP, Package Type V

.025 (.65) BSC

$\frac{.169 (4.3)}{.177 (4.5)}$ .252 (6.4) BSC

$\frac{.193 (4.9)}{.200 (5.1)}$

.047 (1.20)

$\frac{.0075 (.19)}{.0118 (.30)}$

$\frac{.002 (.05)}{.006 (.15)}$

.010 (.25)

Gage Plane

Seating Plane

0° - 8°

$\frac{.019 (.50)}{.029 (.75)}$

Detail A (20X)

.031 (.80)
$\frac{}{.041 (1.05)}$

See Detail "A"
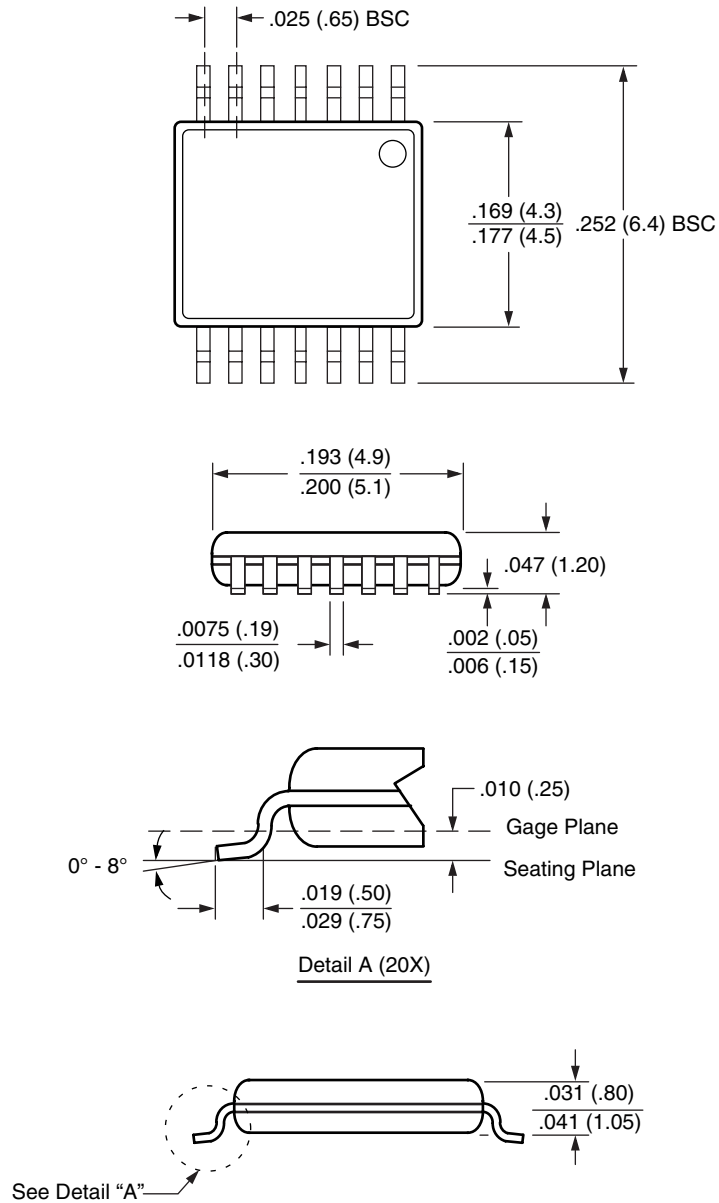
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

X9460

ORDERING INFORMATION

X9460   K   P   T   V

Device

V$_{CC}$ Limits
Blank = 5V ± 10%
-2.7 = 2.7 to 5.5V

Temperature Range
Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C

Package
V14 = 14-Lead TSSOP

Potentiometer Organization

	Left Pot	Right Pot
K =	33KΩ ± 20%	33KΩ ± 20%
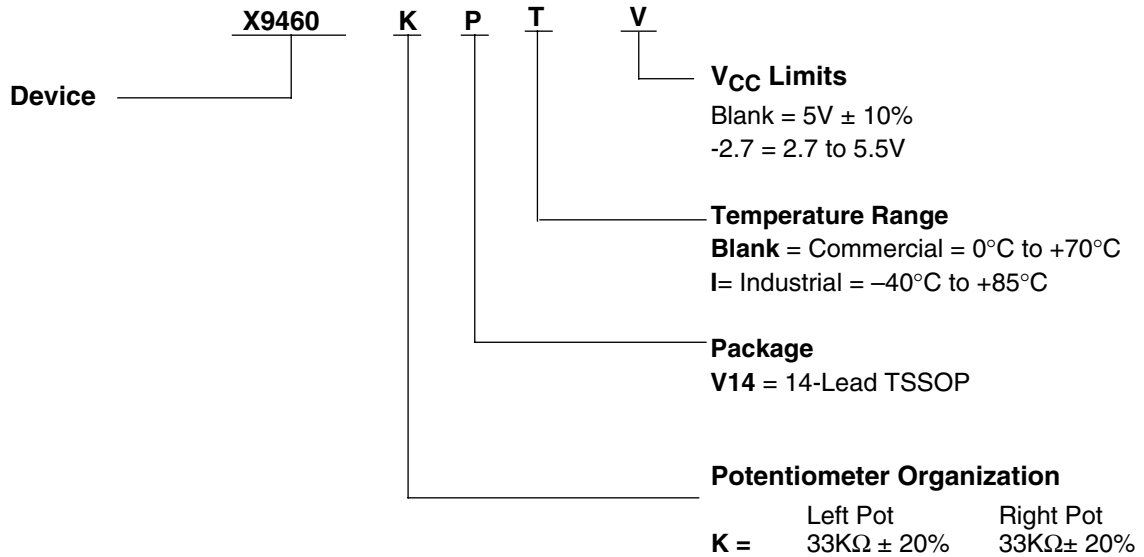
X9460 TSSOP 14L Top Mark Instructions

	Commercial	Industrial
5.0 volt	**X9460KV** **EYWW**	**X9460KV** **EYWW I**
2.7 volt	**X9460KV** **EYWW F**	**X9460KV** **EYWW G**