



CS3844B

Preliminary

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Current Mode PWM Control Circuit with 50% Max Duty Cycle

Description

The CS3844B provides all the necessary features to implement off-line fixed frequency current-mode control with a minimum number of external components.

The CS3844B incorporates a precision temperature-controlled oscillator to minimize variations in frequency. An internal toggle flip-flop, which blanks the output off every other clock cycle, limits the duty-cycle range to less than

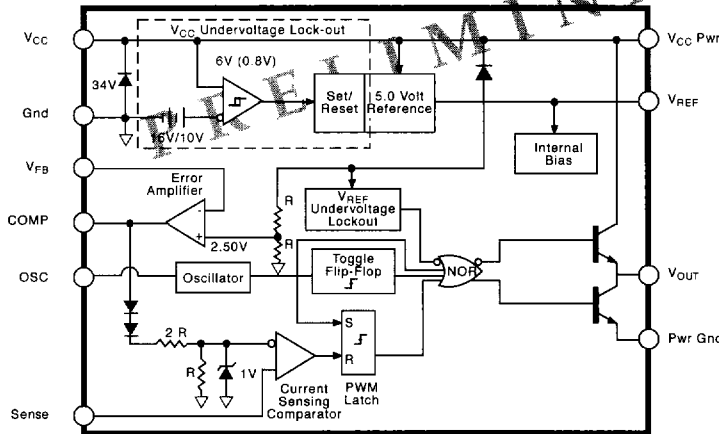
50%. An undervoltage lockout ensures that V_{REF} is stabilized within specification before the output stage is enabled. The CS3844B has been optimized for lower start up current (600 μ A max).

Other features include 1% trimmed band gap reference, pulse-by-pulse current limiting, and a high-current totem pole output for driving capacitive loads.

Absolute Maximum Ratings

Supply Voltage ($I_{CC} < 30mA$)	Self Limiting
Supply Voltage (Low Impedance Source)	30V
Output Current	$\pm 1A$
Output Energy (Capacitive Load)	5 μ J
Analog Inputs (V_{FB} , V_{Sense})	-0.3V to 5.5V
Error Amp Output Sink Current	10mA
Lead Temperature Soldering	
Wave Solder (through hole styles only)	10 sec. max, 260°C peak
Reflow (SMD styles only)	60 sec. max above 183°C, 230°C peak

Block Diagram



Features

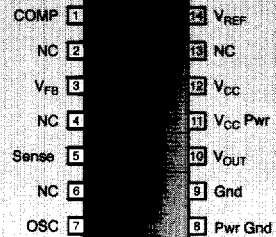
- Undervoltage Lockout
- 50% Max Duty Cycle
- Down
- Double Pulse Suppression
- 1% Trimmed Bandgap Reference
- High Current Totem Pole Output

Package Options

8 Lead PDIP & SO



14 Lead SO Narrow



Electrical Characteristics: $0 \leq V_A \leq 70^\circ\text{C}$, $V_{CC} = 15\text{V}$ (Note 1); $R_I = 10\text{k}\Omega$, $C_L = 3.3\mu\text{F}$ for sawtooth mode, unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	$T_J = 25^\circ\text{C}$, $I_{REF} = 1\text{mA}$	4.90	5.00	5.10	V
Line Regulation	$12 \leq V_{CC} \leq 25\text{V}$		6	20	mV
Load Regulation	$1 \leq I_{REF} \leq 20\text{mA}$		6	25	mV
Temperature Stability	(Note 1)		0.2	0.4	mV/ $^\circ\text{C}$
Total Output Variation	Line, Load, Temp. (Note 1)	4.82		5.18	V
Output Noise Voltage	$10\text{Hz} \leq f \leq 10\text{kHz}$, $T_J = 25^\circ\text{C}$ (Note 1)		50		μV
Long Term Stability	$T_A = 125^\circ\text{C}$, 1000 Hrs. (Note 1)		5	25	mV
Output Short Circuit	$T_A = 25^\circ\text{C}$	-30	-100	-180	mA
Oscillator Section					
Initial Accuracy	Sawtooth Mode, $T_J = 25^\circ\text{C}$	47	52	57	kHz
Voltage Stability	$12 \leq V_{CC} \leq 25\text{V}$		0.2	1.0	%
Temperature Stability	Sawtooth Mode $T_{MIN} \leq T_A \leq T_{MAX}$		5		%
Amplitude	V_{OSC} (peak to peak)		1.7		V
Error Amp Section					
Input Voltage	$V_{COMP} = 2.5\text{V}$	2.42	2.50	2.58	V
Input Bias Current	$V_{FB} = 0\text{V}$		-0.3	-2.0	μA
AVOL	$2 \leq V_{OUT} \leq 4\text{V}$	65	90		dB
Unity Gain Bandwidth	(Note 2)	0.7	1.0		MHz
PSRR	$12 \leq V_{CC} \leq 25\text{V}$	60	70		dB
Output Sink Current	$V_{FB} = 2.7\text{V}$, $V_{COMP} = 1.1\text{V}$	2	6		mA
Output Source Current	$V_{FB} = 2.3\text{V}$, $V_{COMP} = 5\text{V}$	0.5	-0.8		mA
V_{OUT} HIGH	$V_{FB} = 2.3\text{V}$, $R_L = 15\text{k}\Omega$ to GND	5	6		V
V_{OUT} LOW	$V_{FB} = 2.7\text{V}$, $R_L = 15\text{k}\Omega$ to V_{REF}		0.7	1.1	V
Current Sense Section					
Gain	(Notes 2&3)	2.85	3.00	3.15	V/V
Maximum Input Signal	$V_{COMP} = 5\text{V}$ (Note 2)	0.9	1.0	1.1	V
PSRR	$12 \leq V_{CC} \leq 25\text{V}$ (Note 2)		70		dB
Input Bias Current	$V_{SENSE} = 0\text{V}$		-2	-10	μA
Delay to Output	$T_J = 25^\circ\text{C}$ (Note 1)		150	300	ns
Output Section					
Output Low Level	$I_{SINK} = 20\text{mA}$		0.1	0.4	V
	$I_{SINK} = 200\text{mA}$		1.5	2.2	V
Output High Level	$I_{SOURCE} = 20\text{mA}$	13.0	13.5		V
	$I_{SOURCE} = 200\text{mA}$	12.0	13.5		V
Rise Time	$T_J = 25^\circ\text{C}$, $C_L = 1\text{nF}$ (Note 2)		50	150	ns
Fall Time	$T_J = 25^\circ\text{C}$, $C_L = 1\text{nF}$ (Note 2)		50	150	ns

Electrical Characteristics: continued

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
■ Total Standby Current					
Start-Up Current			400	600	μA
Operating Supply Current	$V_{FB} = V_{Sense} = 0V, R_T = 10k\Omega, C_T = 3.3nF$		11	17	mA
V_{CC} Zener Voltage	$I_{CC} = 25mA$		34		V
■ PWM Section					
Maximum Duty Cycle		46	48	50	%
Minimum Duty Cycle				0	%
■ Under-Voltage Lockout Section					
Start Threshold		14.5	16.0	17.5	V
Min. Operating Voltage	After Turn On	8.5	10.0	11.5	V

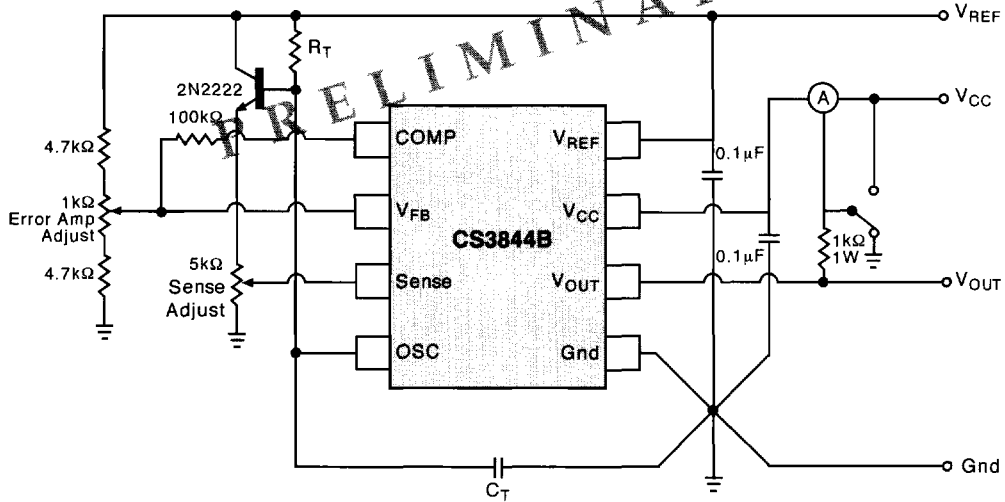
Notes: 1. These parameters, although guaranteed, are not 100% tested in production.

2. Parameter measured at trip point of latch with $V_{FB}=0$

3. Gain defined as: $A = \frac{\Delta V_{COMP}}{\Delta V_{Sense}}; 0 \leq V_{Sense} \leq 0.8V.$

Package Pin Description

PACKAGE PIN #		PIN SYMBOL	FUNCTION
8L PDIP & SO	14L SO		
1	1	COMP	Error amp output, used to compensate error amplifier
2	3	V_{FB}	Error amp inverting input
3	5	Sense	Noninverting input to Current Sense Comparator
4	7	OSC	Oscillator timing network with capacitor to Gnd, resistor to V_{REF}
5	9	Gnd	Ground
6	10	V_{OUT}	Output drive pin
7	12	V_{CC}	Positive power supply
8	14	V_{REF}	Output of 5V internal reference
	8	Pwr Gnd	Output driver Gnd
	11	V_{CC} Pwr	Output driver positive supply
	2, 4, 6, 13	NC	No Connection



Circuit Description

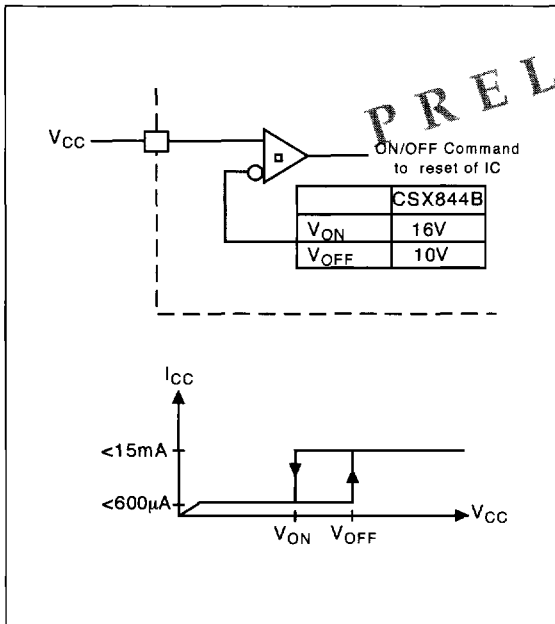


Figure 1: Typical Undervoltage Characteristics

Undervoltage Lockout

During Undervoltage Lockout (Figure 1), the output driver is biased to sink minor amounts of current. The output should be shunted to ground with a resistor to prevent activating the power switch with extraneous leakage currents.

PWM Waveform

To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal which represents the peak output inductor current (Figure 2). An increase in V_{CC} causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed-forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.

When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exceed the maximum allowed to prevent transformer saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of OSC components.

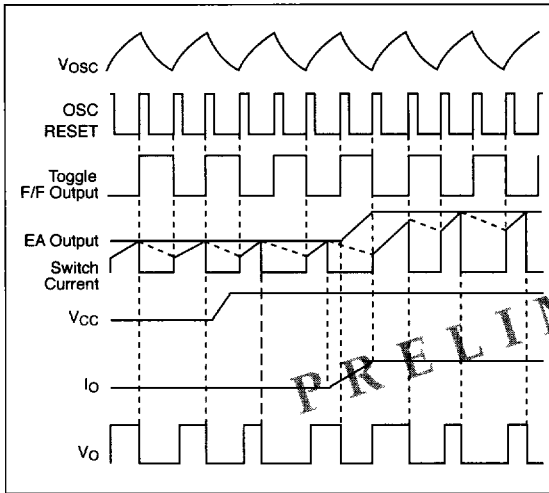


Figure 2: Timing Diagram

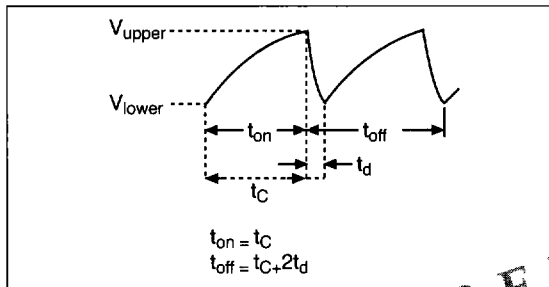


Figure 3: Timing Parameters

Setting the Oscillator

The values for t_c and t_d are determined from the formulas:

$$t_c = R_T C_T \ln \left(\frac{V_{REF} - V_{lower}}{V_{REF} - V_{upper}} \right)$$

$$t_d = R_T C_T \ln \left(\frac{V_{REF} - I_d R_T - V_{lower}}{V_{REF} - I_d R_T - V_{upper}} \right)$$

Substituting in typical values for the parameters in:

$$V_{REF} = 5.0V, V_{upper} = 2.7V, V_{lower} = 1.0V, I_d = 8.3mA,$$

then

$$t_c = 0.5534 R_T C_T$$

$$t_d = R_T C_T \ln \left(\frac{2.3 - 0.0083 R_T}{4.0 - 0.0083 R_T} \right)$$

For better accuracy R_T should be $\geq 10k\Omega$.

Grounding

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Gnd in a single point ground.

The transistor and 5k Ω potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Sense.

Package Specification

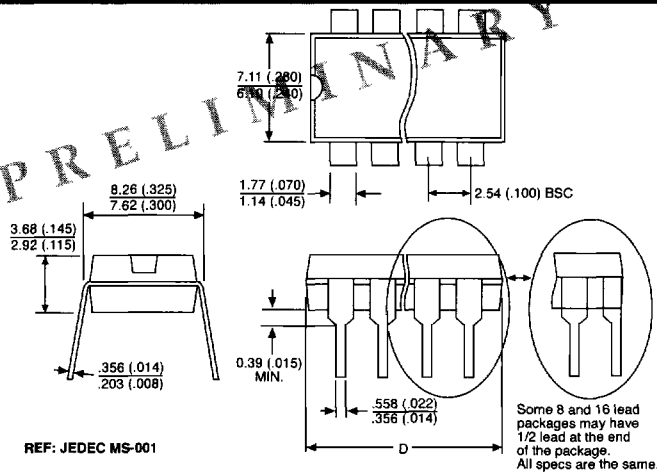
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
8L PDIP	10.16	9.02	.400	.355
8L SO Narrow	5.00	4.80	.197	.189
14L SO Narrow	8.75	8.55	.344	.337

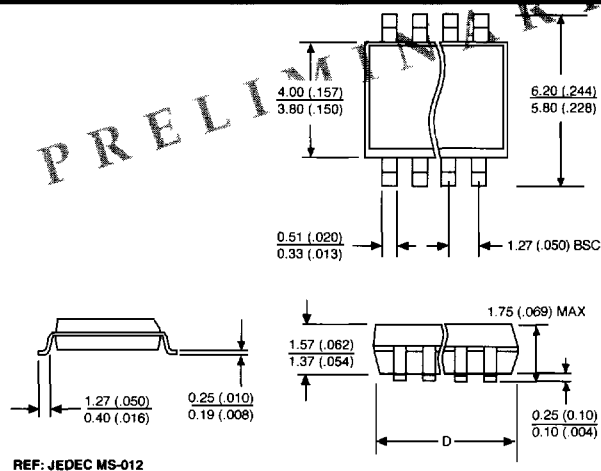
PACKAGE THERMAL DATA

Thermal Data		8 L	8L	14 L	
		PDIP	SO	SO	
RQ _{IC}	typ	52	45	30	°C/W
RQ _{JA}	typ	100	165	125	°C/W

Plastic DIP (N); 300 mil wide



Surface Mount Narrow Body (D); 150 mil wide



Ordering Information

Part Number	Description
CS3844BGN8	8L PDIP
CS3844BGD8	8L SO
CS3844BGDR8	8L SO (tape & reel)
CS3844BGD14	14L SO
CS3844BGDR14	14L SO (tape & reel)

Preliminary

This product is in the preproduction stages of the design process. The data sheet contains preliminary data. Cherry Semiconductor Corporation reserves the right to make changes to the specifications without notice. Please contact Cherry Semiconductor Corporation for the latest available information.