



A Product Line of
Diodes Incorporated



SPECIFICATION FOR APPROVAL

CUSTOMER _____

NOMINAL FREQUENCY _____ 135.000000 MHz _____

PRODUCT TYPE _____ TYPE NX 3.2x2.5 SEAM SEALED CRYSTAL CLOCK OSCILLATOR _____

SPEC. NO. (P/N) _____ NX32D5001Q _____

CUSTOMER P/N _____

ISSUE DATE _____ February 27, 2018 _____

VERSION _____ A _____

APPROVED	PREPARED	QA

Diodes Incorporated

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- *Pb-free
- *RoHS Compliant
- *HF-Halogen Free
- *REACH Compliant
- *AEC-Q200 Compliant

TYPE NX 3.2x2.5 SEAM SEALED CRYSTAL CLOCK OSCILLATOR

NX32D5001Q

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ELECTRICAL SPECIFICATIONS

SRe Part Number : NX32D5001Q

Item	Symbol	Specifications	Units	Notes
Nominal Frequency	F ₀	135.000000	MHz	
Frequency Stability	FT	± 50	ppm	**See note
Operating Temperature Range	TR	-40 to +85	°C	
Supply Voltage	V _{CC}	+3.3 ± 5.0%	V	
Logic Type	LT	LVPECL		
Supply Current, Output Enabled	I _{CC/OE}	80	mA	Max.
Supply Current, Output Disabled	I _{CC/OD}	40	mA	Max.
Duty Cycle (Symmetry)	DC/SY	45 / 55	%	Measured 50% of Waveform
Rise / Fall Time	T _R /T _F	400	ps	Max. measured 20/80% of Waveform
Output Voltage "0" Level	V _{OL}	V _{CC} -1.55V	V	Max.
Output Voltage "1" Level	V _{OH}	V _{CC} -1.2V	V	Min.
Output Load		50Ω to V _{CC} -2V		
Jitter, Phase	RMS	1	ps	Max. 12KHz ~ 20MHz Frequency Band
Jitter, Accumulated	RMS(1-σ)	6	ps	Max. 20,000 Consecutive Periods
Jitter, Peak to Peak	Pk-Pk	40	ps	Max. 100,000 Random Periods
Storage Temperature Range		-55 to +125	°C	

※ This product doesn't include harmful substance that stipulated by SONY SS-00259 Level 1 and S-AT2-001 Level 1 standard. RoHS Compliant (Pb - Free).

**Stability includes all combinations of Operating Temperature, Load changes, rated Input (Supply) Voltage changes, Initial Calibration Tolerance (25°C), Aging (1 year at 25°C Average Effective Ambient Temperature), Shock and Vibration.

Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (Pin1), Output Enable	0.7V _{CC}			V	Or Open
Input Voltage (Pin1), Output Disable (low power standby)			0.3V _{CC}	V	Output is Hi-Z
Output Disable Delay			100	ns	
Output Enable Delay			100	ns	
Start Up Time			10	ms	

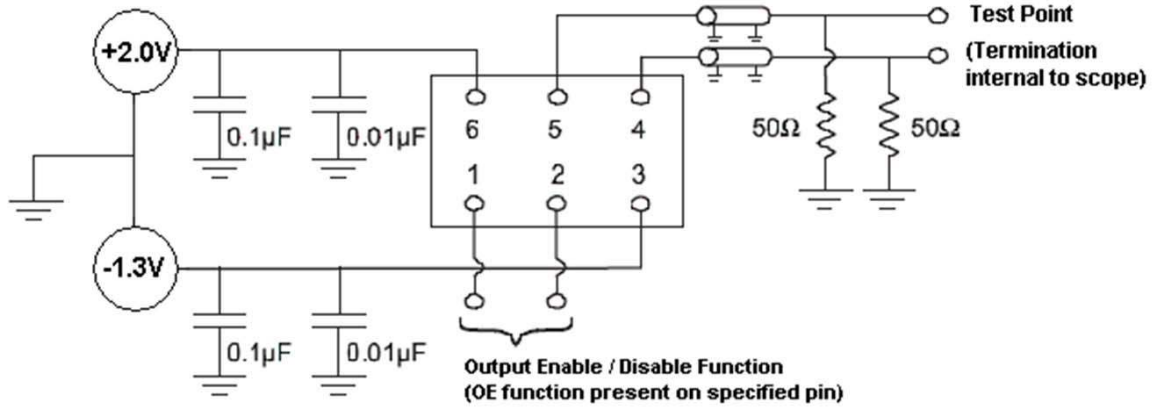


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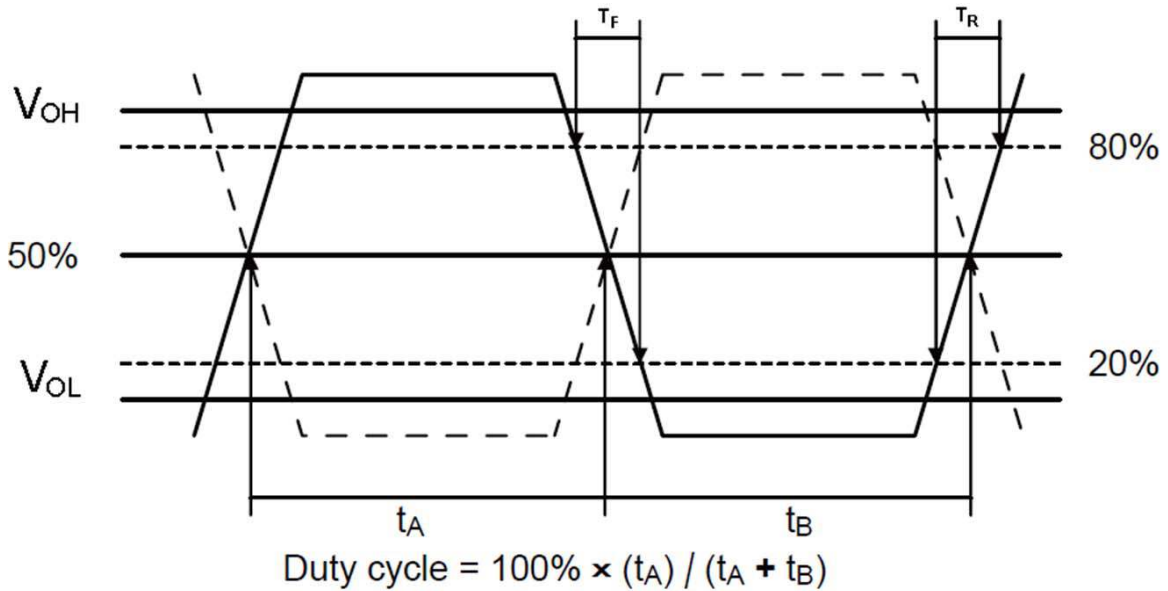
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TEST CIRCUIT



OUTPUT WAVEFORM



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AEC-Q200 RELIABILITY TEST SPECIFICATIONS:

1. Initial

- 1.1 Physical Dimensions: JESD22, Method JB1-100
- 1.2 External Visual: MIL-STD-883, Method 2009
- 1.3 Freq. Vs. Temperature: Per Specification/Datasheet

2. Mechanical

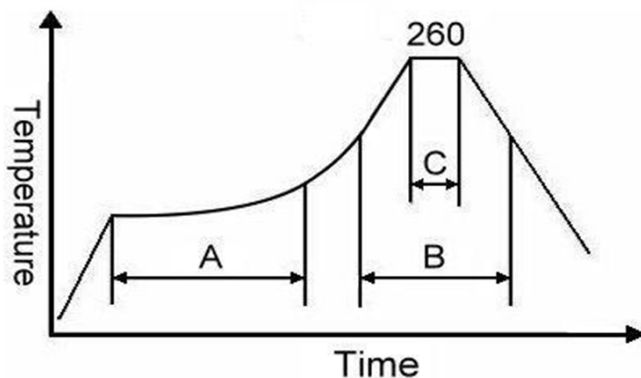
- 2.1 Mechanical Shock: MIL-STD-202 Method 213
- 2.2 Vibration: MIL-STD-202 Method 204
- 2.3 Solderability: J-STD-002
- 2.4 Board Flex: AEC Q200-005
- 2.5 Terminal Strength (SMD): AEC Q200-006

3.Environmental

- 3.1 Temp Cycle: JESD22, Method JA-104
- 3.2 Resistance to Solder Heat: MIL-STD-202 Method 210
- 3.3 High Temperature Operating Life: MIL-STD-202, Method 108
- 3.4 High Temp Exposure: MIL-STD-202, Method 108
- 3.5 High Temp & High Humidity: MIL-STD-202, Method 103
- 3.6 Thermal Shock: MIL-STD-202, Method 107

SUGGESTED IR REFLOW PROFILE

*As per IPC-JEDEC J-STD-020D



Note:

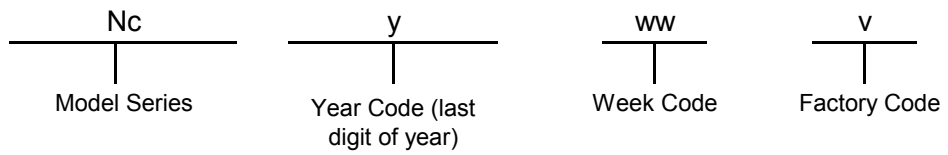
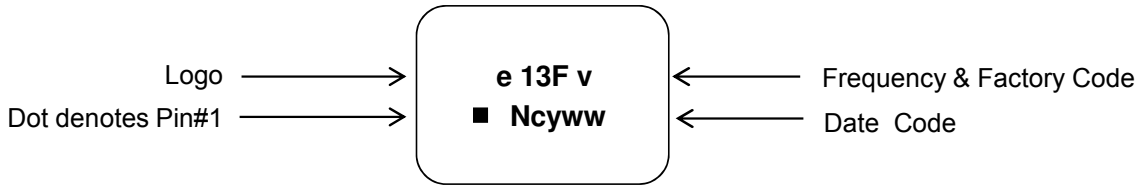
	Stage	Temperature	Time
A	Preheat	150~200°C	60~120 Sec
B	Primary Heat	217°C	60~150 Sec
C	Peak	260°C	10 Sec

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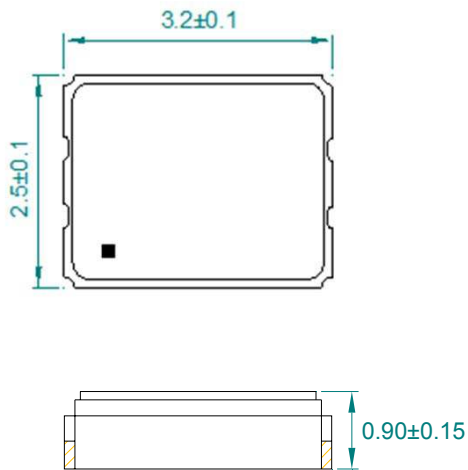
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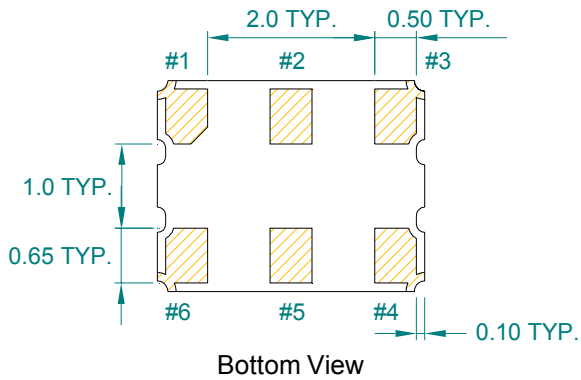
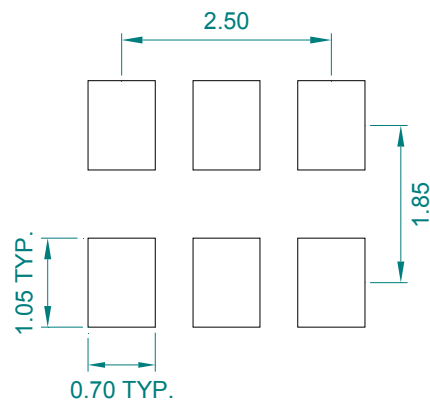
MARKING



MECHANICAL DRAWINGS (Scale:None. Dimensions are in mm.)



Recommended Land Pattern*



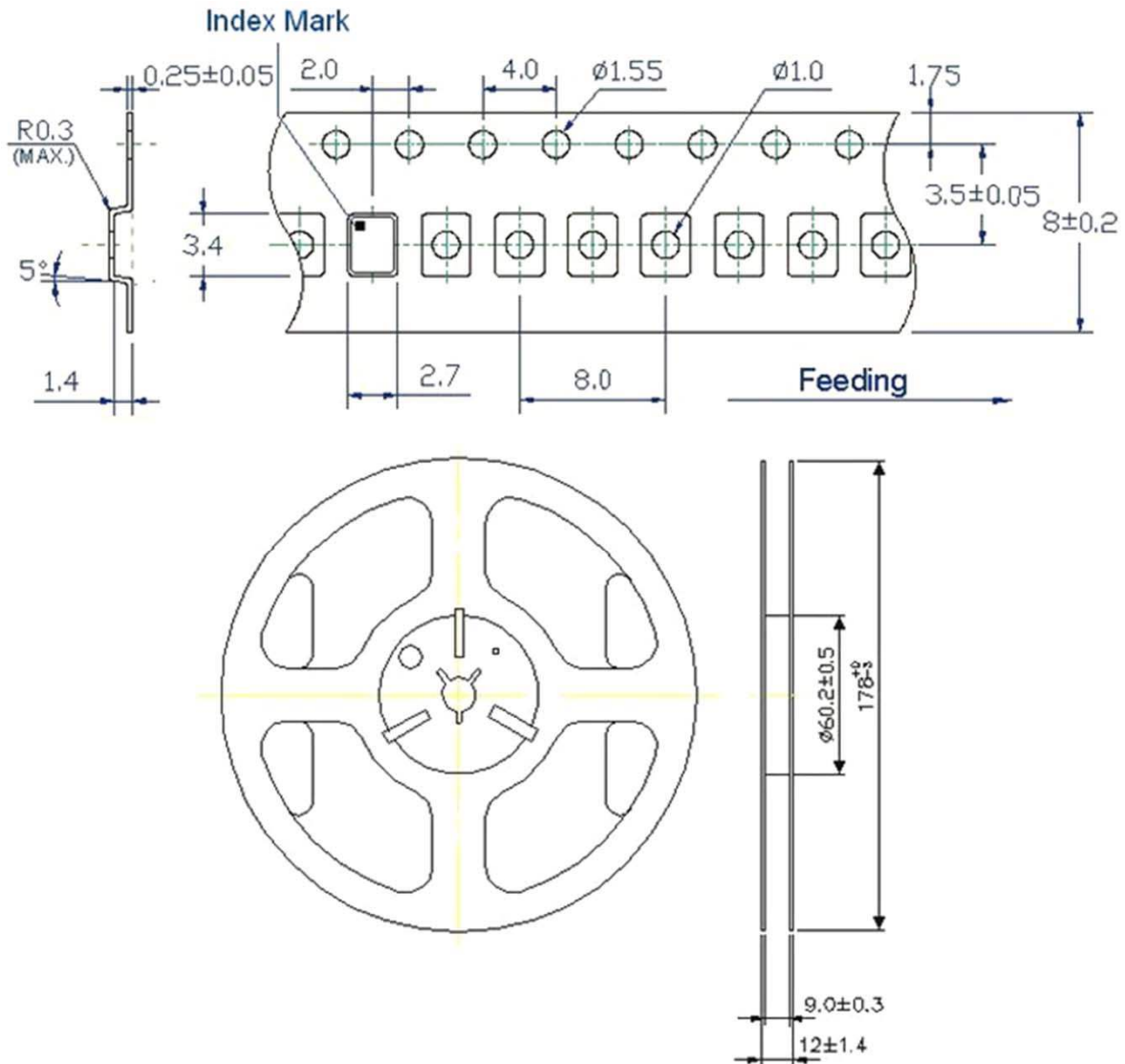
Pin	Function
1	OE
2	NC
3	Ground
4	Q
5	\overline{Q}
6	V _{CC}

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TAPE&REEL



1. 230mm minimum leader which consist of carrier and/or tape followed by a minimum of 160mm of empty carrier tape sealed with cover tape.
2. 160mm minimum trailer of empty carrier tape sealed with cover tape.

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PACKING

