VND5E008MY-E

Double channel high-side driver with analog current sense for automotive applications

Datasheet - production data

PowerSSO-36

Features

Max transient supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4.5 to 28 V
Typ on-state resistance (per ch.)	R_{ON}	8 mΩ
Current limitation (typ)	I_{LIMH}	76 A
Off-state supply current	I_S	2 µA(1)

1. Typical value with all loads connected

- General
  - Inrush current active management by power limitation
  - Very low standby current
  - 3.0V CMOS compatible inputs
  - Optimized electromagnetic emissions
  - Very low electromagnetic susceptibility
  - Compliant with European directive 2002/95/EC
  - Proportional load current sense
  - High current sense precision for wide current range
  - Very low current sense leakage
- Diagnostic functions
  - Current sense disable
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Thermal shutdown
  - Reverse battery protection with self switch on of the Power MOSFET
  - Electrostatic discharge protection

Applications

- All types of resistive, inductive and capacitive loads

Description

The VND5E008MY-E is a double channel high-side driver manufactured using STMicroelectronics® proprietary VIPower® M0-5 technology and housed in PowerSSO-36 package. The device is designed to drive 12 V automotive grounded loads, and to provide protection and diagnostics. It also implements a 3 V and 5 V CMOS compatible interface for the use with any microcontroller.

The device integrates advanced protective functions such as load current limitation, inrush and overload active management by power limitation, overtemperature shut-off with auto restart and overvoltage active clamp. A dedicated analog current sense pin is associated with every output channel providing enhanced diagnostic functions including fast detection of overload and short-circuit to ground through power limitation indication and overtemperature indication.

The current sensing and diagnostic feedback of the whole device can be disabled by pulling the CS_DIS pin high to share the external sense resistor with similar devices.

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1 Block diagram and pin description

Figure 1. Block diagram

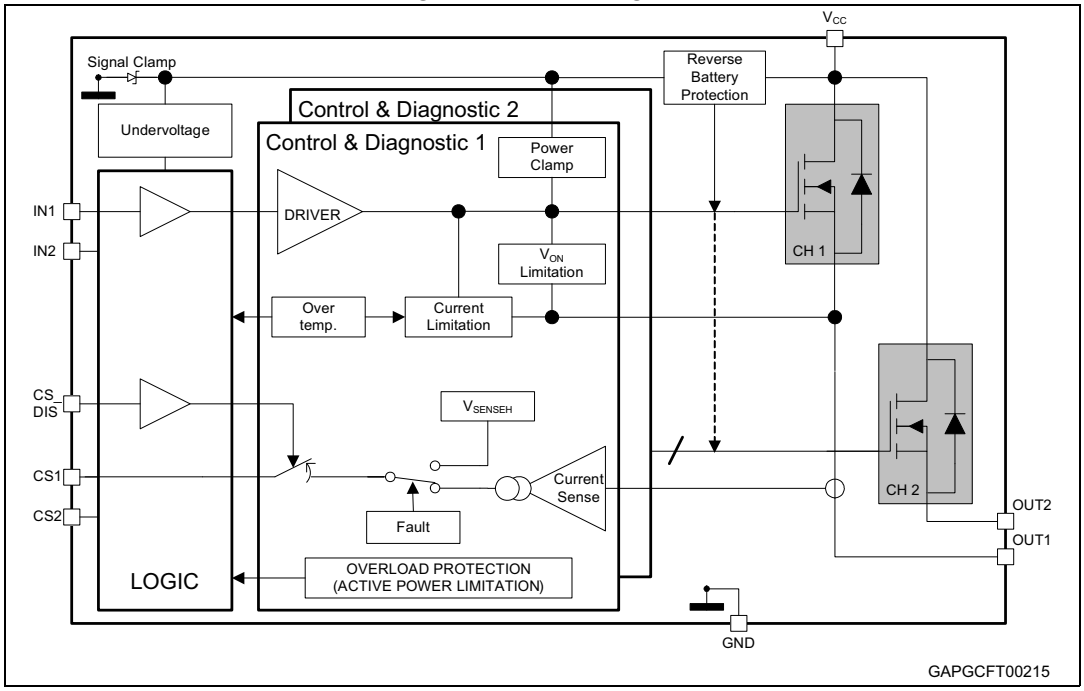


Table 1. Pin function

Name	Function
V_{CC}	Battery connection
$OUT_{1,2}$	Power output
GND	Ground connection
$IN_{1,2}$	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state
$CS_{1,2}$	Analog current sense pin, delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin

Figure 2. Configuration diagram (top view)

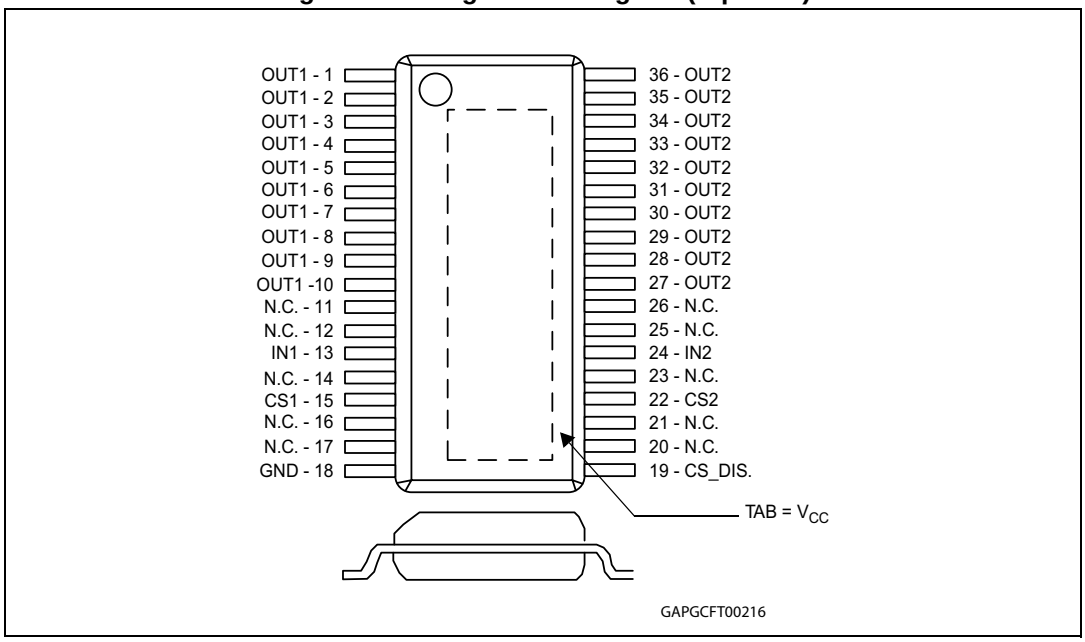
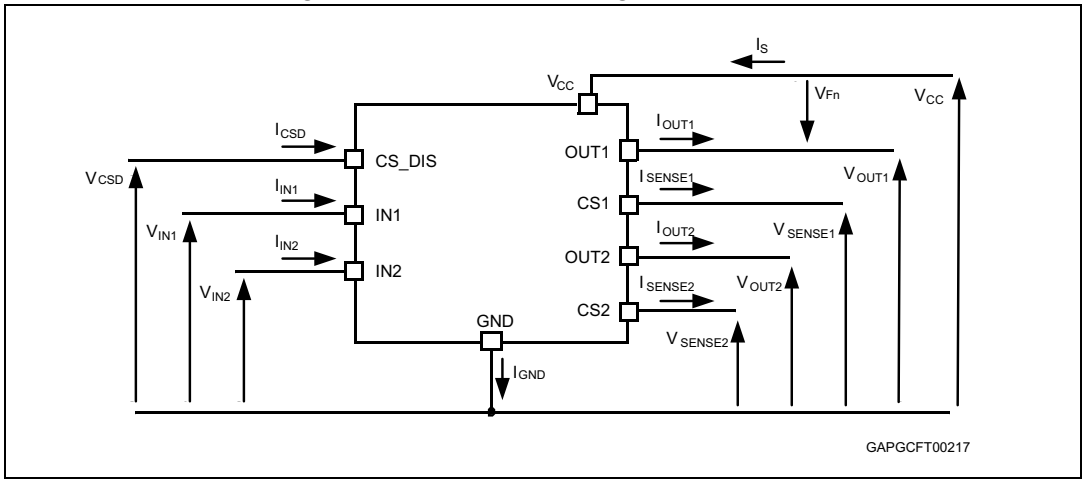


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current Sense	N.C.	Output	Input	CS_DIS
Floating	Not allowed	X	X	X	X
To ground	Through 1 KΩ resistor	X	Not allowed	Through 10 KΩ resistor	Through 10 KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	28	V
V_{CCPK}	Transient supply voltage (T<400ms, R_{LOAD} > 0.5Ω)	41	V
$-V_{CC}$	Reverse DC supply voltage	16	V
V_{CC_LSC}	Maximum supply voltage for full protection to short-circuit (acc. AEC-Q100-012)	18	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	50	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC} - 41 $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) (L = 0.85 mH; R_L = 0 Ω; V_{bat} = 13.5 V; T_{jstart} = 150 °C; I_{OUT} = I_{limL}(Typ.))	260	mJ

Table 3. Absolute maximum rating (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (Human Body Model: R = 1.5 KΩ; C = 100 pF) – V_{CC}, OUTPUT – INPUT, CS_DIS – CURRENT SENSE	 5000 4000 2000	 V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (MAX) (with one channel ON)	0.85	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (MAX)	See *Figure 33* in the Thermal section	°C/W

2.3 Electrical characteristics

8 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance	I_{OUT} = 6 A; T_j = 25 °C		8		mΩ
		I_{OUT} = 6 A; T_j = 150 °C			15	mΩ
		I_{OUT} = 6A; V_{CC} = 5V; T_j = 25 °C			11	mΩ
$R_{ON\ REV}$	Reverse battery on-state resistance	V_{CC} = -13 V; I_{OUT} = -6 A; T_j = 25 °C		8		mΩ
V_{clamp}	Clamp Voltage	I_S = 20 mA	41	46	52	V
I_S	Supply current	Off-state; V_{CC} = 13 V; T_j = 25 °C; V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0 V		2(1)	5(1)	µA
		On-state; V_{CC} = 13 V; V_{IN} = 5 V; I_{OUT} = 0 A		3.5	6.5	mA
$I_{L(off)}$	Off-state output current (2)	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25 °C	0	0.01	3	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125 °C			5	µA

1. PowerMOS leakage included.
2. For each channel.

Table 6. Switching (V_{CC} = 13V; T_j = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 2.2 Ω (see *Figure 7*)	—	30	—	µs
$t_{d(off)}$	Turn-off delay time	R_L = 2.2 Ω (see *Figure 7*)	—	15	—	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L = 2.2 Ω	—	See *Figure 20*	—	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L = 2.2 Ω	—	See *Figure 21*	—	V/µs
W_{ON}	Switching energy losses during t_{won}	R_L = 2.2 Ω (see *Figure 7*)	—	1.2	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 2.2 Ω (see *Figure 7*)	—	0.43	—	mJ

Table 7. Current sense (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.25 A; V_{SENSE} = 0.5 V; T_j = -40 °C...150 °C	3658	6000	8926	
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 6 A; V_{SENSE} = 0.5 V T_j = -40 °C...150 °C T_j = 25 °C...150 °C	3910 4336	6000 6000	8928 8044	
dK_1/K_1 (1)	Current sense ratio drift	I_{OUT} = 6 A; V_{SENSE} = 0.5 V V_{CSD} = 0 V; T_J= -40 °C to 150 °C	-12		12	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 10 A; V_{SENSE} = 4 V T_j = -40 °C...150 °C T_j = 25 °C...150 °C	4948 5298	6000 6000	7372 6762	
dK_2/K_2 (1)	Current sense ratio drift	I_{OUT} = 10 A; V_{SENSE} = 4 V; V_{CSD} = 0 V; T_j = -40 °C to 150 °C	-7		7	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 25 A; V_{SENSE} = 4 V T_j = -40 °C...150 °C T_j = 25 °C...150 °C	5455 5535	6000 6000	6762 6282	
dK_3/K_3 (1)	Current sense ratio drift	I_{OUT} = 25 A; V_{SENSE} = 4 V; V_{CSD}= 0V; T_j = -40 °C to 150 °C	-5		5	%
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{CSD} = 5 V; V_{IN} = 0 V; T_j = -40 °C...150 °C	0		1	µA
		V_{CSD} = 0V; V_{IN} = 5V; T_j = -40 °C...150 °C	0		2	µA
		I_{OUT} = 6 A; V_{SENSE} = 0 V; V_{CSD} = V_{IN} = 5 V	0		1	µA
V_{SENSE}	Max analog sense output voltage	I_{OUT} = 15 A; V_{CSD} = 0 V	5			V
V_{SENSEH}	Analog sense output voltage in overtemperature condition (2)	V_{CC} = 13 V; R_{SENSE} = 10 KΩ		8		V
I_{SENSEH}	Analog sense output current in overtemperature condition (2)	V_{CC} = 13 V; V_{SENSE} = 5 V		9		mA
$t_{DSENSE1H}$	Delay Response time from falling edge of CS_DIS pin	V_{SENSE} < 4V, 1.5A < I_{OUT} < 25A I_{SENSE} = 90% of $I_{SENSE\ max}$ (see *Figure 4*)		50	100	µs
$t_{DSENSE1L}$	Delay Response time from rising edge of CS_DIS pin	V_{SENSE} < 4V, 1.5A < I_{OUT} < 25A I_{SENSE} = 10% of $I_{SENSE\ max}$ (see *Figure 4*)		5	20	µs

Table 7. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{DSENSE2H}$	Delay Response time from rising edge of INPUT pin	V_{SENSE} < 4V, 1.5A < I_{OUT} < 25A I_{SENSE} = 90% of $I_{SENSE\ max}$ (see *Figure 4*)		70	300	µs
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4 V, I_{SENSE} = 90 % of $I_{SENSEMAX}$, I_{OUT} = 90 % of I_{OUTMAX} I_{OUTMAX} = 5 A (see *Figure 10*)			300	µs
$t_{DSENSE2L}$	Delay Response time from falling edge of INPUT pin	V_{SENSE} < 4V, 1.5A < I_{OUT} < 25A I_{SENSE} = 10% of $I_{SENSE\ max}$ (see *Figure 4*)		100	250	µs

1. Parameter guaranteed by design; it is not tested.
2. Fault condition includes: power limitation and overtemperature.

Table 8. Protections and diagnostics(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC Short circuit current	V_{CC} = 13 V	53	76	106	A
		5 V < V_{CC} < 18 V			106	A
I_{limL}	Short circuit current during thermal cycling	V_{CC} = 13V; T_R < T_j < T_{TSD}		21		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of STATUS		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD}-T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; V_{IN} = 0; L = 6 mH	V_{CC}-29	V_{CC}-32	V_{CC}-36	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.4 A; T_j = -40 °C...150 °C (see *Figure 9*)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

Table 9. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V

Table 9. Logic inputs (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	V_{CSD} = 0.9 V	1			µA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	V_{CSD} = 2.1 V			10	µA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	I_{CSD} = 1 mA	5.5		7	V
		I_{CSD} = -1 mA		-0.7		V

Figure 4. Current sense delay characteristics

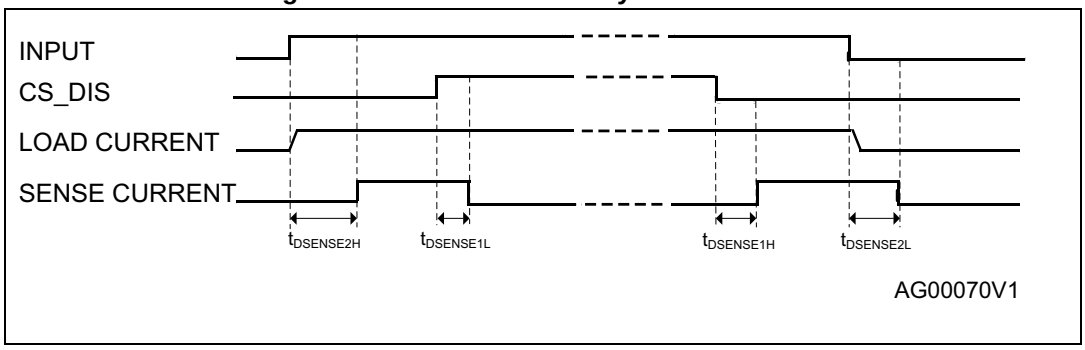


Figure 5. I_{OUT}/I_{SENSE} vs I_{OUT}

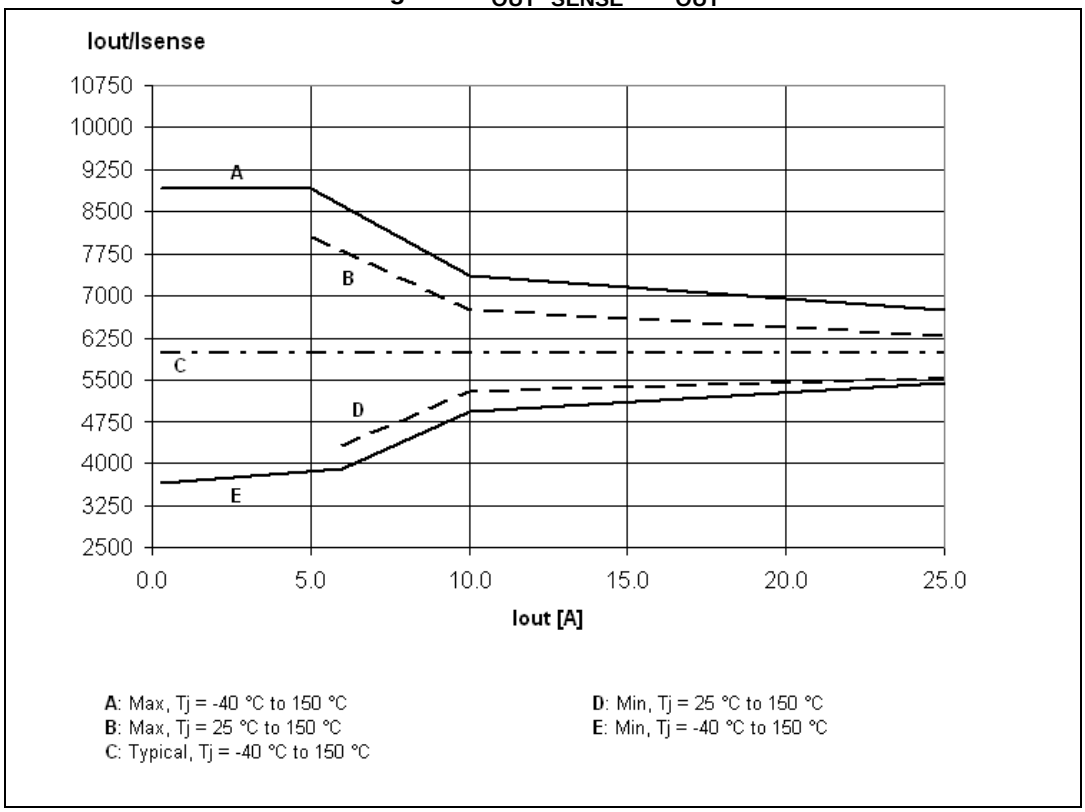
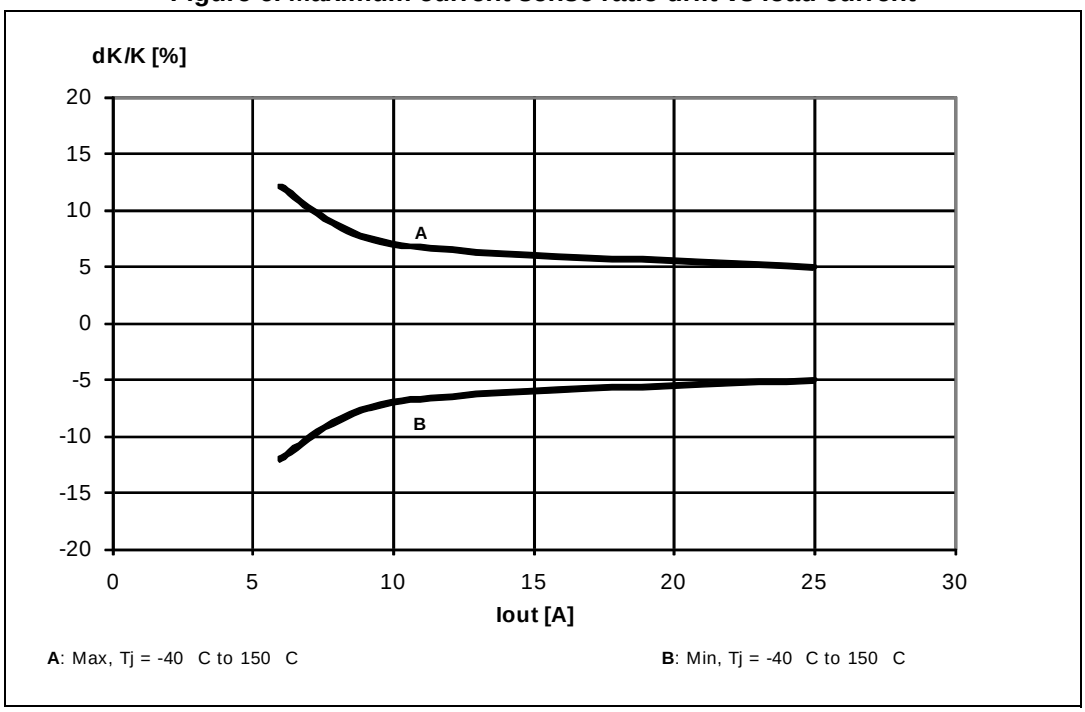


Figure 6. Maximum current sense ratio drift vs load current



Note: Parameter guaranteed by design; it is not tested.

Table 10. Truth table

Conditions	Input	Output	Sense (V_{csd} = 0V)(1)
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overload	H H	X (no power limitation) Cycling (power limitation)	Nominal V_{SENSEH}
Short circuit to GND (Power limitation)	L H	L L	0 V_{SENSEH}
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Figure 7. Switching characteristics

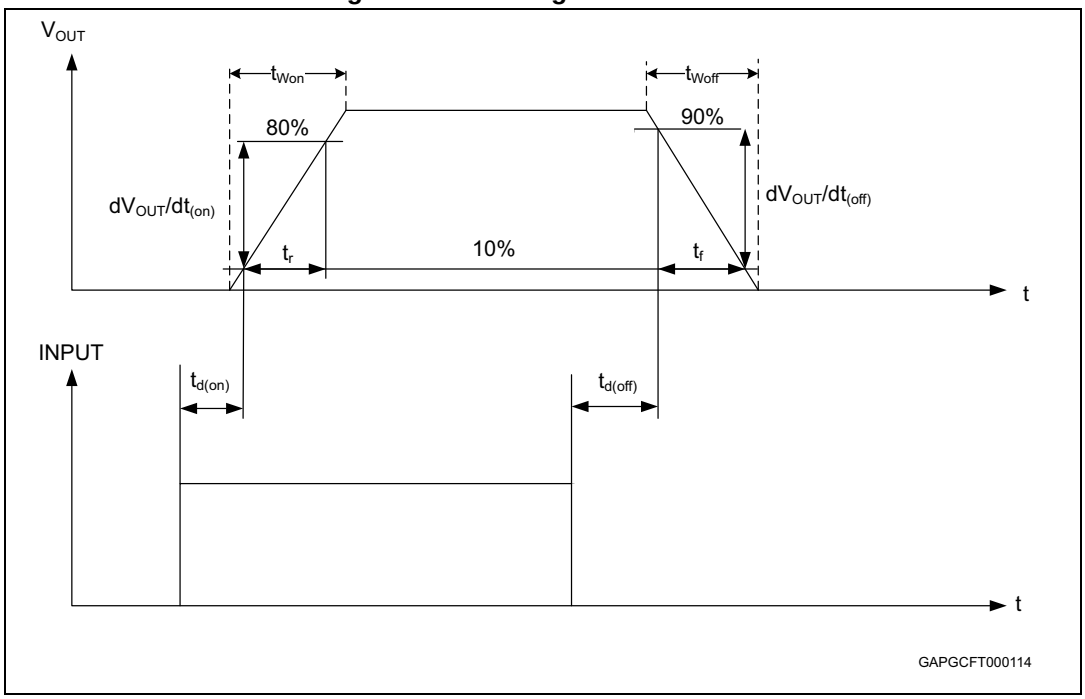


Figure 8. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

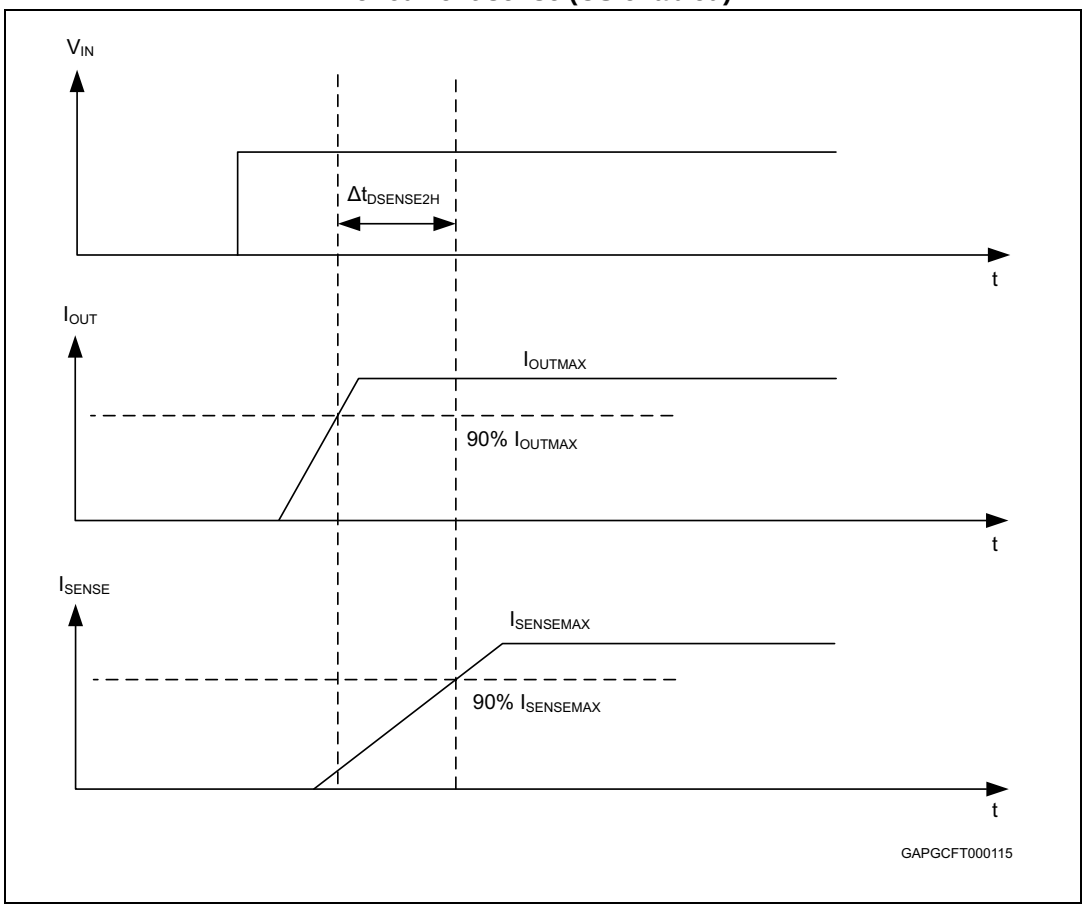


Figure 9. Output voltage drop limitation

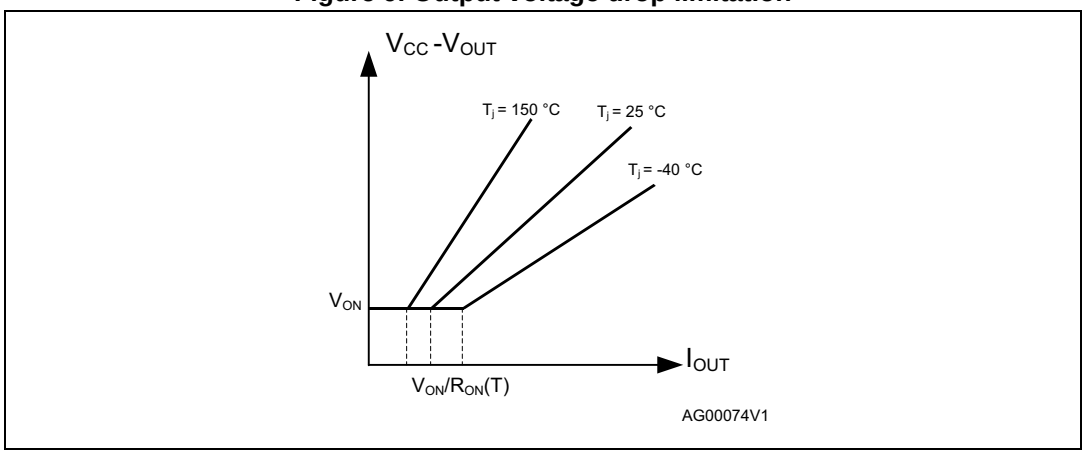


Table 11. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b(2)	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.

Table 12. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results(1)	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(2)(3)	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.
3. Suppressed load dump (pulse 5b) is withstood with a minimum load connected as specified in *Table 3: Absolute maximum rating*.

Table 13. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 10. Normal operation

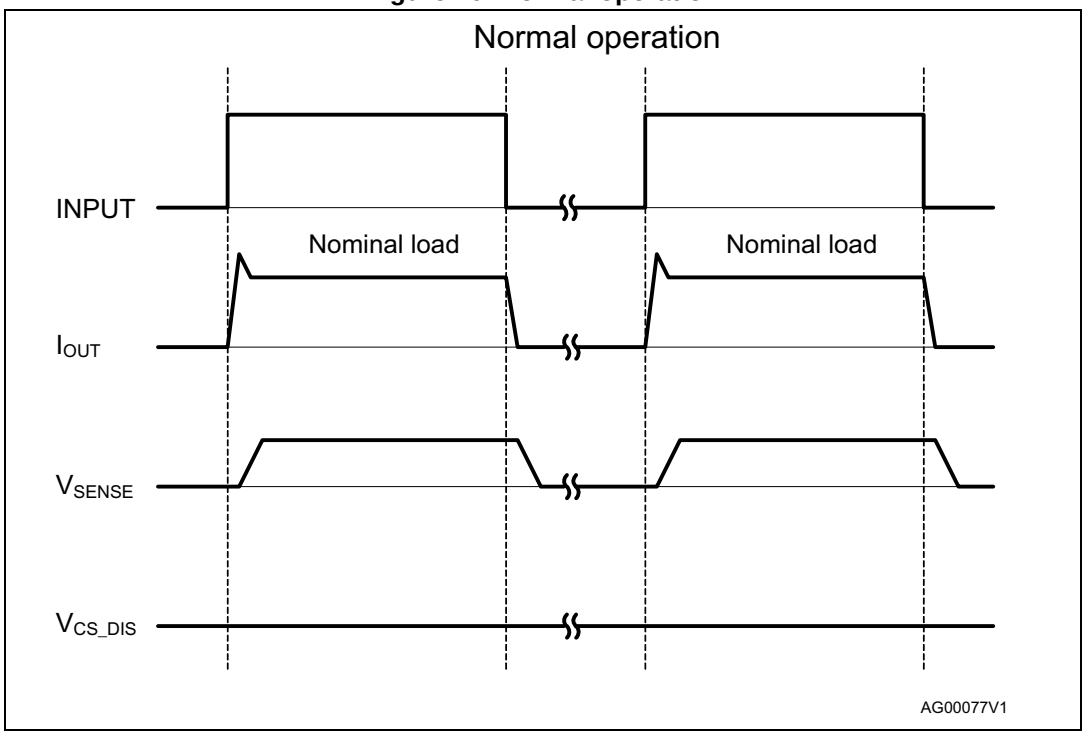


Figure 11. Overload or short to GND

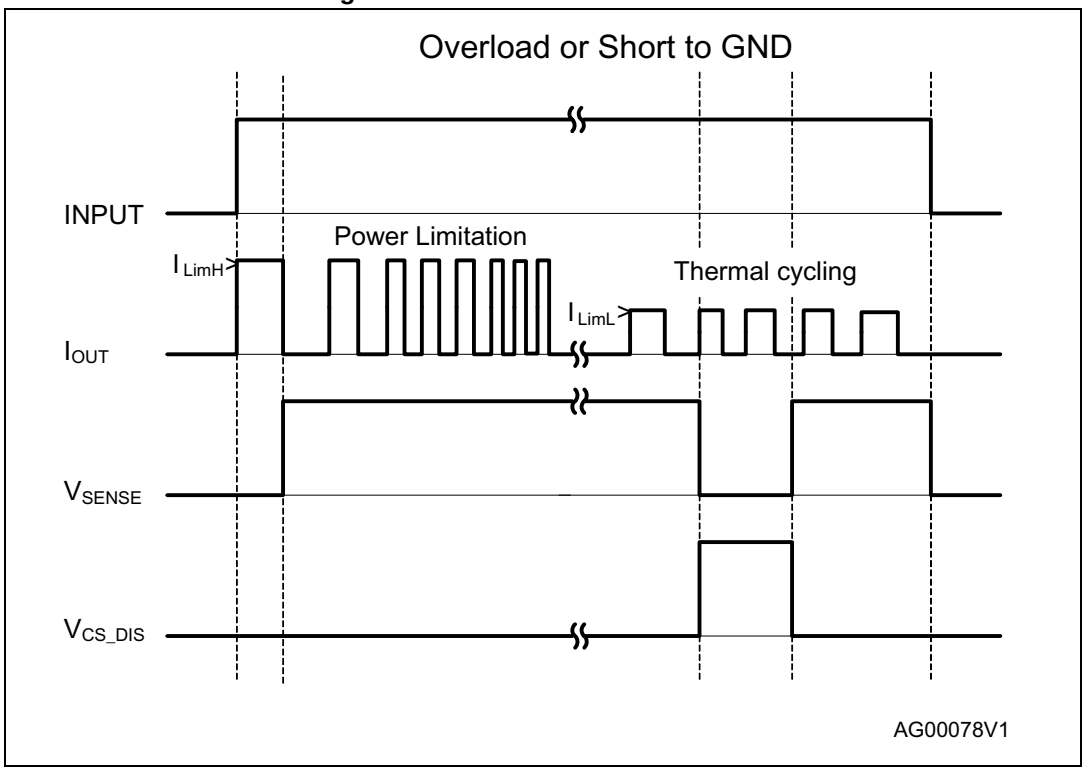


Figure 12. Intermittent overload

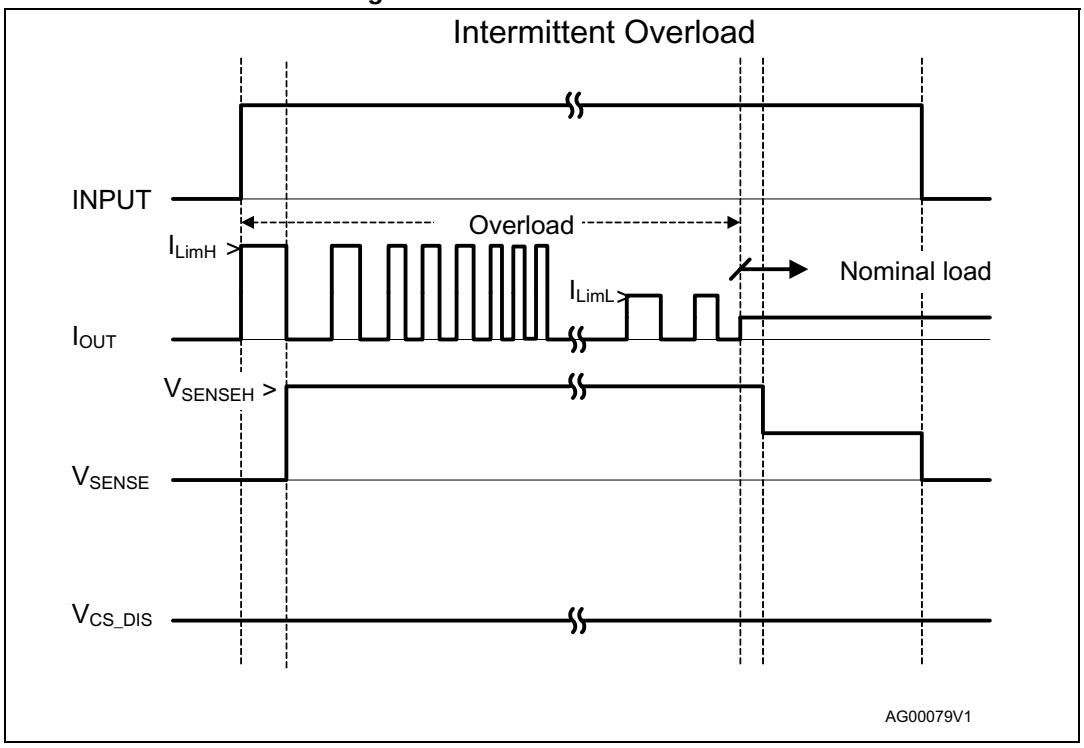
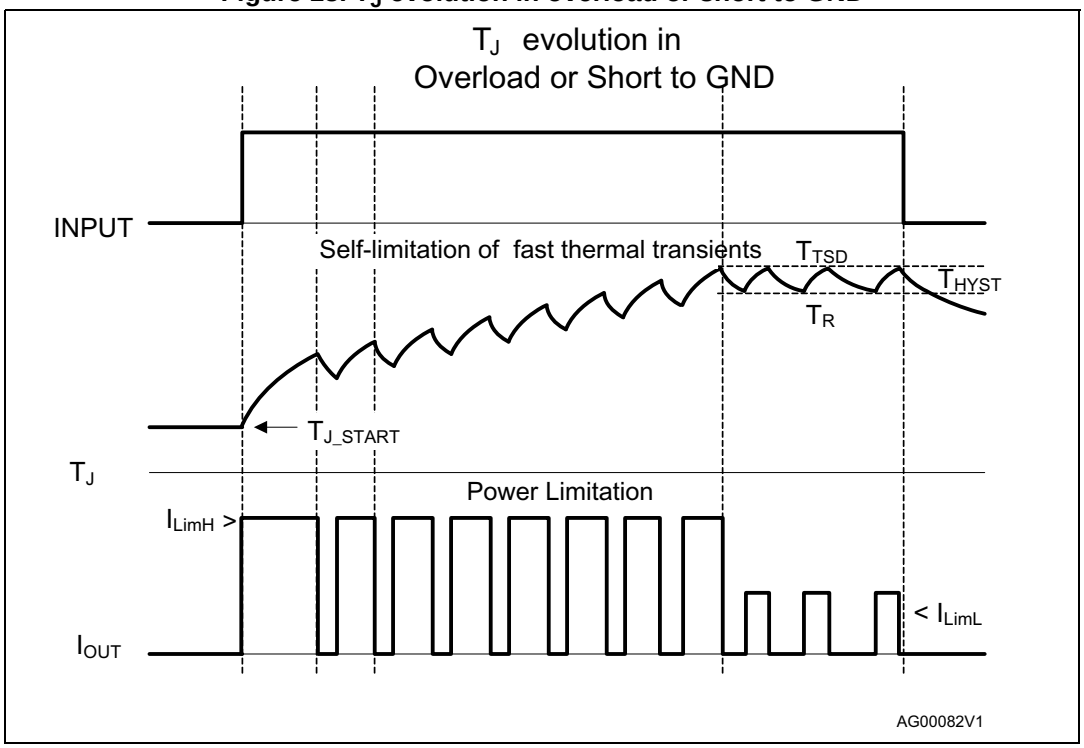


Figure 13. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 14. Off-state output current

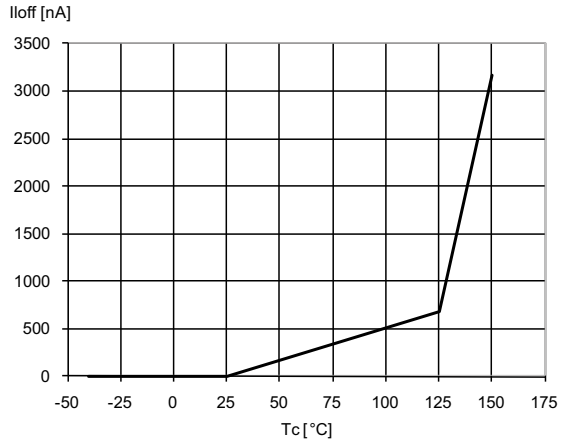


Figure 15. High level input current

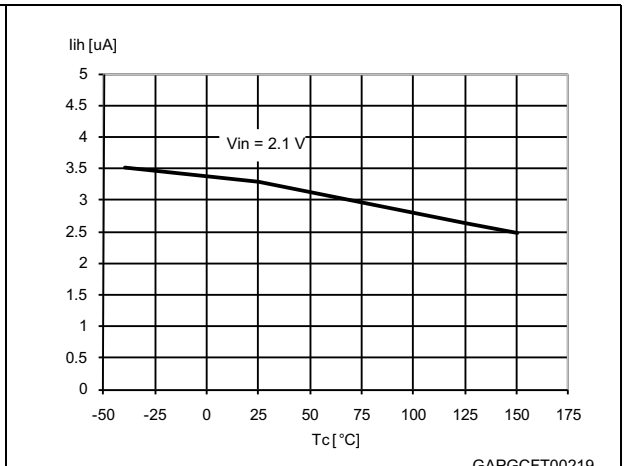


Figure 16. Input clamp voltage

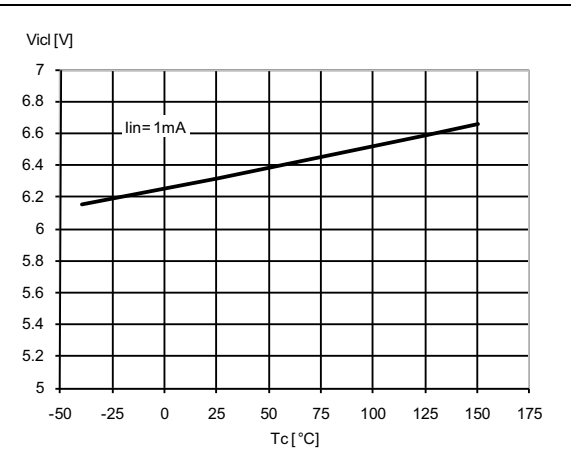


Figure 17. Input high level voltage

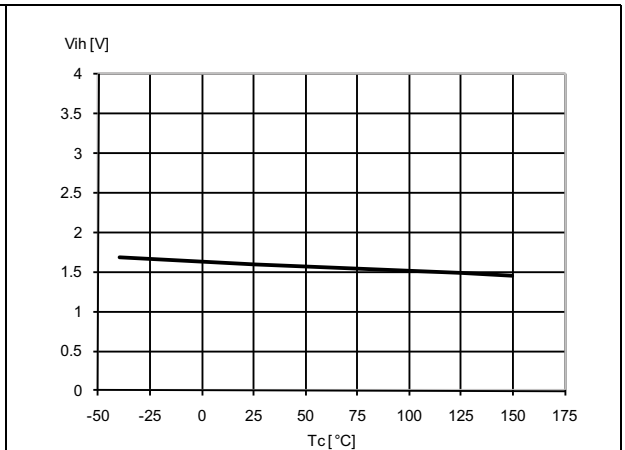


Figure 18. Input low level voltage

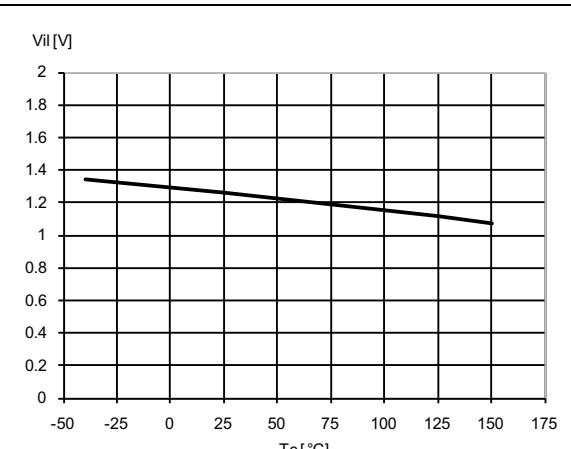


Figure 19. Input hysteresis voltage

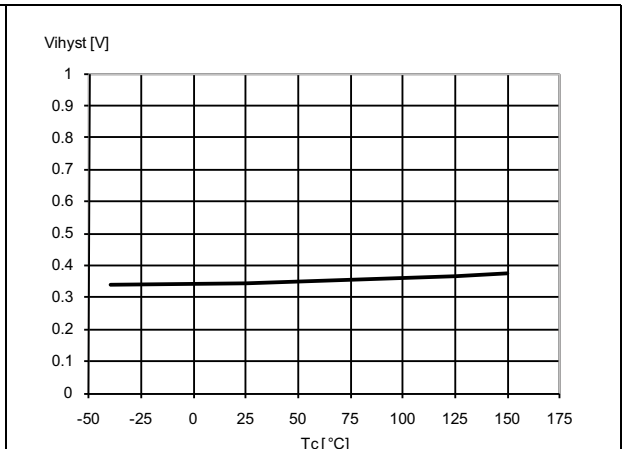


Figure 20. On-state resistance vs T_{case}

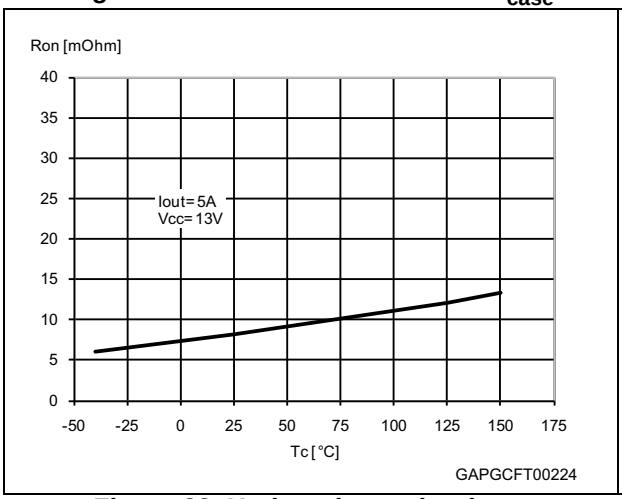


Figure 21. On-state resistance vs V_{CC}

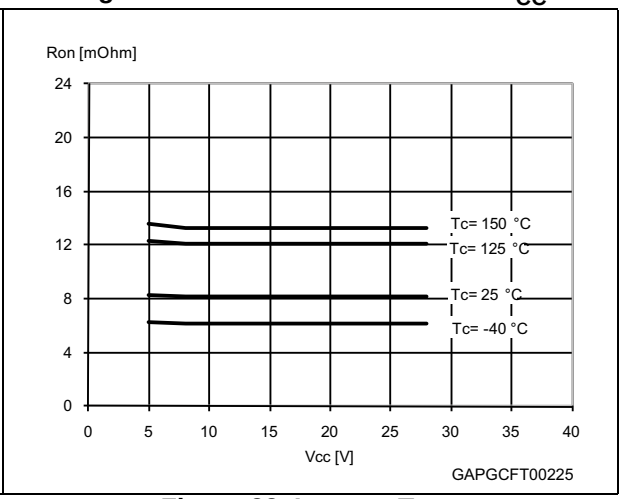


Figure 22. Undervoltage shutdown

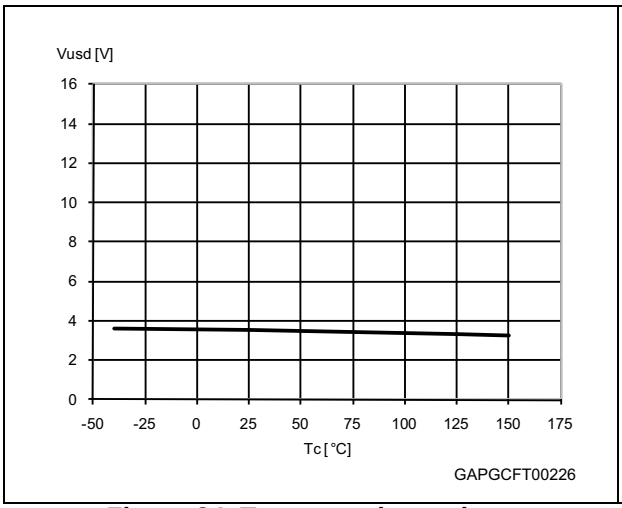


Figure 23. I_{LIMH} vs T_{case}

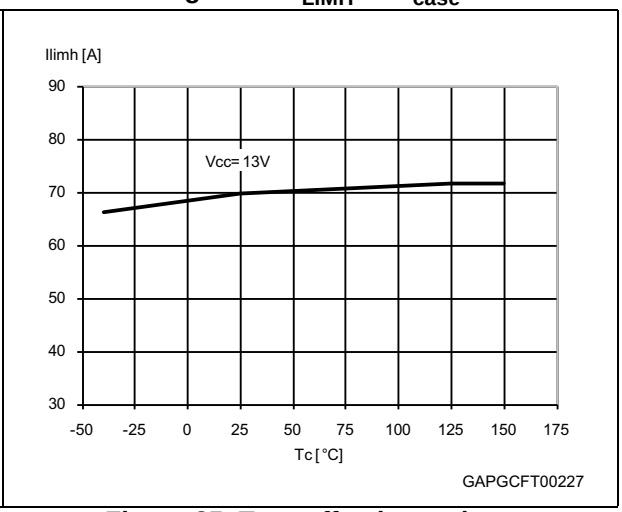


Figure 24. Turn-on voltage slope

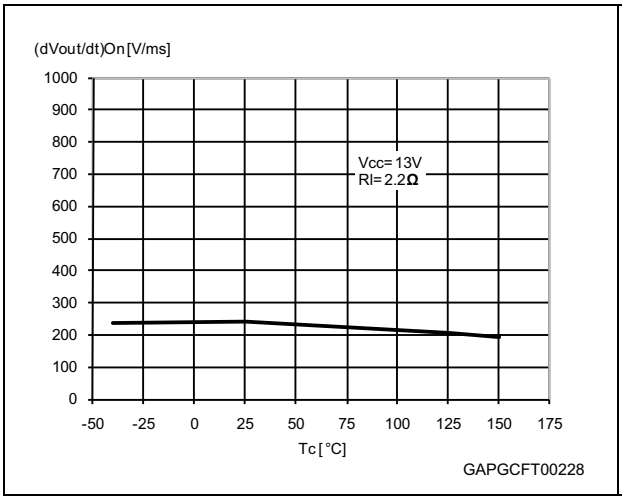


Figure 25. Turn-off voltage slope

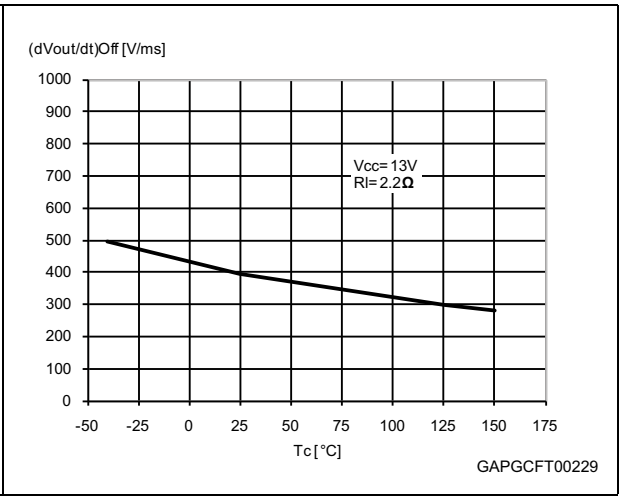


Figure 26. CS_DIS clamp voltage

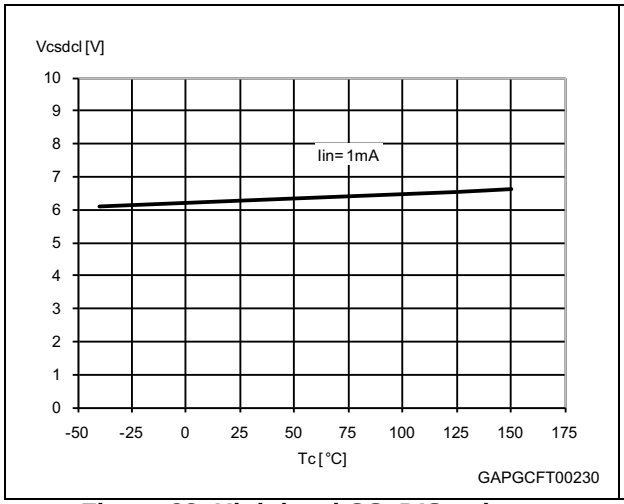


Figure 27. Low level CS_DIS voltage

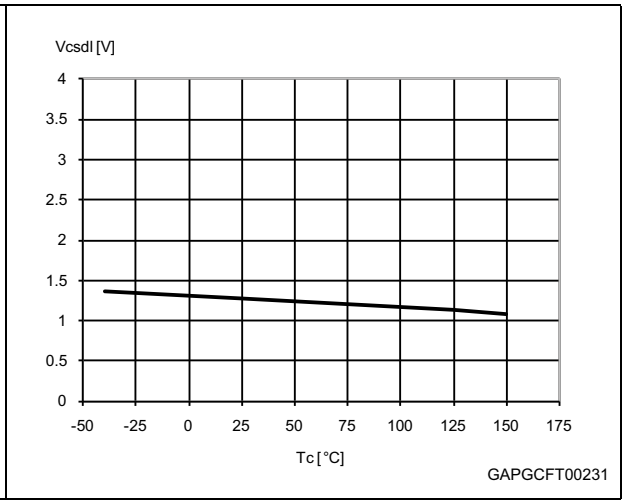
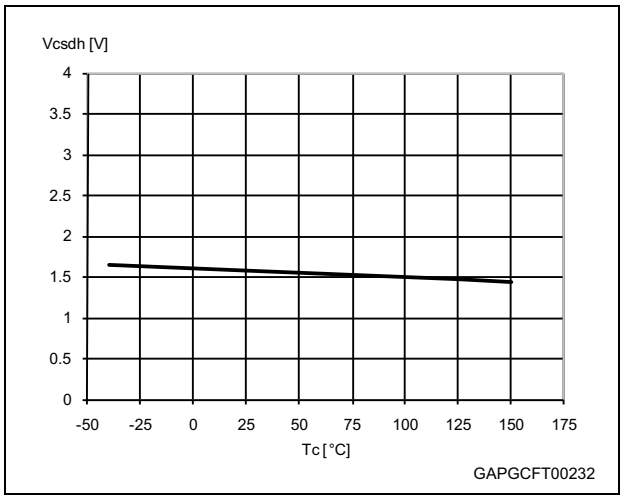
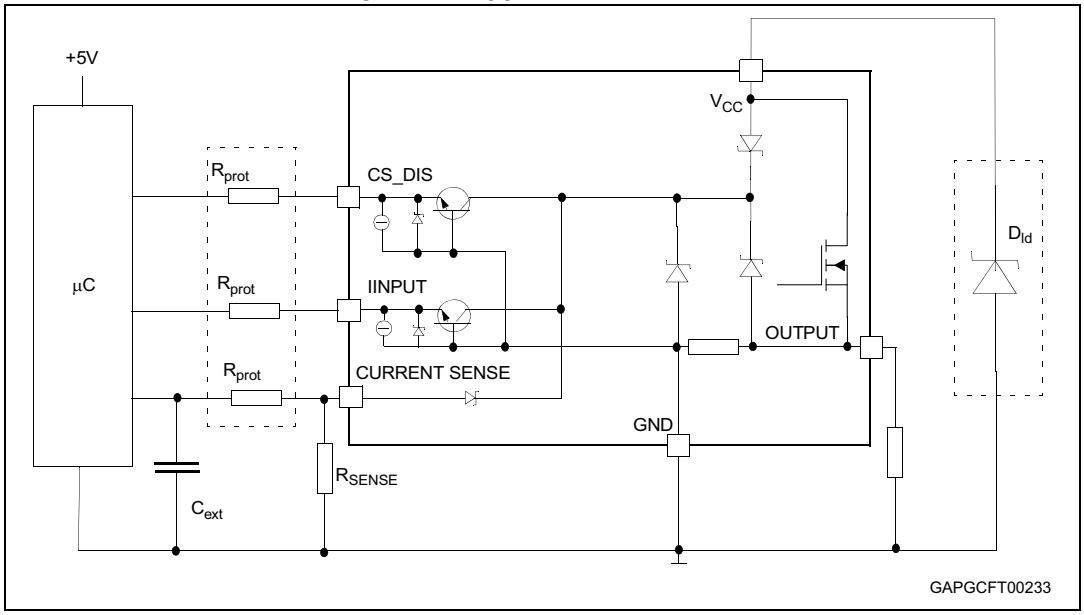


Figure 28. High level CS_DIS voltage



3 Application information

Figure 29. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

3.1 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CCPK} max rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.2 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pin is pulled negative to approximately -1.5 V. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 1

$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH}) / I_{IHmax}$

Calculation example:

For V_{CCpeak} = - 1.5 V; $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

$75\ \Omega \leq R_{prot} \leq 240\ k\Omega$.

Recommended values: R_{prot} =10 kΩ, C_{EXT} =10 nF.

3.3 Current sense and diagnostic

The current sense pin performs a double function (see *Figure 30: Current sense and diagnostic*):

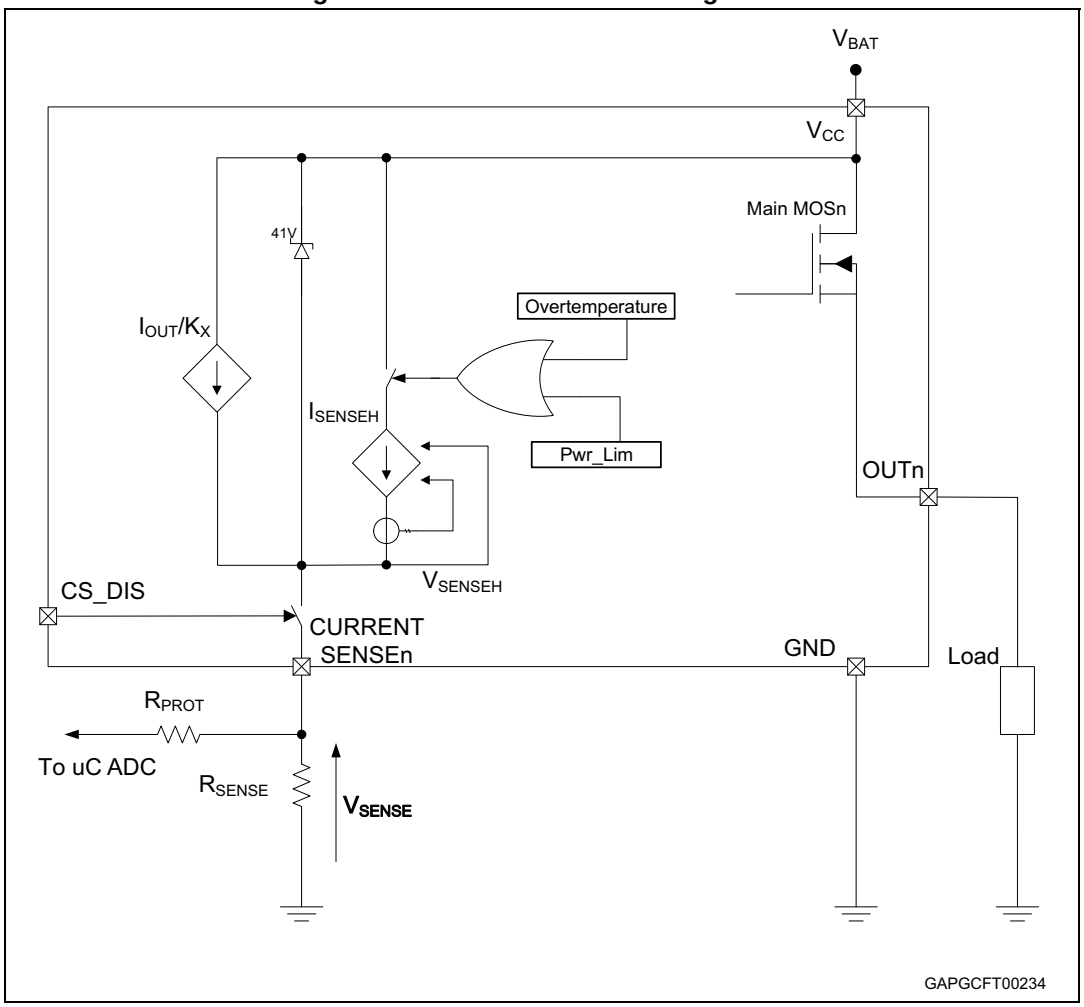
- **Current mirror of the load current in normal operation,** delivering a current proportional to the load one according to a known ratio $\mathbf{K_X}$.
  The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE}. Linearity between I_{OUT} and V_{SENSE} is ensured up to 5V minimum (see parameter V_{SENSE} in *Table 7: Current sense (8 V < VCC < 18 V)*). The current sense accuracy depends on the output current (refer to current sense electrical characteristics *Table 7: Current sense (8 V < VCC < 18 V)*).

- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to *Table 10: Truth table*):

  – Power limitation activation
  – Overtemperature

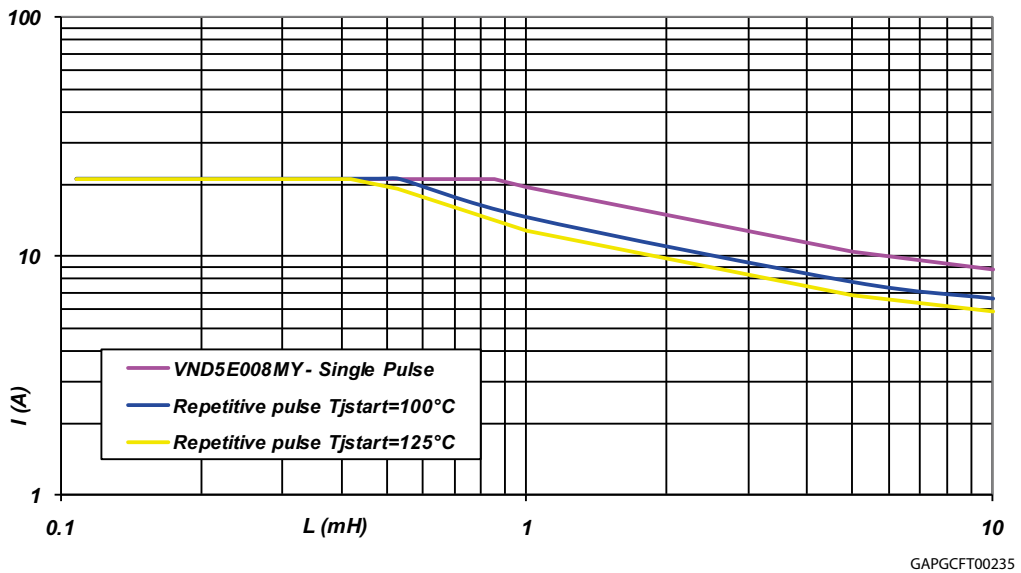
A logic level high on CS_DIS pin sets at the same time all the current sense pins of the device in a high impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

Figure 30. Current sense and diagnostic



3.4 Maximum demagnetization energy (V_{CC} = 13.5V)

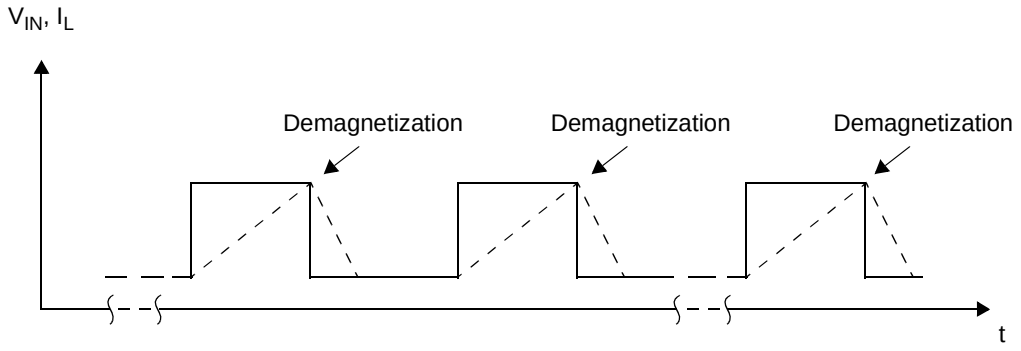
Figure 31. Maximum turn-off current versus inductance



A: T_{jstart} = 150°C single pulse

B: T_{jstart} = 100°C repetitive pulse

C: T_{jstart} = 125°C repetitive pulse

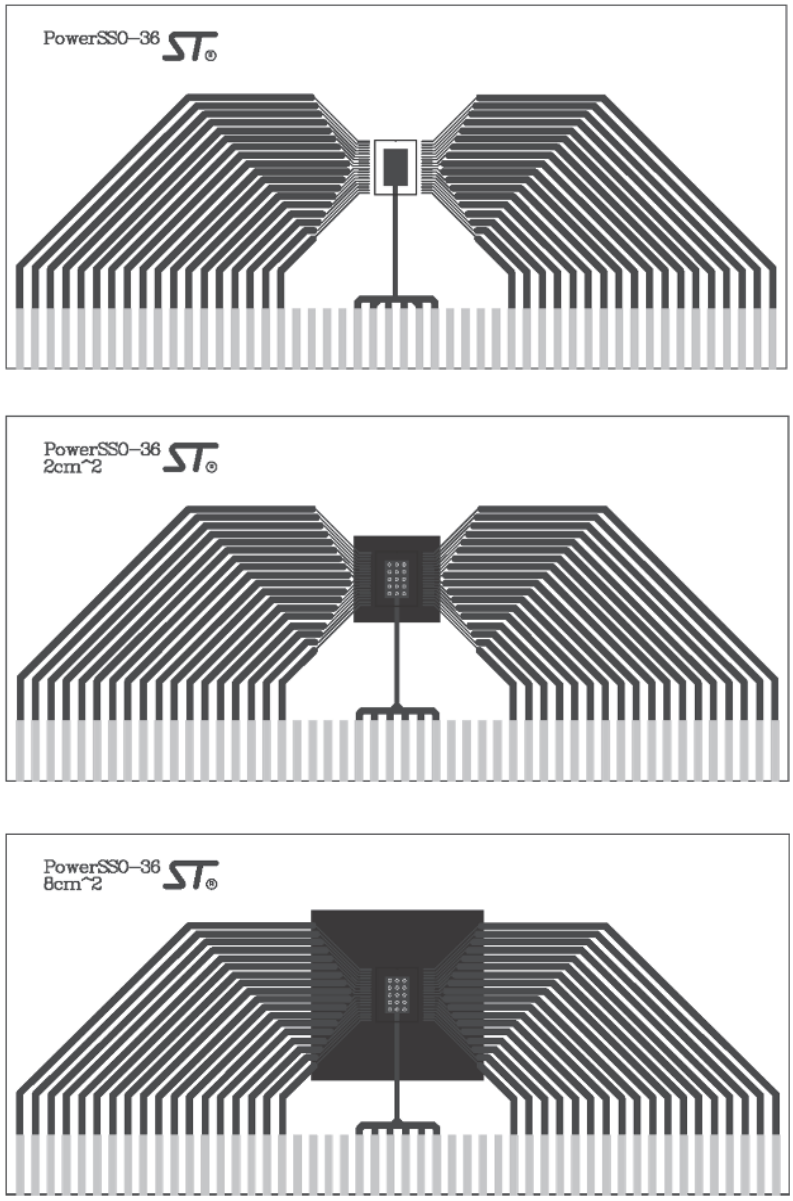


Note: Values are generated with R_L = 0 Ω.
In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-36 thermal data

Figure 32. PowerSSO-36 PC board



Note:
Layout condition of R_{th} and Z_{th} measurements (Board finish thickness 1.6 mm +/-10 %; Board double layer; Board dimension 129 mm x 60 mm; Board Material FR4; Cu thickness 0.070 mm; Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm +/-0.08 mm; Cu thickness on vias 0.025 mm; Footprint dimension 4.1 mm x 6.5 mm)

Figure 33. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

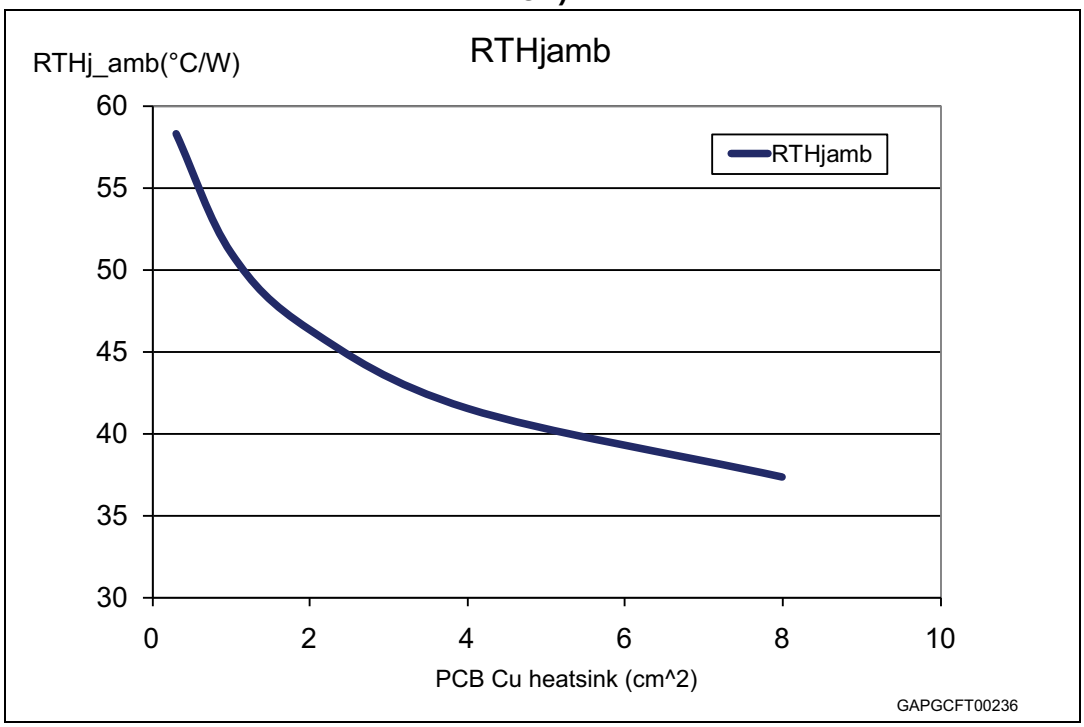


Figure 34. PowerSSO-36 thermal impedance junction ambient single pulse (one channel ON)

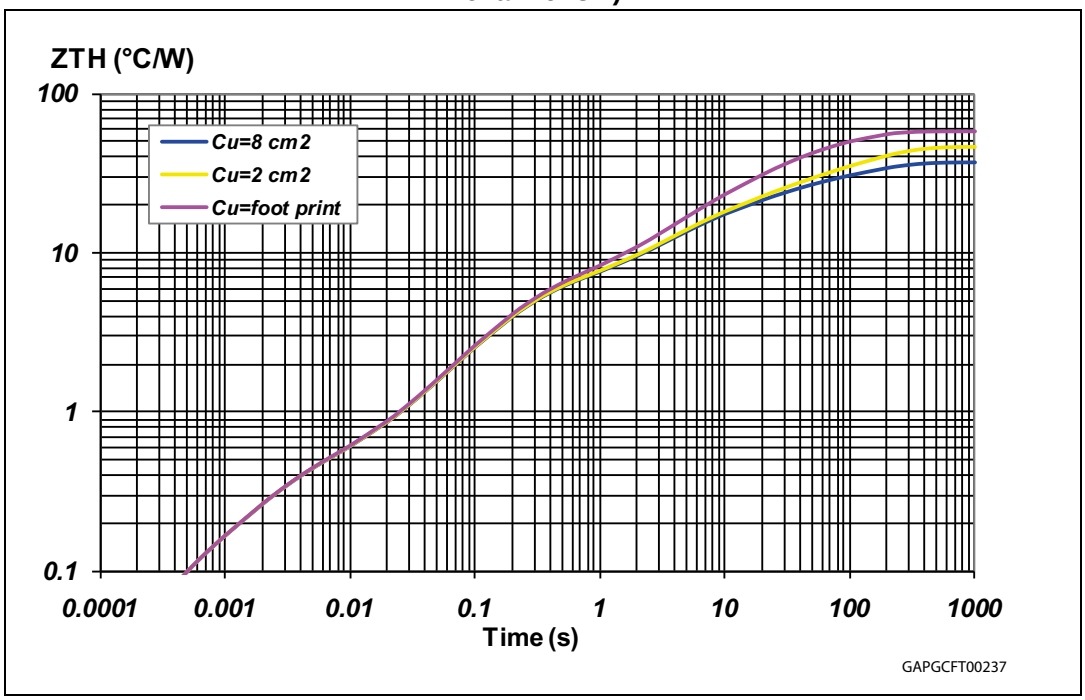
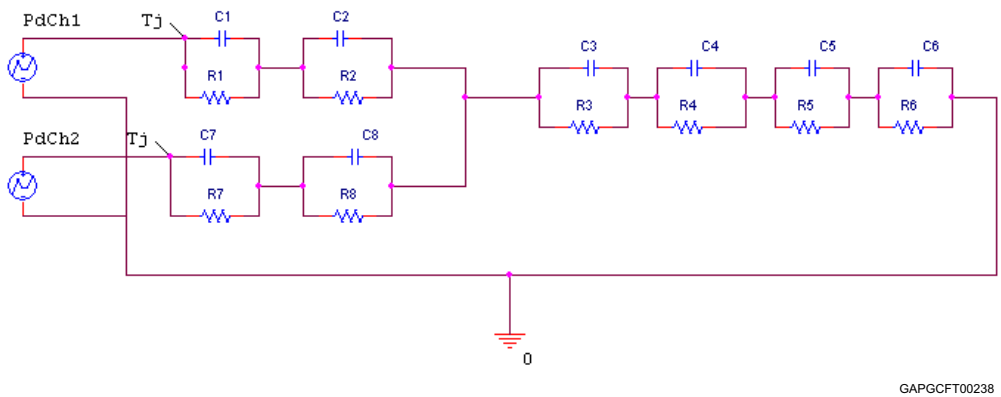


Figure 35. Thermal fitting model of a double channel HSD in PowerSSO-36



Note:
The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where $\delta = t_p / T$

Table 14. Thermal parameter

Area/island (cm^2)	Footprint	2	8
R1 = R7 (°C/W)	0.05		
R2 = R8 (°C/W)	0.3		
R3 (°C/W)	5		
R4 (°C/W)	8		
R5 (°C/W)	18	10	10
R6 (°C/W)	27	23	14
C1 = C7 (W.s/°C)	0.004		
C2 = C8 (W.s/°C)	0.008		
C3 (W.s/°C)	0.04		
C4 (W.s/°C)	0.5		
C5 (W.s/°C)	1	2	2
C6 (W.s/°C)	3	6	9

5 Package information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

5.2 PowerSSO-36 mechanical data

Figure 36. PowerSSO-36 package dimensions

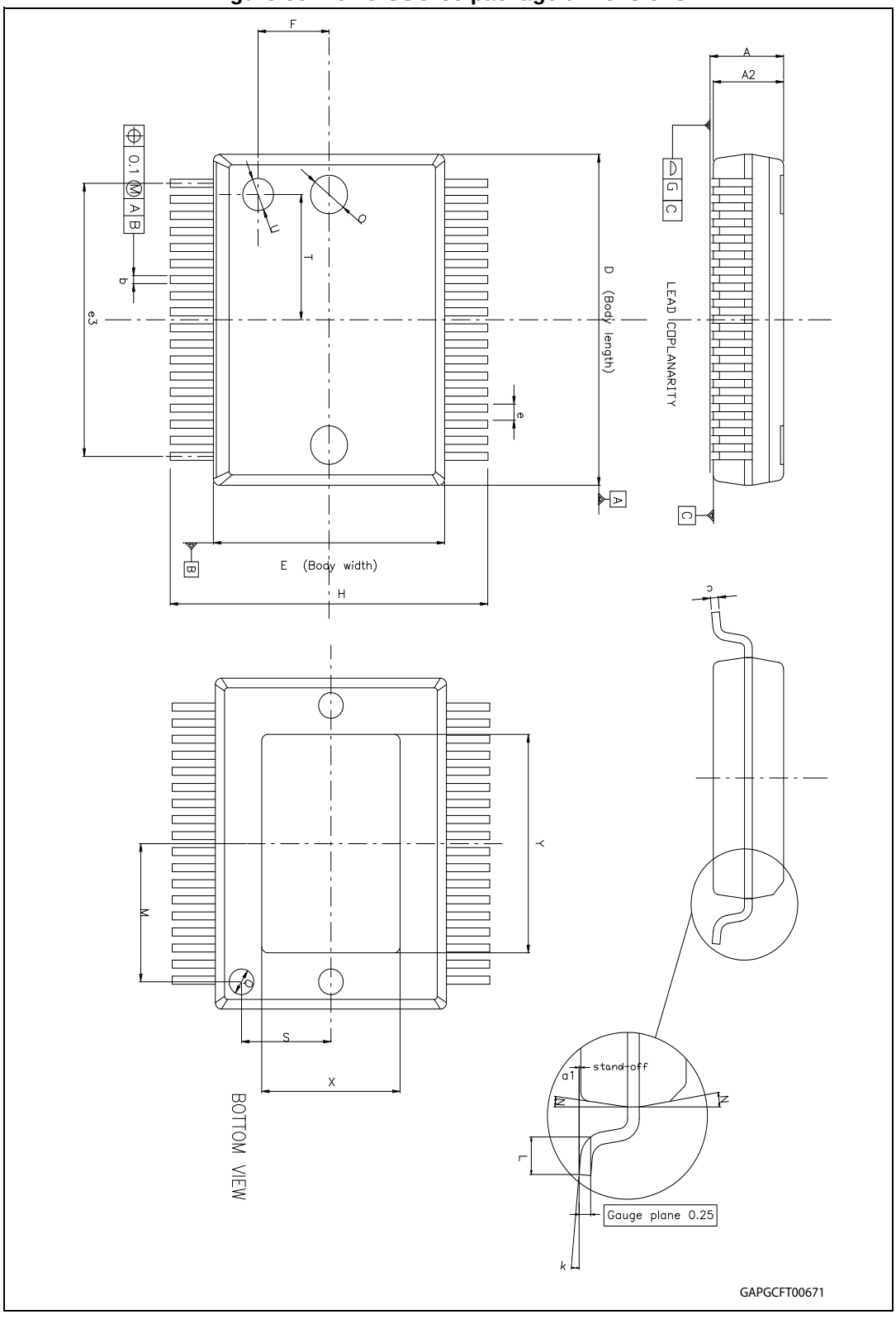
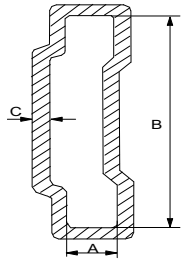


Table 15. PowerSSO-36 mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	2.15	—	2.47
A2	2.15	—	2.40
a1	0	—	0.075
b	0.18	—	0.36
c	0.23	—	0.32
D	10.10	—	10.50
E	7.4	—	7.6
e	—	0.5	—
e3	—	8.5	—
G	—	—	0.1
G1	—	—	0.06
H	10.1	—	10.5
h	—	—	0.4
L	0.55	—	0.85
N	—	—	10 deg
X	4.1	—	4.7
Y	6.5	—	7.1

5.3 Packing information

Figure 37. PowerSSO-36 tube shipment (no suffix)

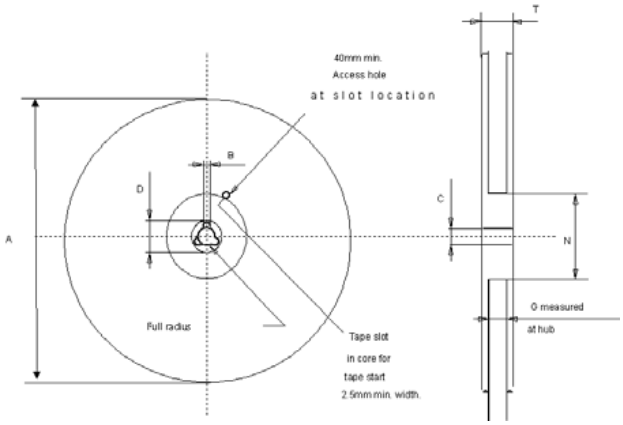


GAPGCFT00002

Base Q.ty	49
Bulk Q.ty	1225
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 38. PowerSSO-36 tape and reel shipment (suffix "TR")



REEL DIMENSIONS

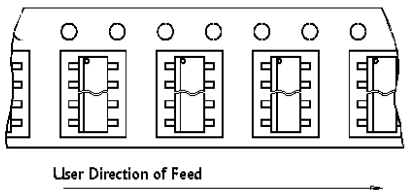
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	100
T (max)	30.4

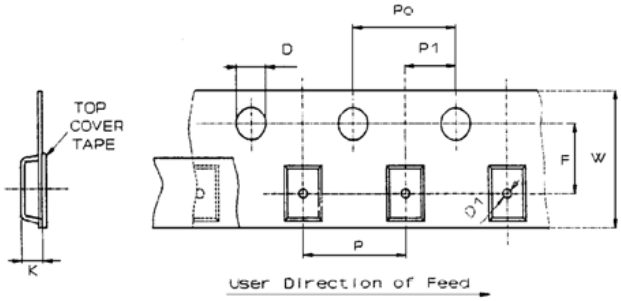
TAPE DIMENSIONS

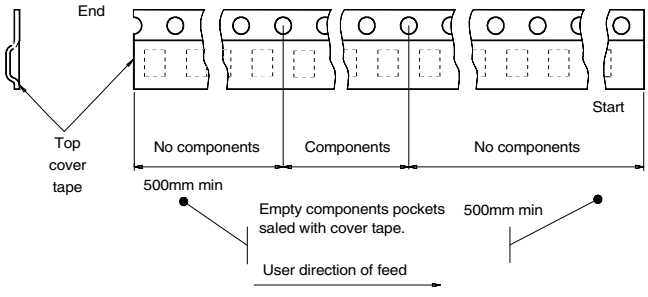
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







GAPGCFT00003

6 Order codes

Table 16. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36	VND5E008MY-E	VND5E008MYTR-E

7 Revision history

Table 17. Document revision history

Date	Revision	Changes
20-Apr-2011	1	Initial release.
27-Apr-2011	2	Updated *Table 8: Protections and diagnostics*: – I_{limH}: updated test condition
13-July-2012	3	Updated *Figure 36: PowerSSO-36 package dimensions*
18-Sep-2013	4	Updated Disclaimer.
25-Oct-2013	5	Updated footnote 2 into the *Table 11: Electrical transient requirements (part 1)* and *Table 12: Electrical transient requirements (part 2)*.

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