AN-1947 LM25069 Evaluation Board

1 Introduction

The LM25069EVAL evaluation board provides the design engineer with a fully functional hot swap controller board designed for positive voltage systems. This board contains an LM25069-2, the auto restart version of this IC. This application note describes the various functions of the board, how to test and evaluate it, and how to change the components for a specific application. For more information please review the *LM25069 Positive Low Voltage Power Limiting Hot Swap Controller* (SNVS607) data sheet.

The board's specifications are:

- Input voltage range: +2.9V to 17V
- Current limit: 5 Amps, ±10%
- Q1 Power limit: 15W
- UVLO Thresholds: 4.8V and 4.5V
- OVLO Thresholds: 15V and 14.6V
- Insertion delay: 213 ms
- Fault timeout period: 14.6 ms and 12.1 ms
- Restart time: 1.8 seconds
- Size: 4.0" x 1.38"

2 Board Configuration

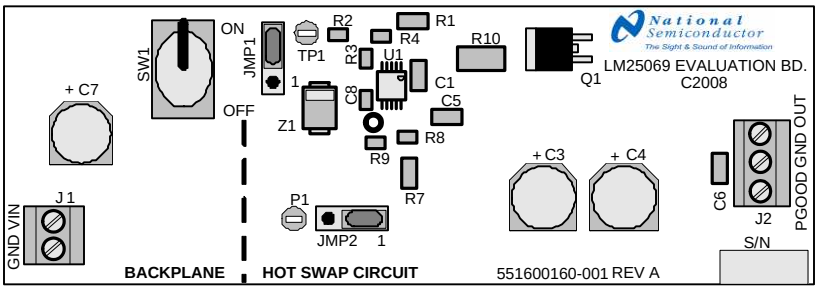

Figure 1. Evaluation Board - Top Side

A pictorial of the LM25069 evaluation board is shown in Figure 1, and the schematic is shown in Figure 2. The "BACKPLANE" section, at the left end of the board, represents the backplane voltage source. The vertical dashed line is the boundary between the backplane voltage source and the hot swap circuit input. In other words, it represents the edge connector in a card cage system. The toggle switch (SW1) provides a means to "connect" and "disconnect" the hot swap circuit from the backplane voltage source. The circuitry to the right of the vertical dashed line is the hot swap circuit. The system voltage is to be connected to the input terminal block (J1). The external load is to be connected to the output terminal block (J2). Capacitors C3 and C4 represent capacitance which is typically present on the input of the load circuit, and are present on this evaluation board so the turn-on characteristics of the LM25069 may be tested without having to connect a load.

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For a hot swap circuit to function reliably, capacitance is needed on the supply side of the system connector (C7). Its purpose is to minimize voltage transients which occur whenever the load current changes or is shut off. If the capacitance is not present, wiring inductance in the supply lines generate a voltage transient at shutoff which can exceed the absolute maximum rating of the LM25069, resulting in its destruction.

The LM25069EVB is supplied with pins 2-3 jumpered on JMP1, and pins 1-2 jumpered on JMP2.

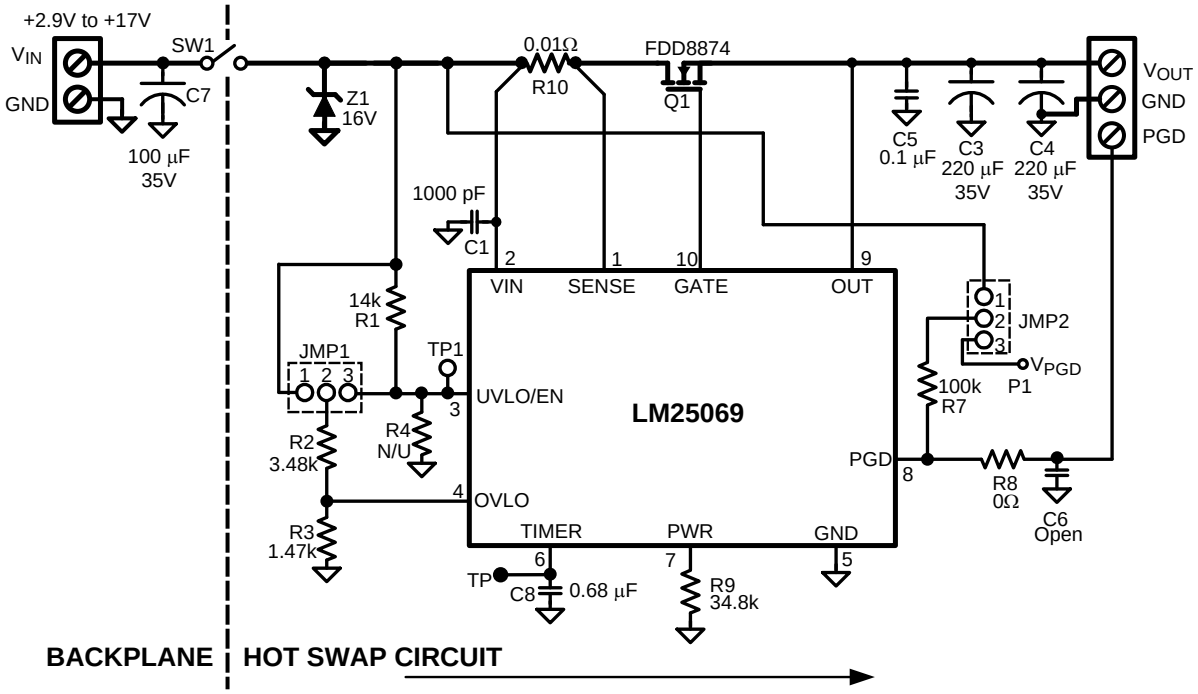

Figure 2. Evaluation Board Schematic

3 Theory of Operation

The LM25069 provides intelligent control of the power supply connections of a load which is to be connected to a live power source. The two primary functions of a hot swap circuit are in-rush current limiting during turn-on, and monitoring of the load current for faults during normal operation. Additional functions include Under-Voltage Lock-Out (UVLO) and Over-Voltage Lock-Out (OVLO) to ensure voltage is supplied to the load only when the system input voltage is within a defined range, power limiting in the series pass FET (Q1) during turn-on, and a Power Good logic output (PGD) to indicate the circuit status.

Upon applying the input voltage to the LM25069 (e.g., SW1 is switched on), Q1 is initially held off for the insertion delay (≅213 ms) to allow ringing and transients at the input to subside. At the end of the insertion delay, if the input voltage at VIN is between the UVLO and OVLO thresholds, Q1 is turned on in a controlled manner to limit the in-rush current. If the in-rush current were not limited during turn-on, the current would be high (very high!) as the load capacitors (C3, C4) charge up, limited only by the surge current capability of the voltage source, C7's characteristics, and the wiring resistance (a few milliohms). That very high current could damage the edge connector, PC board traces, and possibly the load capacitors receiving the high current. Additionally, the dV/dt at the load's input is controlled to reduce possible EMI problems.

The LM25069 limits in-rush current to a safe level using a two step process. In the first portion of the turn-on cycle, when the voltage differential across Q1 is highest, Q1's power dissipation is limited to a peak of 15W by monitoring its drain current (the voltage across R10) and its drain-to-source voltage. Their product is maintained constant by controlling the drain current as the drain-to-source voltage decreases (as the output voltage increases). This is shown in the constant power portion of Figure 3 where the drain current

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is increasing to I_{LIM}. When the drain currrent reaches the current limit threshold (5 Amps), it is then maintained constant as the output voltage continues to increase. When the output voltage reaches the input voltage (V_{DS} decreases to near zero), the drain current then reduces to a value determined by the load. Q1's gate-to-source voltage then increases to its final value. The circuit is now in normal operation mode.

Monitoring of the load current for faults during normal operation is accomplished using the current limit circuit described above. If the load current increases to 5 Amps (50 mV across R10), Q1's gate is controlled to prevent the current from increasing further. When current limiting takes effect, the fault timer limits the duration of the fault. At the end of the fault timeout period Q1 is shut off, denying current to the load. The LM25069-2 then initiates a restart every 1.8 seconds. The restart consists of turning on Q1 and monitoring the load current to determine if the fault is still present. After the fault is removed, the circuit powers up to normal operation at the next restart.

In a sudden overload condition (e.g., the output is shorted to ground), it is possible the current could increase faster than the response time of the current limit circuit. In this case, the circuit breaker sensor shuts off Q1's gate rapidly when the voltage across R10 reaches ≅95 mV. When the current reduces to the current limit threshold, the current limit circuitry then takes over.

The PGD logic level output is low during turn-on, and switches high when the output voltage at OUT has increased to within 1.3V of the input voltage, signifying the turn-on procedure is essentially complete. If the OUT voltage decreases more than 1.9V below VIN due to a fault, PGD switches low. The high level voltage at PGD can be any appropriate voltage up to +17V, and can be higher or lower than the voltages at VIN and OUT.

The UVLO and OVLO thresholds are set by resistors R1-R3. The threshold at the UVLO pin is 1.17V, and is 1.16V at the OVLO pin. The internal 20 µA current sources provide hysteresis for each of the thresholds.

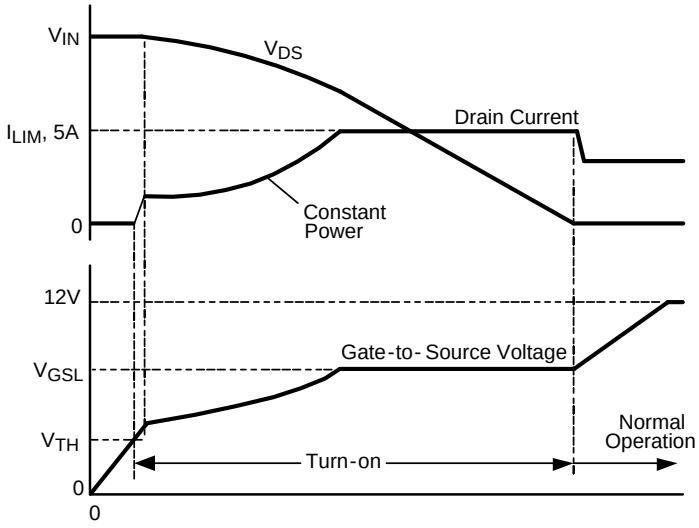

Figure 3. Power Up Using Power Limit and Current Limit

4 Board Layout and Probing Cautions

The pictorial in Figure 1 shows the placement of the circuit components. The following should be kept in mind when the board is powered:

1. Use CAUTION when probing the circuit to prevent injury, as well as possible damage to the circuit.
2. At maximum load current (5A), the wire size and length used to connect the power source and the load become important. The wires connecting this evaluation board to the power source SHOULD BE TWISTED TOGETHER to minimize inductance in those leads. The same applies for the wires connecting this board to the load. This recommendation is made in order to minimize high voltage transients from occurring when the load current is shut off.

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5 Board Connections/Startup

The input voltage source is connected to the J1 connector, and the load is connected to the J2 connector at the OUT and GND terminals. USE TWISTED WIRES. A voltmeter should be connected to the input terminals, and one to the output terminals. The input current can be monitored with an ammeter or current probe. To monitor the status of the PGD output, connect a voltmeter from PGOOD to GND on the J2 terminal block. Put the toggle switch in the ON position.

Increase the input voltage gradually. The input current should remain less than 2 mA until the upper UVLO threshold is reached. When the threshold is reached, Q1 is turned on. If viewed on an oscilloscope, the input current increases as shown in Figure 3 before settling at the value defined by the load. The turn-on timing depends on the input voltage, power limit setting, current limit setting, and the final load current, and is between ≅3.0 ms with no load current, and ≅6.5 ms with a 3.7A load current, with VIN = 14V. See Figure 9 and Figure 10.

6 Circuit Parameter Changes

6.1 Current Limit

The current limit threshold is set by R10 according to the following equation:

$$I_{LIM} = 50\ mV/R10 \quad (1)$$

If the load current increases such that the voltage across R10 reaches 50 mV, the LM25069 then modulates Q1's gate to limit the current to that level. This evaluation board is supplied with a 10 mohm resistor for R10, resulting in a current limit of 5A. To change the current limit threshold replace R10 with a resistor of the required value and power capability.

6.2 Power Limit

The maximum power dissipated in Q1 during turn-on, or due to a fault, is limited by R9 and R10 according to the following equation:

$$P_{FET(LIM)} = \frac{R9}{2.32 \times 10^5 \times R10} \quad (2)$$

With the components supplied on the evaluation board, $P_{FET(LIM)}$ = 15W. During turn-on, when the voltage across Q1 is high, its gate is modulated to limit its drain current so the power dissipated in Q1 does not exceed 15W. As the drain-to-source voltage decreases, the drain current increases, maintaining the power dissipation constant. When the drain current reaches the current limit threshold set by R10, the current is then maintained constant until the output voltage reaches its final value. The current then decreases to a value determined by the load. See Figure 3, Figure 9, and Figure 10.

Each time Q1 is subjected to the maximum power limit conditions it is internally stressed for a few milliseconds. For this reason, the power limit threshold must be set lower than the limit indicated by the FET's SOA chart. In this evaluation board, the power limit threshold is set at 15W, compared to ≅40W limit indicated in the Fairchild FDD8874 data sheet. The FET manufacturer should be contacted for more information on this subject.

6.3 Insertion Time

The insertion time starts when the input voltage at VIN reaches 2.6V, and its duration is equal to

$$t_{INSERTION} = C8 \times 3.13 \times 10^5 \quad (3)$$

During the insertion time, Q1 is held off regardless of the voltage at VIN. This delay allows ringing and transients at VIN subside before the input voltage is applied to the load via Q1. The insertion time on this evaluation board is ≅213 ms. See Figure 8.

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7 Fault Detection and Restart

If the load current increases to the fault level (the current limit threshold, 5A), an internal current source charges the timing capacitor at the TIMER pin. When the voltage at the TIMER pin reaches 1.72V, the fault timeout period is complete, and the LM25069 shuts off Q1. The restart sequence then begins, consisting of seven cycles at the TIMER pin between 1.72V and 1V, as shown in Figure 4. When the voltage at the TIMER pin reaches 0.3V during the eighth high-to-low ramp, Q1 is turned on. If the fault is still present, the fault timeout period and the restart sequence repeat.

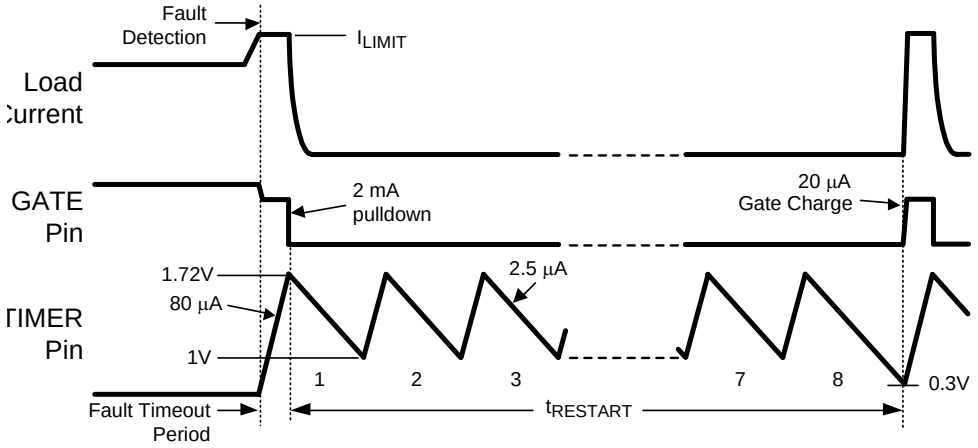

Figure 4. Fault Timeout and Restart Sequence

The initial fault timeout period is equal to:

$$t_{FAULT(Init)} = C_T \times 2.15 \times 10^4 \quad (4)$$

The restart fault timeout period is equal to:

$$t_{FAULT(Restart)} = C_T \times 1.776 \times 10^4 \quad (5)$$

The restart time is equal to:

$$t_{Restart} = C_T \times 2.65 \times 10^6 \quad (6)$$

The waveform at the TIMER pin can be monitored at the test pad located between C8 and R9. In this evaluation board the initial fault timeout period is 14.6 ms, the restart fault timeout period is 12.1 ms, and the restart time is 1.8 seconds. See Figure 11, Figure 12, and Figure 13.

8 UVLO/OVLO Input Voltage Thresholds

As supplied, the input voltage UVLO thresholds on this evaluation board are approximately 4.8V increasing, and 4.5V decreasing. The OVLO thresholds are approximately 15V increasing, and 14.6V decreasing. The four thresholds are determined by resistors R1-R4. The threshold at the UVLO pin is 1.17V, and is 1.16V at the OVLO pin, and internal 20 µA current sources provide hysteresis for each threshold. See the *LM25069 Positive Low Voltage Power Limiting Hot Swap Controller* (SNVS607 for more details.

8.1 Option A

This evaluation board is supplied with the jumper at JMP1 on pins 2-3, resulting in the configuration shown in Figure 5.

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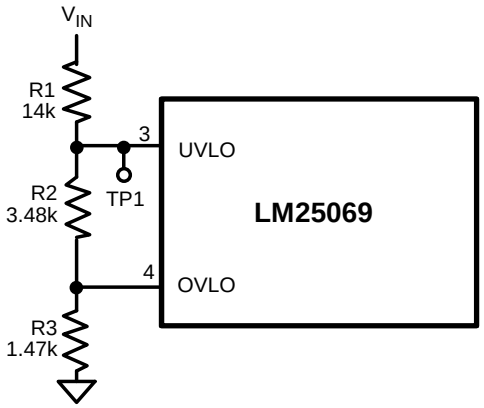

Figure 5. UVLO, OVLO Inputs (Option A)

To change the thresholds in this configuration, resistors R1-R3 are calculated using the following procedure:

- Choose the upper UVLO threshold (V_{UVH}), and the lower UVLO threshold (V_{UVL}).
- Choose the upper OVLO threshold (V_{OVH})
- The lower OVLO threshold (V_{OVL}) cannot be chosen in advance in this case, but is determined after the values for R1-R3 are determined. If V_{OVL} must be accurately defined in addition to the other three thresholds, see Option B below.

The resistors are calculated as follows:

$$R1 = \frac{V_{UVH} - V_{UVL}}{20\ \mu A} \quad (7)$$

$$R3 = \frac{1.16V \times R1 \times V_{UVL}}{V_{OVH} \times (V_{UVL} - 1.17V)} \quad (8)$$

$$R2 = \frac{1.17V \times R1}{(V_{UVL} - 1.17V)} - R3 \quad (9)$$

The lower OVLO threshold is calculated from:

$$V_{OVL} = [(R1 + R2) \times ((\frac{1.16V}{R3}) - 20\ \mu A)] + 1.16V \quad (10)$$

8.2 Option B

If all four thresholds must be determined accurately, move the jumper at JMP1 to pins 1-2, and add R4, resulting in the configuration shown in Figure 6.

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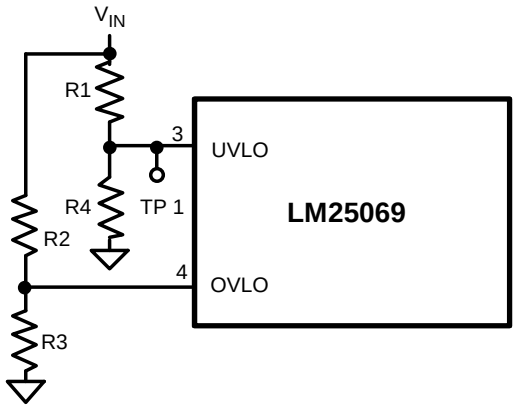

Figure 6. UVLO, OVLO Inputs (Option B)

The four resistor values are calculated as follows:

Choose the upper and lower UVLO thresholds (V_{UVH}) and (V_{UVL}).

$$R1 = \frac{V_{UVH} - V_{UVL}}{20\ \mu A} \quad (11)$$

$$R4 = \frac{1.17V \times R1}{(V_{UVL} - 1.17V)} \quad (12)$$

Choose the upper and lower OVLO threshold (V_{OVH}) and (V_{OVL}).

$$R2 = \frac{V_{OVH} - V_{OVL}}{20\ \mu A} \quad (13)$$

$$R3 = \frac{1.16V \times R2}{(V_{OVH} - 1.16V)} \quad (14)$$

8.3 Option C

The minimum UVLO level is obtained by positioning the jumper at JMP1 on pins 1-2, and leaving R4 open, resulting in the configuration shown in Figure 7. Q1 is switched on when the voltage at VIN reaches the POR threshold (≅2.6V). The OVLO thresholds are set by R2 and R3, and their values are calculated using the procedure in Option B. The value for R1 is not critical, and can be as supplied.

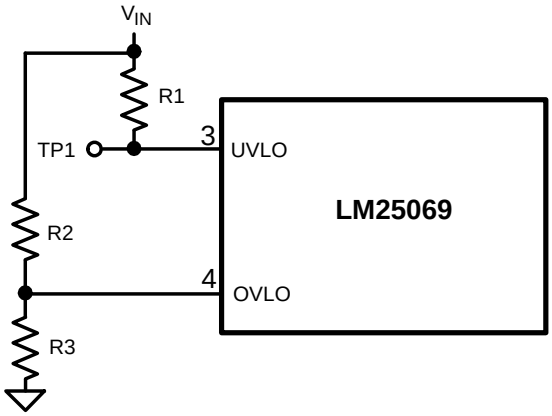

Figure 7. Minimum UVLO Threshold, Adjustable OVLO

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8.4 OPTION D

The OVLO function can be disabled by removing the jumper from JMP1. The UVLO thresholds are set by R1 and R4 using the procedure in option B above.

9 Shutdown

With the circuit in normal operation, the LM25069 can be shut down by grounding the UVLO pin. Test point TP1, located next to JMP1, can be used for this purpose.

10 Power Good Output

The PGOOD logic output provides an indication of the circuit's condition. This output is high when the circuit is in normal operation - the OUT voltage is within 1.3V of the input. PGOOD is low when the circuit is shutdown, either intentionally or due to a fault. PGOOD is also high when VIN is less than 1.6V.

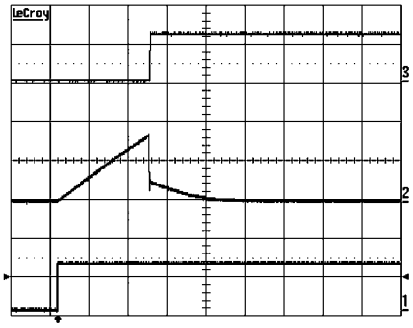
This EVB is supplied with pins 1-2 jumpered on JMP2, powering the PGD pin from the input voltage through a 100 kΩ pull-up resistor. To change the high level PGOOD voltage, move the jumper on JMP2 to pins 2-3, and supply the appropriate pull-up voltage to terminal P1 (located next to JMP2). If the UVLO pin is taken low to disable the LM25069, PGOOD switches low within 10 µs without waiting for the OUT voltage to fall.

If a delay at the PGOOD output is desired, a resistor and capacitor can be added at positions R8 and C6.

11 LM25069-1 Latch Version

The LM25069-2 supplied on this evaluation board provides a restart attempt after a fault detection, as described above. The companion Hot-Swap IC, the LM25069-1, latches off after a fault detection, with external control required for restart. Restart is accomplished by momentarily taking the UVLO pin below its threshold, or by removing and re-applying the input voltage at VIN. Contact the nearest Texas Instruments sales office to obtain samples of the LM25069-1.

12 Performance Characteristics



Horizontal Resolution: 100 ms/div
Trace 1: V_{IN}, 10V/div
Trace 2: TIMER Pin, 1V/div
Trace 3: V_{OUT}, 10V/div
V_{IN} = 12V, C_T = 0.68 µF

Figure 8. Insertion Time Delay

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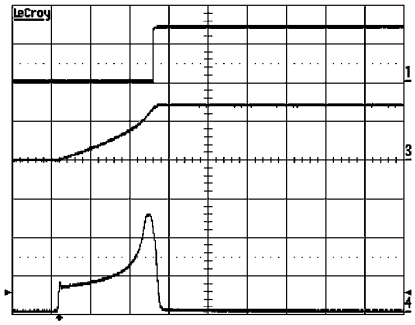
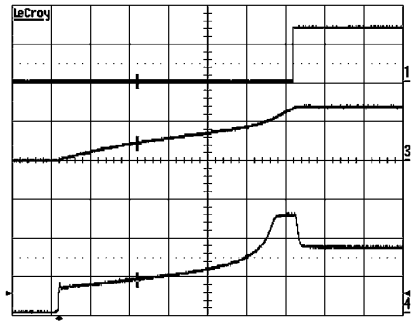


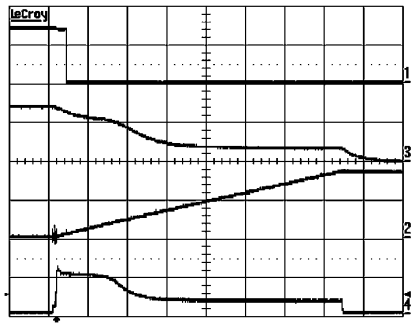
Horizontal Resolution: 1 ms/div
Trace 1: PGD Pin, 10V/div
Trace 3: V_{OUT}, 10V/div
Trace 4: Input Current, 2A/div
V_{IN} = 14V, Load = 1 kΩ

Figure 9. Turn-On Sequence with Minimal Load Current



Horizontal Resolution: 1 ms/div
Trace 1: PGD Pin, 10V/div
Trace 3: V_{OUT}, 10V/div
Trace 4: Input Current, 2A/div
V_{IN} = 14V, Load = 4Ω

Figure 10. Turn-On Sequence into a 4Ω Load



Horizontal Resolution: 2 ms/div
Trace 1: PGD Pin, 10V/div
Trace 2: TIMER Pin, 1V/div
Trace 3: V_{OUT}, 10V/div
Trace 4: Input Current, 5A/div
V_{IN} = 14V, Load Switched from 1 kΩ to 2Ω
C_T = 0.68 µF

Figure 11. Initial Fault Timeout

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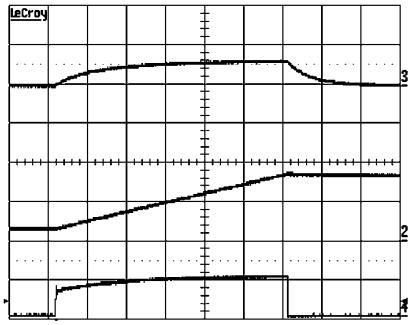
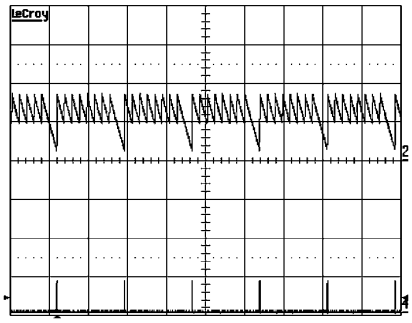


Horizontal Resolution: 2 ms/div
Trace 2: TIMER Pin, 1V/div
Trace 3: V_{OUT}, 10V/div
Trace 4: Input Current, 2A/div
V_{IN} = 14V, Load = 3Ω, C_T = 0.68 µF

Figure 12. Restart Fault Timeout



Horizontal Resolution: 1sec/div
Trace 2: TIMER Pin, 1V/div
Trace 4: Input Current, 2A/div
V_{IN} = 14V, Load = 2Ω, C_T = 0.68 µF

Figure 13. Restart Timing

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13 Bill of Materials

Item	Description	Mfg., Part No.	Package	Value
C1	Ceramic Capacitor	TDK C2012X7R2A102M	0805	1000 pF, 100V
C3, C4	Alum. Elec. Capacitor	Panasonic EEE-TG1V221UP	Surf. Mount	220 µF, 35V
C5	Ceramic Capacitor	TDK C3216X7R2A104M	1206	0.1 µF, 100V
C6	Unpopulated			
C7	Alum. Elec. Capacitor	Panasonic EEE-TG1V101P	Surf. Mount	100 µF, 35V
C8	Ceramic Capacitor	MuRata GRM188R61A684KA61D or Panasonic ECJ-2FB1A684K	0805	0.68 µF, 10V or higher
Q1	MOSFET	Fairchild FDD8874	TO-252	30V, 116A
R1	Resistor	Vishay CRCW120614K0F	1206	14k
R2	Resistor	Vishay CRCW08053K48F	0805	3.48k
R3	Resistor	Vishay CRCW080551K47F	0805	1.47k
R4	Unpopulated			
R7	Resistor	Vishay CRCW1206100KF	1206	100k, ¼ W
R8	Resistor	Vishay CRCW08050000Z	0805	Zero ohm jumper
R9	Resistor	Vishay CRCW080534K8F	0805	34.8k
R10	Resistor	Vishay WSL2010R0100F	2010	0.010 ohm, ½ W
SW1	Toggle Switch	NKK M2012SS1W03-RO		SPDT switch, 6A
U1	Hot Swap IC	Texas Instruments LM25069-2	VSSOP-10	
Z1	Trans. Suppressor	Diodes Inc. SMBJ16A	SMB	16V

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14 PC Board Layout

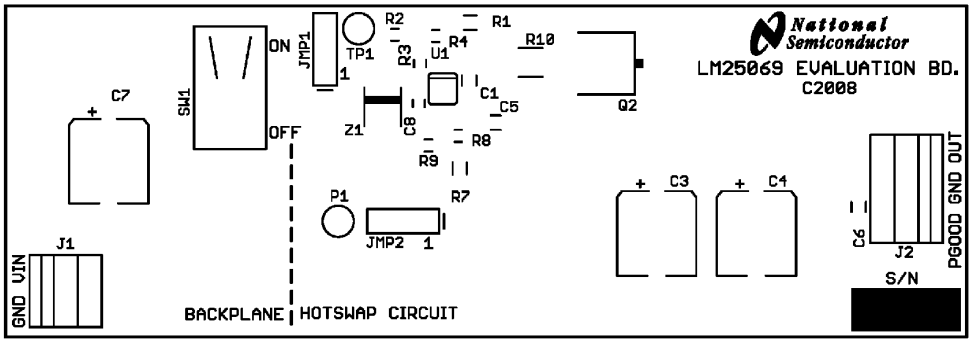

Figure 14. Board Silkscreen

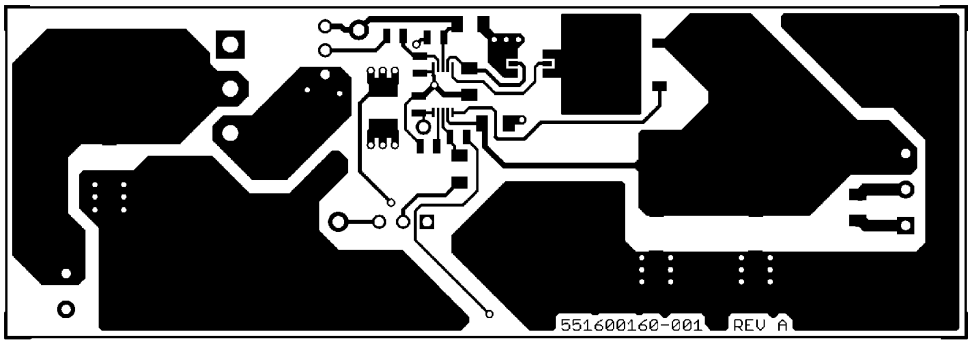

Figure 15. Board Top Layer

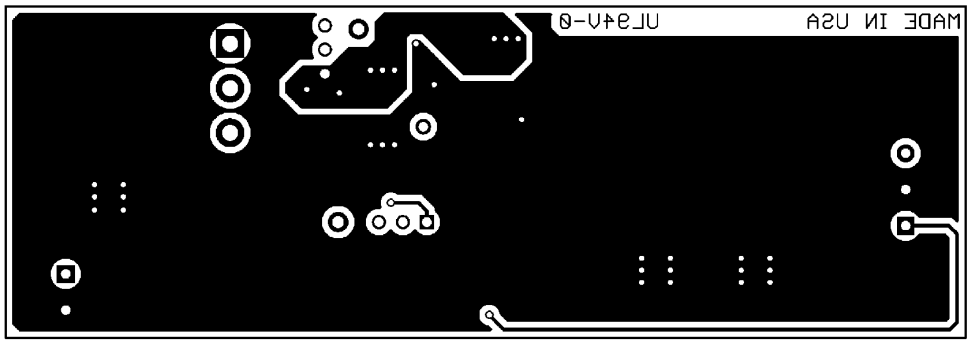

Figure 16. Board Bottom Layer (viewed from top)

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