

## 74LVTH16835 Low Voltage 18-Bit Universal Bus Driver with Bushold and 3-STATE Outputs

### General Description

The LVTH16835 is an 18-bit universal bus driver that combines D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.

Data flow is controlled by output-enable ( $\overline{OE}$ ), latch-enable (LE), and clock (CLK) inputs. The device operates in Transparent Mode when LE is held HIGH. The device operates in clocked mode when LE is LOW and CLK is toggled. Data transfers from the Inputs ( $A_n$ ) to Outputs ( $Y_n$ ) on a Positive Edge Transition of the Clock. When  $\overline{OE}$  is LOW, the output data is enabled. When  $\overline{OE}$  is HIGH the output port is in a high impedance state.

The LVTH16835 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

The bus driver is designed for low voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH16835 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

### Features

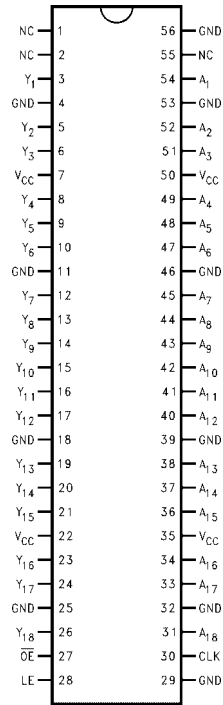
- Input and output interface capability to systems at 5V  $V_{CC}$
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power up/down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- ESD Performance:
  - Human-Body Model > 2000V
  - Machine Model > 200V
  - Charged-Device Model > 1000V

### Ordering Code:

Order Number	Package Number	Package Description
74LVTH16835MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
74LVTH16835MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram



### Pin Descriptions

Pin Names	Description
A <sub>1</sub> -A <sub>18</sub>	Data Register Inputs
Y <sub>1</sub> -Y <sub>18</sub>	3-STATE Outputs
CLK	Clock Pulse Input
$\overline{OE}$	Output Enable Input
LE	Latch Enable Input

### Function Table

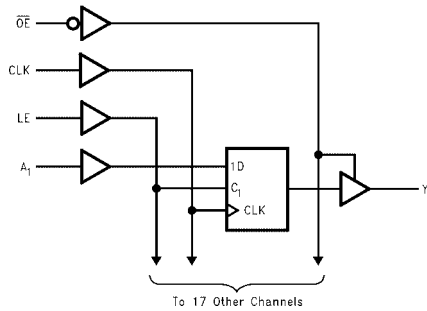
Inputs				Output
$\overline{OE}$	LE	CLK	A <sub>n</sub>	Y <sub>n</sub>
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	Y <sub>0</sub> (Note 1)
L	L	L	X	Y <sub>0</sub> (Note 2)

H = HIGH Voltage Level      L = LOW Voltage Level  
 X = Immaterial                  Z = High Impedance  
 ↑ = HIGH-to-LOW Clock Transition

**Note 1:** Output level before the indicated steady-state input conditions were established, provided that CLK was HIGH before LE went LOW.

**Note 2:** Output level before the indicated steady-state input conditions were established.

### Logic Diagram



Absolute Maximum Ratings <sup>(Note 3)</sup>				
Symbol	Parameter	Value	Conditions	Units
V <sub>CC</sub>	Supply Voltage	-0.5 to +4.6		V
V <sub>I</sub>	DC Input Voltage	-0.5 to +7.0		V
V <sub>O</sub>	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to +7.0	Output in HIGH or LOW State (Note 4)	V
I <sub>IK</sub>	DC Input Diode Current	-50	V <sub>I</sub> < GND	mA
I <sub>OK</sub>	DC Output Diode Current	-50	V <sub>O</sub> < GND	mA
I <sub>O</sub>	DC Output Current	64	V <sub>O</sub> > V <sub>CC</sub> Output at HIGH State	mA
		128	V <sub>O</sub> > V <sub>CC</sub> Output at LOW State	
I <sub>CC</sub>	DC Supply Current per Supply Pin	±64		mA
I <sub>GND</sub>	DC Ground Current per Ground Pin	±128		mA
T <sub>STG</sub>	Storage Temperature	-65 to +150		°C
Recommended Operating Conditions				
Symbol	Parameter	Min	Max	Units
V <sub>CC</sub>	Supply Voltage	2.7	3.6	V
V <sub>I</sub>	Input Voltage	0	5.5	V
I <sub>OH</sub>	HIGH-Level Output Current		-32	mA
I <sub>OL</sub>	LOW-Level Output Current		64	mA
T <sub>A</sub>	Free-Air Operating Temperature	-40	85	°C
Δt/ΔV	Input Edge Rate, V <sub>IN</sub> = 0.8V–2.0V, V <sub>CC</sub> = 3.0V	0	10	ns/V
<p><b>Note 3:</b> Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.</p> <p><b>Note 4:</b> I<sub>O</sub> Absolute Maximum Rating must be observed.</p>				

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units	Conditions	
			Min	Max			
V <sub>IK</sub>	Input Clamp Diode Voltage	2.7		-1.2	V	I <sub>I</sub> = -18 mA	
V <sub>IH</sub>	Input HIGH Voltage	2.7-3.6	2.0		V	V <sub>O</sub> ≤ 0.1V or V <sub>O</sub> ≥ V <sub>CC</sub> - 0.1V	
V <sub>IL</sub>	Input LOW Voltage	2.7-3.6		0.8			
V <sub>OH</sub>	Output HIGH Voltage	2.7-3.6	V <sub>CC</sub> - 0.2		V	I <sub>OH</sub> = -100 μA	
		2.7	2.4		V	I <sub>OH</sub> = -8 mA	
		3.0	2.0		V	I <sub>OH</sub> = -32 mA	
V <sub>OL</sub>	Output LOW Voltage	2.7		0.2	V	I <sub>OL</sub> = 100 μA	
		2.7		0.5	V	I <sub>OL</sub> = 24 mA	
		3.0		0.4	V	I <sub>OL</sub> = 16 mA	
		3.0		0.5	V	I <sub>OL</sub> = 32 mA	
		3.0		0.55	V	I <sub>OL</sub> = 64 mA	
I <sub>I(HOLD)</sub>	Bushold Input Minimum Drive	3.0	75		μA	V <sub>I</sub> = 0.8V	
			-75		μA	V <sub>I</sub> = 2.0V	
I <sub>I(OD)</sub>	Bushold Input Over-Drive Current to Change State	3.0	500		μA	(Note 5)	
			-500		μA	(Note 6)	
I <sub>I</sub>	Input Current	3.6		10	μA	V <sub>I</sub> = 5.5V	
		Control Pins	3.6		±1	μA	V <sub>I</sub> = 0V or V <sub>CC</sub>
		Data Pins	3.6		-5	μA	V <sub>I</sub> = 0V
I <sub>OFF</sub>	Power Off Leakage Current	0		±100	μA	0V ≤ V <sub>I</sub> or V <sub>O</sub> ≤ 5.5V	
I <sub>PU/PD</sub>	Power Up/Down 3-STATE Output Current	0-1.5V		±100	μA	V <sub>O</sub> = 0.5V to 3.0V V <sub>I</sub> = GND or V <sub>CC</sub>	
I <sub>OZL</sub>	3-STATE Output Leakage Current	3.6		-5	μA	V <sub>O</sub> = 0.5V	
I <sub>OZH</sub>	3-STATE Output Leakage Current	3.6		5	μA	V <sub>O</sub> = 3.0V	
I <sub>OZH+</sub>	3-STATE Output Leakage Current	3.6		10	μA	V <sub>CC</sub> < V <sub>O</sub> ≤ 5.5V	
I <sub>CCH</sub>	Power Supply Current	3.6		0.19	mA	Outputs HIGH	
I <sub>CCL</sub>	Power Supply Current	3.6		5	mA	Outputs LOW	
I <sub>CCZ</sub>	Power Supply Current	3.6		0.19	mA	Outputs Disabled	
I <sub>CCZ+</sub>	Power Supply Current	3.6		0.19	mA	V <sub>CC</sub> ≤ V <sub>O</sub> ≤ 5.5V, Outputs Disabled	
ΔI <sub>CC</sub>	Increase in Power Supply Current (Note 7)	3.6		0.2	mA	One Input at V <sub>CC</sub> - 0.6V Other Inputs at V <sub>CC</sub> or GND	

**Note 5:** An external driver must source at least the specified current to switch from LOW-to-HIGH.

**Note 6:** An external driver must sink at least the specified current to switch from HIGH-to-LOW.

**Note 7:** This is the increase in supply current for each input that is at the specified voltage level rather than V<sub>CC</sub> or GND.

## Dynamic Switching Characteristics (Note 8)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			Units	Conditions C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω
			Min	Typ	Max		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3		0.8		V	(Note 9)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3		-0.8		V	(Note 9)

**Note 8:** Characterized in SSOP package. Guaranteed parameter, but not tested.

**Note 9:** Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics						
Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, C_L = 50 \text{ pF}, R_L = 500 \Omega$				Units
		$V_{CC} = 3.3 \pm 0.3\text{V}$		$V_{CC} = 2.7\text{V}$		
		Min	Max	Min	Max	
$f_{MAX}$	CLK to Y	150		150		MHz
$t_{PLH}$	Propagation Delay	1.3	5.1	1.3	5.5	ns
$t_{PHL}$	A to Y	1.2	4.7	1.3	5.2	
$t_{PLH}$	Propagation Delay	1.5	5.4	1.5	6.0	ns
$t_{PHL}$	LE to Y	1.4	5.1	1.5	5.7	
$t_{PLH}$	Propagation Delay	1.5	5.5	1.5	6.1	ns
$t_{PHL}$	CLK to Y	1.4	5.1	1.5	5.7	
$t_{PZH}$	Output Enable Time	0.9	4.7	1.3	5.5	ns
$t_{PZL}$		1.3	5.2	1.3	6.4	
$t_{PHZ}$	Output Disable Time	1.7	5.8	1.7	6.3	ns
$t_{PLZ}$		1.6	5.8	1.7	6.3	
$t_s$	Setup Time	A before CLK	2.1		2.4	ns
		A before LE, CLK HIGH	2.3		1.5	
		A before LE, CLK LOW	1.5		1.5	
$t_H$	Hold Time	A after CLK	1.0		1.0	ns
		A after LE	0.8		1.0	
$t_W$	Pulse Duration	LE HIGH	3.3		3.3	ns
		CLK HIGH or LOW	3.3		3.3	
$t_{OSLH}$	Output to Output Skew		1.0		1.0	ns
$t_{OSHL}$	(Note 10)		1.0		1.0	

**Note 10:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ).

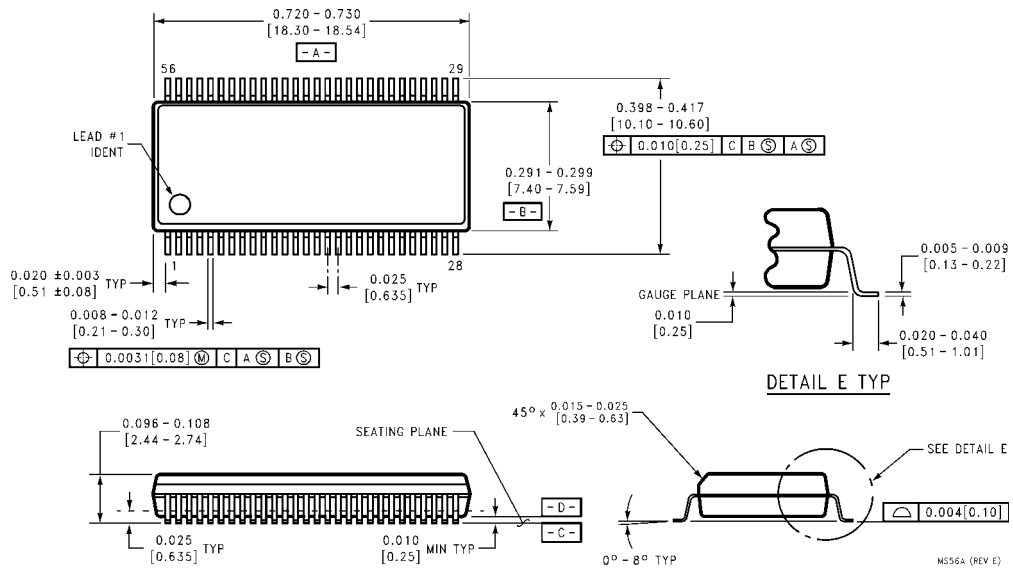
### Capacitance (Note 11)

Symbol	Parameter	Conditions	Typical	Units
$C_{IN}$	Input Capacitance	$V_{CC} = 0\text{V}, V_I = 0\text{V or } V_{CC}$	4	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 3.0\text{V}, V_O = 0\text{V or } V_{CC}$	8	pF

**Note 11:** Capacitance is measured at frequency  $f = 1 \text{ MHz}$ , per MIL-STD-883, Method 3012.

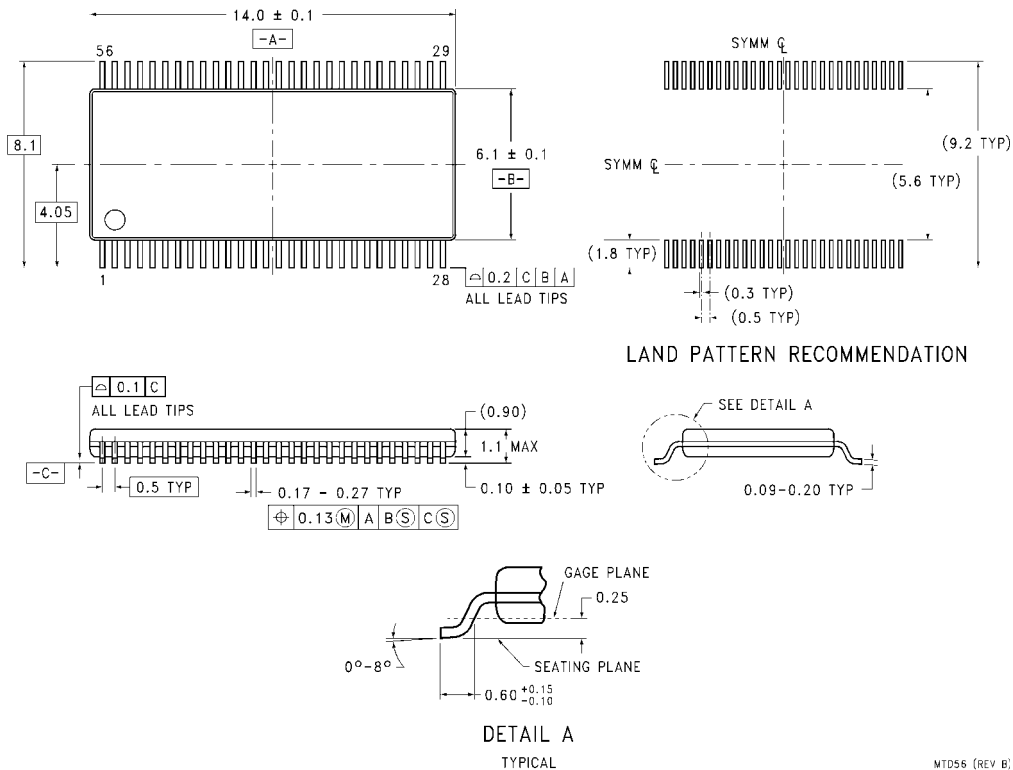
74LVTH16835

**Physical Dimensions** inches (millimeters) unless otherwise noted



**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide  
Package Number MS56A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide  
Package Number MTD56**

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