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Kind regards,

Team Nexperia

# DATA SHEET

## **BSP230**

P-channel enhancement mode  
vertical D-MOS transistor

Product specification  
Supersedes data of 1997 Jun 17  
File under Discrete Semiconductors, SC13b

1997 Oct 21

# P-channel enhancement mode vertical D-MOS transistor

**BSP230**

**FEATURES**

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

**APPLICATIONS**

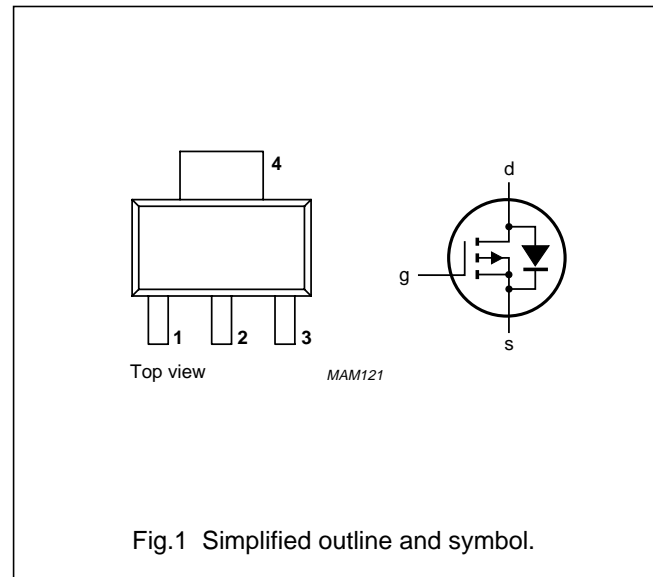
- Line current interruptor in telephone sets
- Relay, high speed and line transformer drivers.

**DESCRIPTION**

P-channel enhancement mode vertical D-MOS transistor in a SOT223 plastic SMD package.

**PINNING - SOT223**

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain



**CAUTION**

The device is supplied in an antistatic package.  
The gate-source input must be protected against static discharge during transport or handling.

**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	–300	V
$V_{GSO}$	gate-source voltage (DC)	open drain	–	±20	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -1 \text{ mA}; V_{DS} = V_{GS}$	–1.95	–2.8	V
$I_D$	drain current (DC)		–	–210	mA
$R_{DSon}$	drain-source on-state resistance	$I_D = -170 \text{ mA}; V_{GS} = -10 \text{ V}$	–	17	$\Omega$
$P_{tot}$	total power dissipation	$T_{amb} \leq 25 \text{ }^\circ\text{C}$	–	1.5	W

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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	–300	V
$V_{GSO}$	gate-source voltage (DC)	open drain	–	±20	V
$I_D$	drain current (DC)		–	–210	mA
$I_{DM}$	peak drain current		–	–0.75	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$ ; note 1	–	1.5	W
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	operating junction temperature		–	150	°C

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	83.3	K/W

### Note to the Limiting values and Thermal characteristics

- Device mounted on an epoxy printed-circuit board,  $40 \times 40 \times 1.5$  mm; mounting pad for drain lead minimum  $6\text{ cm}^2$ .

## CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$ ; $I_D = -10\ \mu\text{A}$	–300	–	–	V
$V_{GSth}$	gate-source threshold voltage	$V_{DS} = V_{GS}$ ; $I_D = -1\text{ mA}$	–1.95	–	–2.8	V
$I_{DSS}$	drain-source leakage current	$V_{GS} = 0$ ; $V_{DS} = -240\text{ V}$	–	–	–100	nA
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 20\text{ V}$ ; $V_{DS} = 0$	–	–	±100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}$ ; $I_D = -170\text{ mA}$	–	–	17	$\Omega$
$ y_{fs} $	forward transfer admittance	$V_{DS} = -25\text{ V}$ ; $I_D = -170\text{ mA}$	100	–	–	mS
$C_{iss}$	input capacitance	$V_{GS} = 0$ ; $V_{DS} = -25\text{ V}$ ; $f = 1\text{ MHz}$	–	60	90	pF
$C_{oss}$	output capacitance	$V_{GS} = 0$ ; $V_{DS} = -25\text{ V}$ ; $f = 1\text{ MHz}$	–	15	30	pF
$C_{rss}$	reverse transfer capacitance	$V_{GS} = 0$ ; $V_{DS} = -25\text{ V}$ ; $f = 1\text{ MHz}$	–	5	15	pF
<b>Switching times</b> (see Figs 2 and 3)						
$t_{on}$	turn-on time	$V_{GS} = 0$ to $-10\text{ V}$ ; $V_{DD} = -50\text{ V}$ ; $I_D = -250\text{ mA}$	–	5	10	ns
$t_{off}$	turn-off time	$V_{GS} = -10$ to $0\text{ V}$ ; $V_{DD} = -50\text{ V}$ ; $I_D = -250\text{ mA}$	–	15	30	ns

P-channel enhancement mode  
vertical D-MOS transistor

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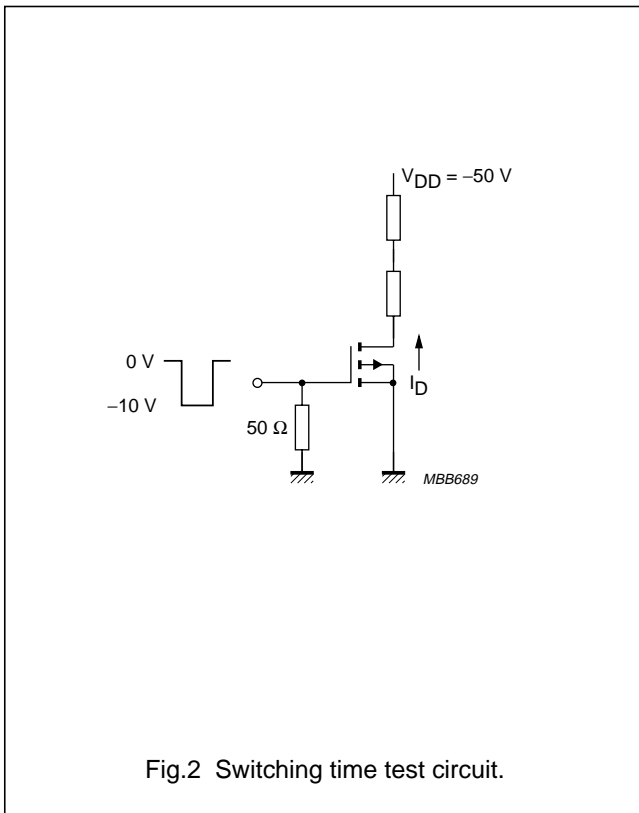


Fig.2 Switching time test circuit.

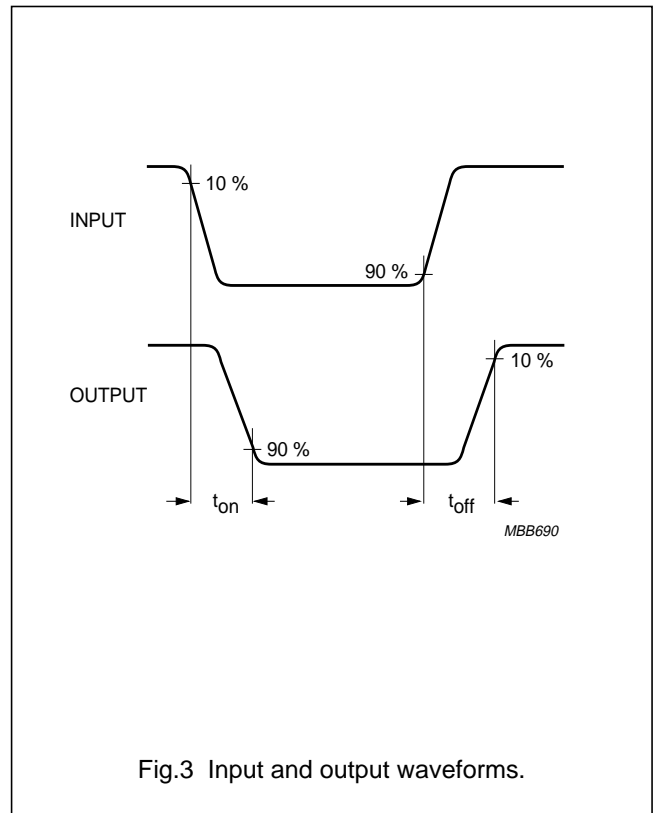


Fig.3 Input and output waveforms.

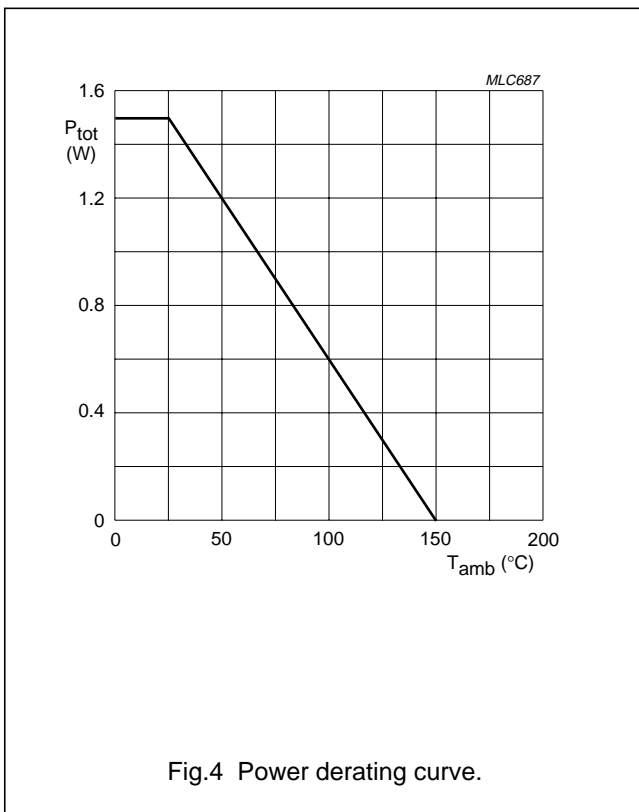
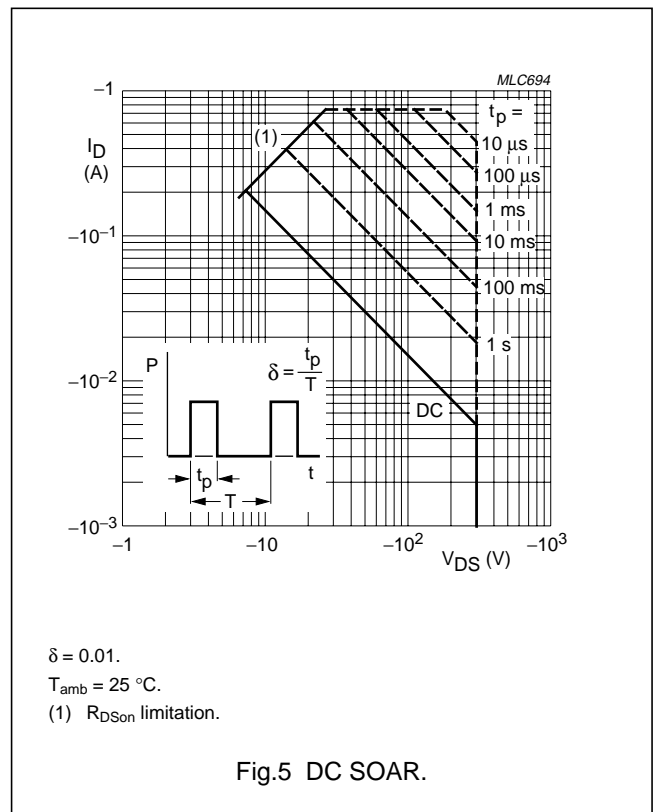


Fig.4 Power derating curve.

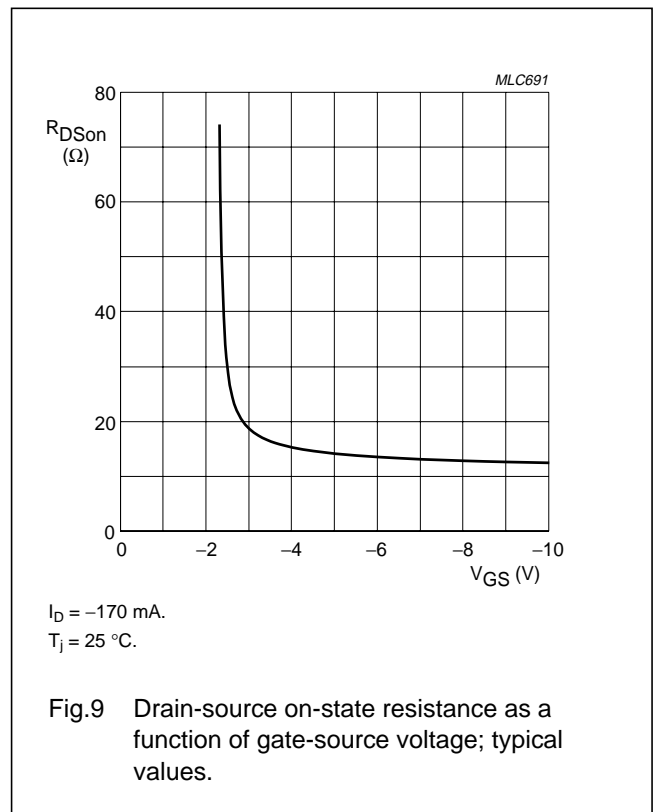
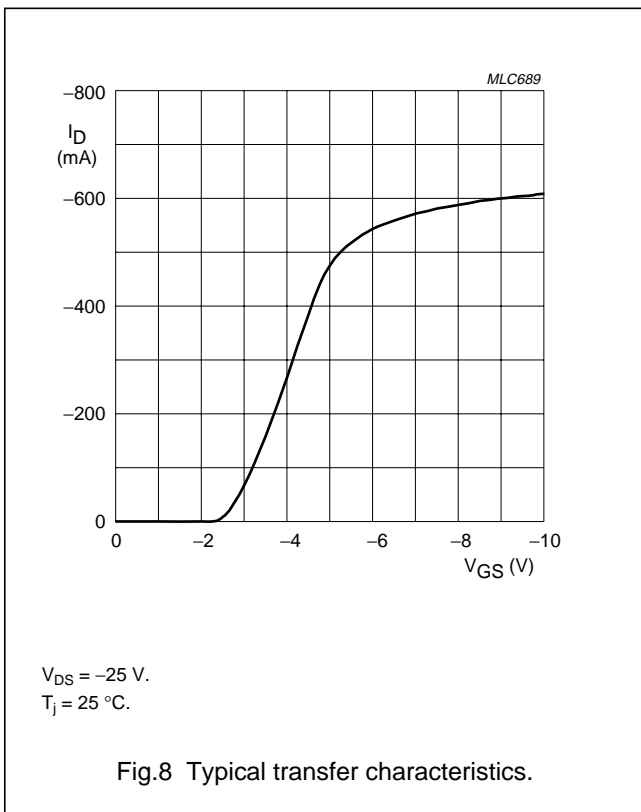
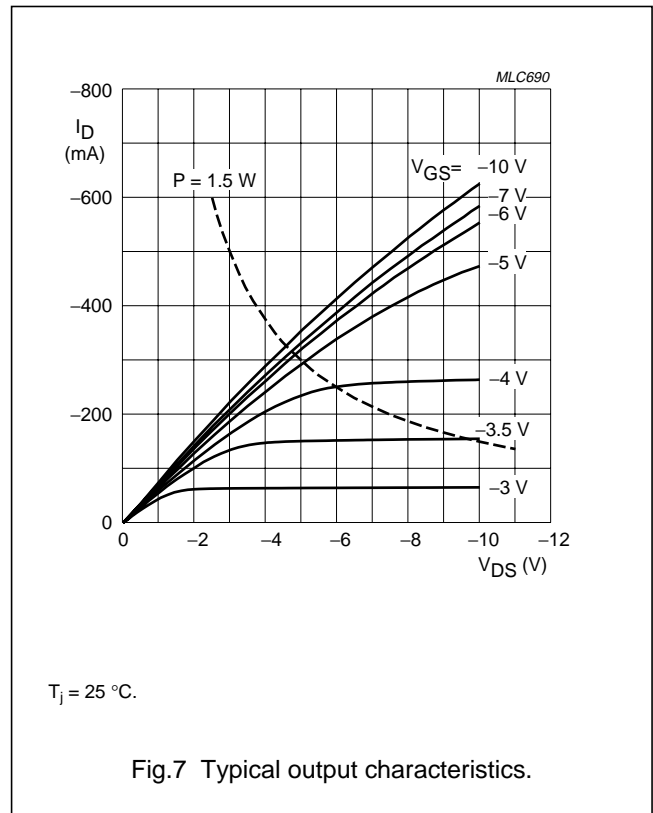
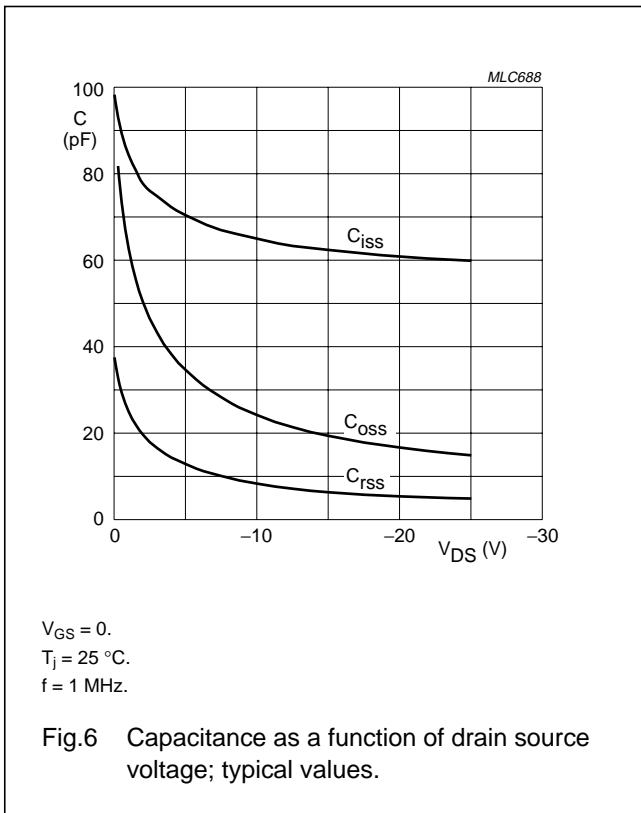


$\delta = 0.01$ .  
 $T_{amb} = 25\text{ }^{\circ}\text{C}$ .  
 (1)  $R_{DSon}$  limitation.

Fig.5 DC SOAR.

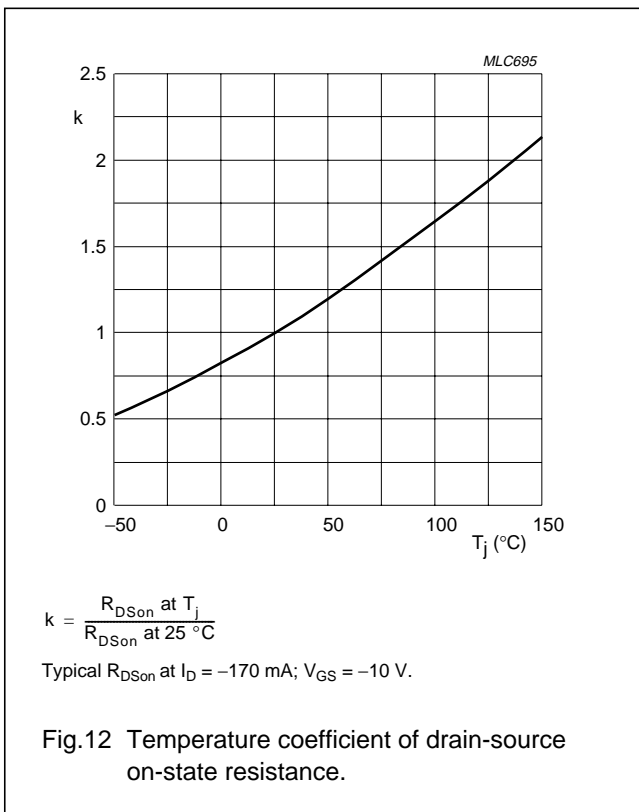
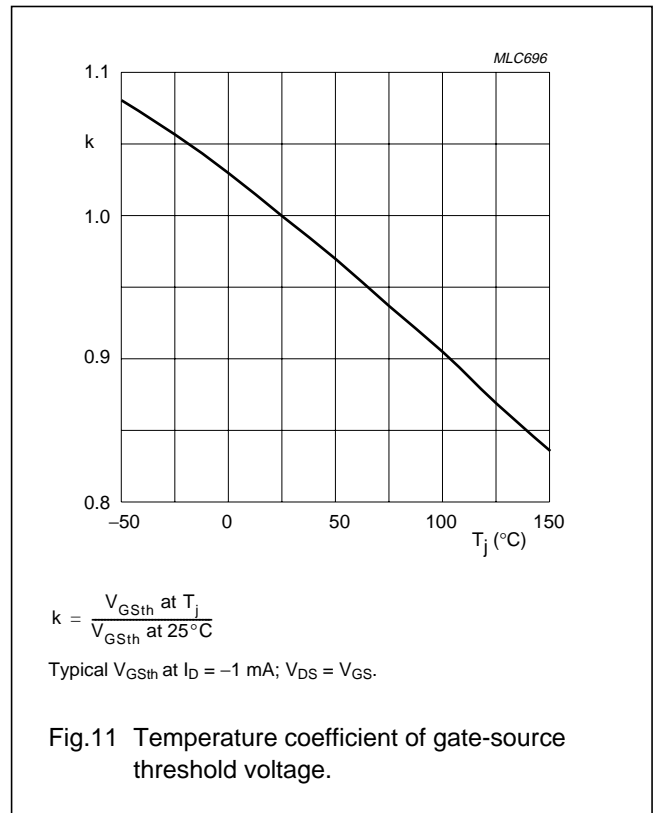
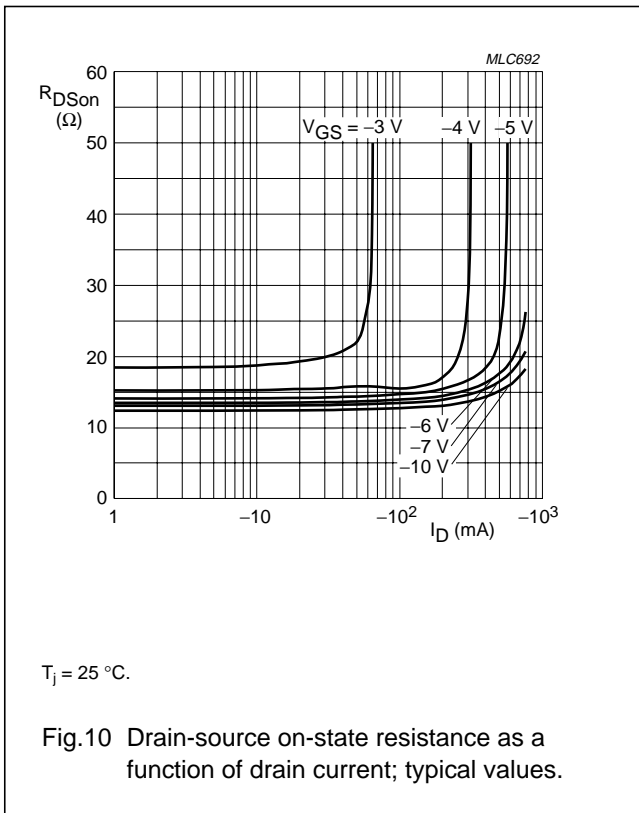
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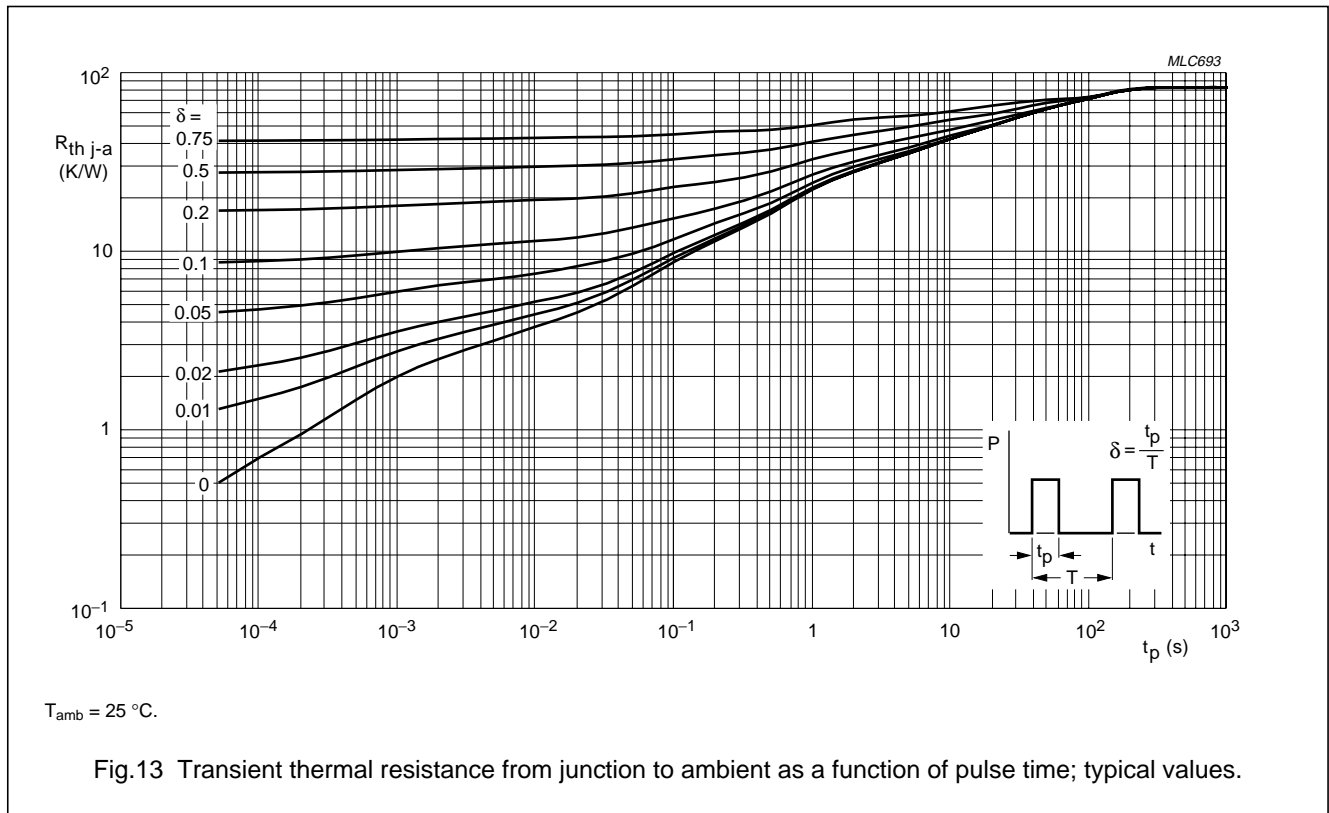


Fig.13 Transient thermal resistance from junction to ambient as a function of pulse time; typical values.



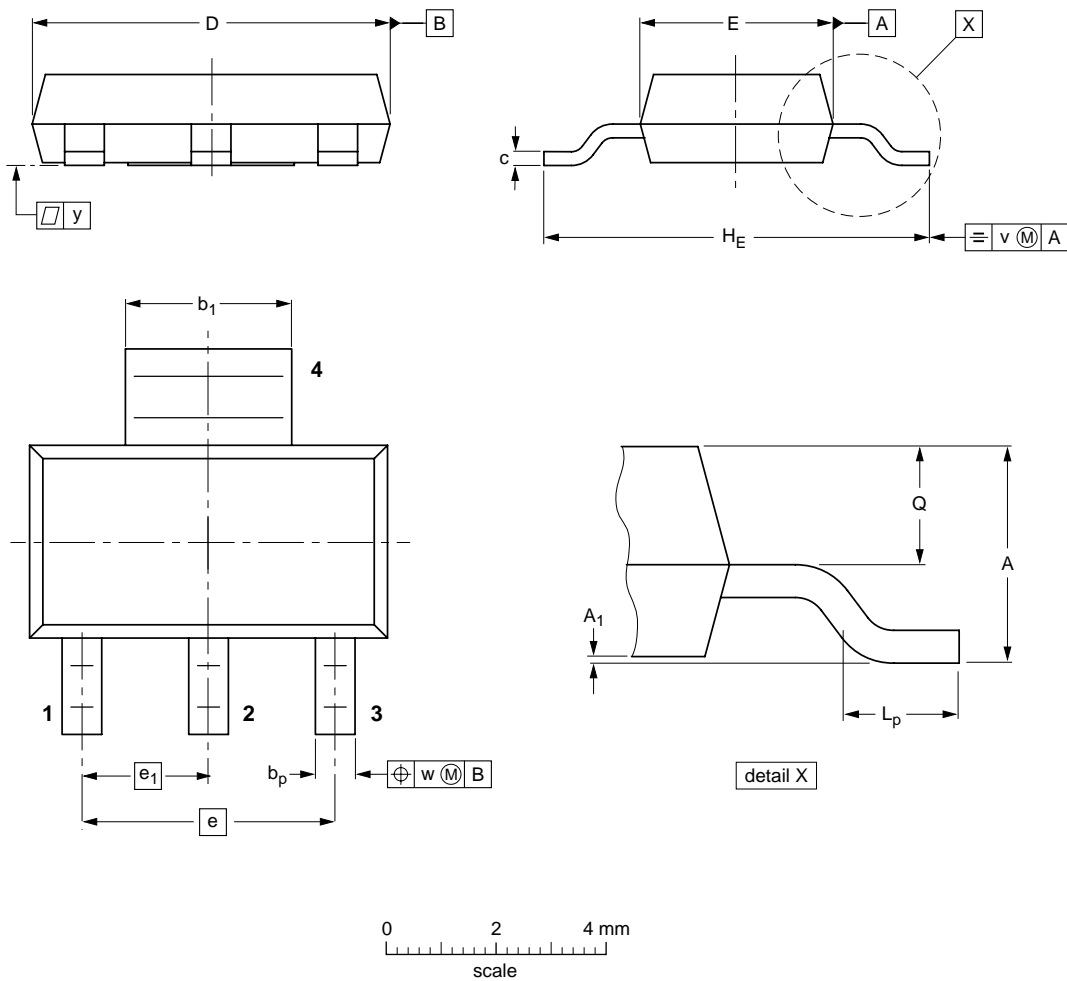
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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						96-11-11 97-02-28

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**BSP230****DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
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**NOTES**

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