Viking TechnologySingle-Channel RDRAM NexMod™ Specification

General Description

Viking VINRxxxETx0xCxx are high-density Direct Rambus NexMod™ Modules. The modules consist of up to eight, CMOS 16M x 18-bit Rambus DRAM in FBGA packages uniquely arranged in a PCB stacked module. The modules also include an EEPROM for Serial Presence Detect, VRM (voltage regulator module), DRCG (Direct Rambus Clock Generator), and end-of-channel termination. Decoupling capacitors are mounted on the circuit boards for each RDRAM. NexMod™ modules directly mount to motherboards using a BGA connection.

The NexMod™ product family addresses the needs of customers designing space-constrained systems. NexMod™ is a cost effective, small volumetric form factor solution that simplifies system layout and speeds time-to-market by providing virtually all the components needed for a complete Rambus channel.

Rambus Signaling Level (RSL) technology permits up to 1066 MHz transfer rates while using conventional system and board design technologies. RDRAM devices are capable of sustained data transfers at 938ps per two bytes (7.5ns per 16 bytes). The RDRAM architecture enables the highest sustained bandwidth for multiple, simultaneous, randomly addressed, memory transactions. The separate control and data buses with independent row and column control yield over 95% bus efficiency. The RDRAM's multi-bank architecture supports up to four simultaneous transactions per device.

Features

- NexMod and Rambus compatible:
  - Fully compatible with NexMod
  - Simplifies system layout
  - Faster time-to-market
- Stacked PCB module design:
  - Improves signal integrity and margin
  - Shortens Rambus channel length by stacking PCBs and placing DRCG, VRM, RDRAM VREF and termination networks on module
  - BGA connectors to mainboard provide mounting and prototype flexibility
  - BGA connector to mainboard utilizes tin/lead paste for RoHS 5 applications
  - BGA interposers within module
- 200 pin interconnect pattern with 0.50" (1.27mm) pitch
- Module footprint: 1.1 inches x 2.0 inches
- Serial Presence Detect (SPD) support
- Operates from a 2.5 volt supply (±5%)
- Low power and powerdown self-refresh modes
- I/O Freq up to 1066 Mhz, tRAC up to 32 ns
- Separate RAS and CAS buses for higher efficiency
- RoHS 5 Compliant* (see last page)

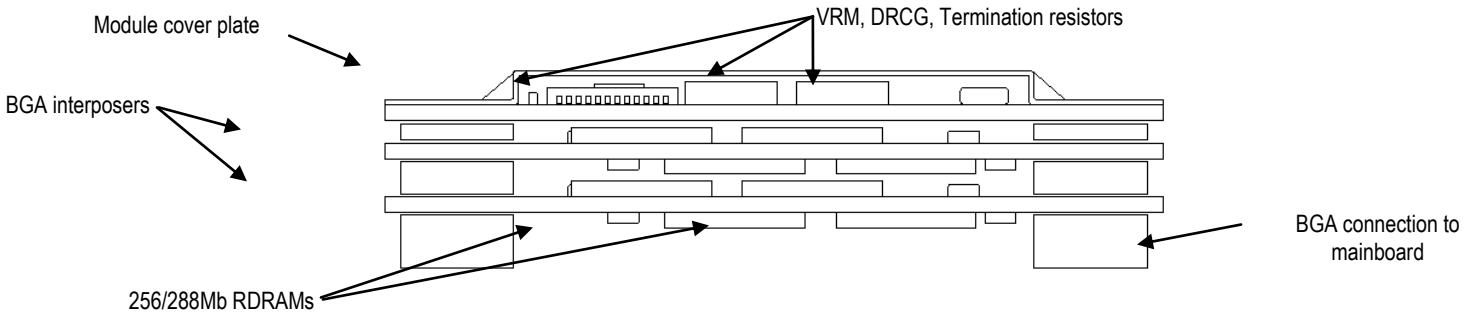
Related Documents

Data sheets for the Rambus memory system components, including the Rambus DRAMs, Rambus standards, and SORIMM connector are available on the Rambus web site at http://www.rambus.com.

Part Numbers by Configuration

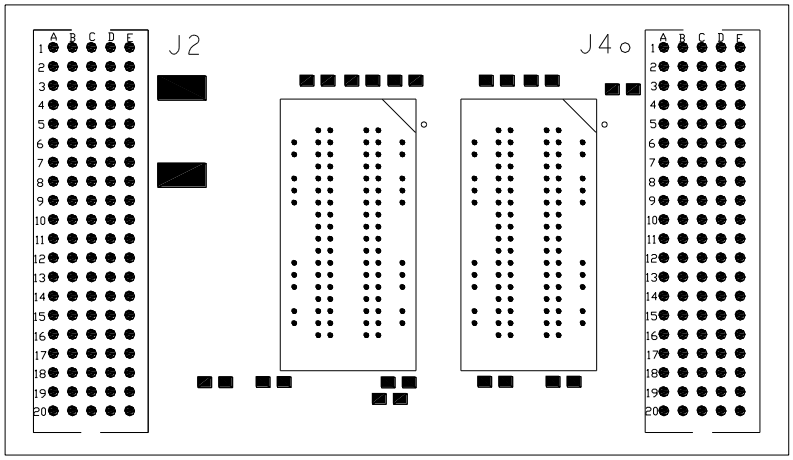
Part Number	Description	RDRAM Device	Module Speed	RDRAM die Rev.
VINR128ET004LCEB-C	144MB, ECC, BGA connector	Elpida EDR2518ABSE-AEP-E	1066MHz 32ns	B
VINR256ET008LCEB-C	288MB, ECC, BGA connector	Elpida EDR2518ABSE-AEP-E	1066MHz 32ns	B
VRNR512ET216LCEB	576MB, ECC, BGA connector	Elpida EDR2518ABSE-AEP-E	1066MHz 32ns	B

Module arrangement



Module Stack-up Diagram

Module Pad Number and Signal Names



Top View of NexMod Footprint, Indicating Pin Locations (Not in scale)

J2 Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	VDD	**B1**	VDD	**C1**	VCMOS	**D1**	VCMOS	**E1**	VCMOS
A2	VDD	**B2**	SCK	**C2**	GND	**D2**	DQA8	**E2**	GND
A3	VDD	**B3**	DQA6	**C3**	GND	**D3**	CMD	**E3**	VTERM*
A4	VDD	**B4**	DQA4	**C4**	GND	**D4**	DQA7	**E4**	VTERM*
A5	VDD	**B5**	DQA2	**C5**	GND	**D5**	DQA5	**E5**	VTERM*
A6	VDD	**B6**	DQA0	**C6**	GND	**D6**	DQA3	**E6**	GND
A7	GND	**B7**	CFM	**C7**	GND	**D7**	DQA1	**E7**	GND
A8	GND	**B8**	CFMN	**C8**	GND	**D8**	CTMN	**E8**	CTMN-DRCG*
A9	GND	**B9**	ROW1	**C9**	GND	**D9**	CTM	**E9**	CTM-DRCG*
A10	GND	**B10**	COL4	**C10**	GND	**D10**	ROW2	**E10**	GND
A11	GND	**B11**	COL2	**C11**	GND	**D11**	ROW0	**E11**	VREF
A12	GND	**B12**	COL0	**C12**	GND	**D12**	COL3	**E12**	VREF
A13	GND	**B13**	DQB0	**C13**	GND	**D13**	COL1	**E13**	GND
A14	VDD	**B14**	DQB2	**C14**	GND	**D14**	DQB1	**E14**	SIN
A15	VDD	**B15**	DQB4	**C15**	GND	**D15**	DQB3	**E15**	GND
A16	VDD	**B16**	DQB6	**C16**	GND	**D16**	DQB5	**E16**	GND
A17	SA0	**B17**	GND	**C17**	GND	**D17**	DQB7	**E17**	GND
A18	SA1	**B18**	REFCLK	**C18**	GND	**D18**	DQB8	**E18**	VDD3.3
A19	SA2	**B19**	SDA	**C19**	SWP	**D19**	GND	**E19**	VDD3.3
A20	PCLK/M	**B20**	GND	**C20**	SYNCLK/N	**D20**	SVDD	**E20**	SCL

*VTERM, CTMN-DRCG, and CTM DRCG pins are only used if internal VRM and DRCG options are not used on the NexMod.

Module Pad Number and Signal Names (cont'd)

J4 Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	VCMOS	**B1**	VCMOS	**C1**	VCMOS	**D1**	VDD	**E1**	VDD
A2	GND	**B2**	RESERVED*	**C2**	GND	**D2**	RESERVED*	**E2**	VDD
A3	VTERM	**B3**	RESERVED*	**C3**	GND	**D3**	RESERVED*	**E3**	VDD
A4	VTERM	**B4**	RESERVED*	**C4**	GND	**D4**	RESERVED*	**E4**	VDD
A5	VTERM	**B5**	RESERVED*	**C5**	GND	**D5**	RESERVED*	**E5**	VDD
A6	GND	**B6**	RESERVED*	**C6**	GND	**D6**	RESERVED*	**E6**	VDD
A7	GND	**B7**	RESERVED*	**C7**	GND	**D7**	RESERVED*	**E7**	GND
A8	GND	**B8**	RESERVED*	**C8**	GND	**D8**	RESERVED*	**E8**	GND
A9	GND	**B9**	RESERVED*	**C9**	GND	**D9**	RESERVED*	**E9**	GND
A10	GND	**B10**	RESERVED*	**C10**	GND	**D10**	RESERVED*	**E10**	GND
A11	VREF	**B11**	RESERVED*	**C11**	GND	**D11**	RESERVED*	**E11**	GND
A12	VREF	**B12**	RESERVED*	**C12**	GND	**D12**	RESERVED*	**E12**	GND
A13	GND	**B13**	RESERVED*	**C13**	GND	**D13**	RESERVED*	**E13**	GND
A14	RESERVED*	**B14**	RESERVED*	**C14**	GND	**D14**	RESERVED*	**E14**	GND
A15	GND	**B15**	RESERVED*	**C15**	GND	**D15**	RESERVED*	**E15**	VDD
A16	GND	**B16**	RESERVED*	**C16**	GND	**D16**	RESERVED*	**E16**	VDD
A17	GND	**B17**	RESERVED*	**C17**	GND	**D17**	GND	**E17**	VDD
A18	GND	**B18**	RESERVED*	**C18**	GND	**D18**	VDD	**E18**	VDD
A19	GND	**B19**	GND	**C19**	GND	**D19**	VDD	**E19**	VDD
A20	GND	**B20**	GND	**C20**	GND	**D20**	GND	**E20**	GND

*Reserved pins are used during module assembly at the factory. Do NOT connect in system layout.

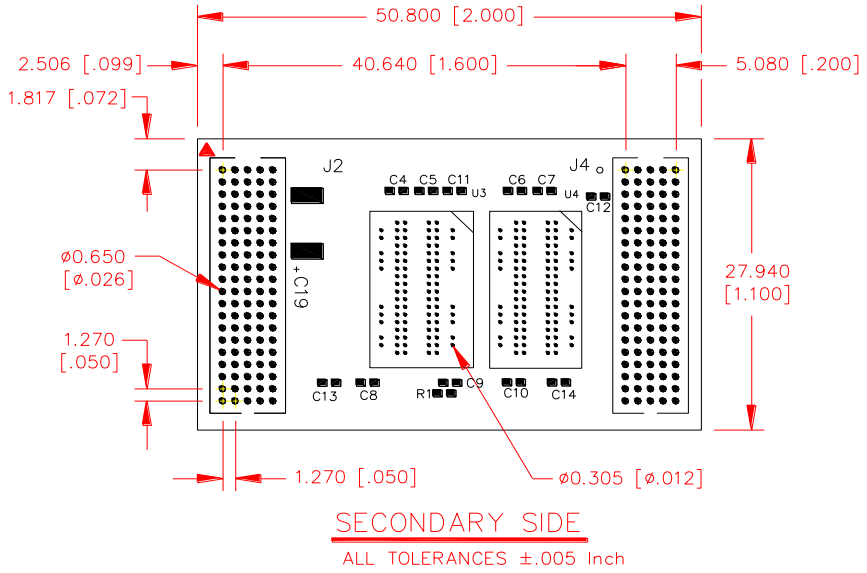
Module Connector Pad Description

Signal	I/O	Type	Description
GND			Ground reference for connector pads, RDRAM core, and interface.
CFM	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
CFMN	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
CMD	I	VCMOS	Serial Command used to read from and write to the control registers. Also used for power management.
COL4… COL0	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
CTM	0	RSL	Clock from on-board DRCG to Master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
CTMN	0	RSL	Clock from on-board DRCG to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
DQA8… DQA0	I/O	RSL	Data bus A. 9-bit bus carrying a byte of read or write data between the Channel and RDRAMs. DQA8 is not used on modules with x16 RDRAM devices.
DQB8… DQB0	I/O	RSL	Data bus B. 9-bit bus carrying a byte of read or write data between the Channel and RDRAMs. DQB8 is not used on modules with x16 RDRAM devices.
ROW2… ROW0	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.
SCK	I	VCMOS	Serial clock input. Clock source used to read from and write to the RDRAM control registers.
NC			Pads are not connected. Reserved for future use.

Module Connector Pad Description (cont'd)

Signal	I/O	Type	Description
SA0	I	SVDD	Serial Presence Detect Address 0.
SA1	I	SVDD	Serial Presence Detect Address 1.
SA2	I	SVDD	Serial Presence Detect Address 2.
SCL	I	SVDD	Serial Presence Detect Clock.
SDA	I/O	SVDD	Serial Presence Detect Data (Open Collector I/O).
SIN	I/O	VCMOS	Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module.
SVDD			SPD Voltage. Used for signals SCL, SDA, SWE, SA0, SA1 and SA2.
SWP	I	SVDD	Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.
PCLK/M		VDD3.3	Phase detector input (DRCG).
SYNCLK/N		VDD3.3	Phase detector input (DRCG).
REFCLK		VDD3.3	Reference clock (DRCG).
CTM-DRCG	I	RSL	Clock from external DRCG to master routed to last device in channel. Positive polarity.
CTMN-DRCG	I	RSL	Clock from external DRCG to master routed to last device in channel. Negative polarity.
VDD3.3			Supply voltage for DRCG
VCMOS			CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT.
VDD			Supply voltage for the RDRAM core and interface logic.
VREF			Logic threshold reference voltage for RSL signals.

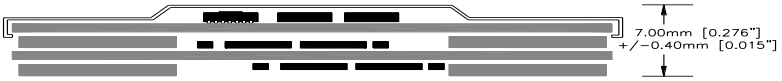
Physical Layout Dimensions



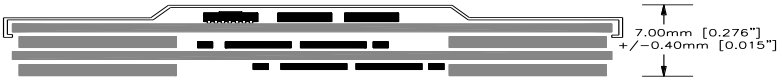
Top view layout dimensions (millimeters)

256MB NexMod with BGA connector vertical dimensions

Physical Layout Dimensions (cont'd)

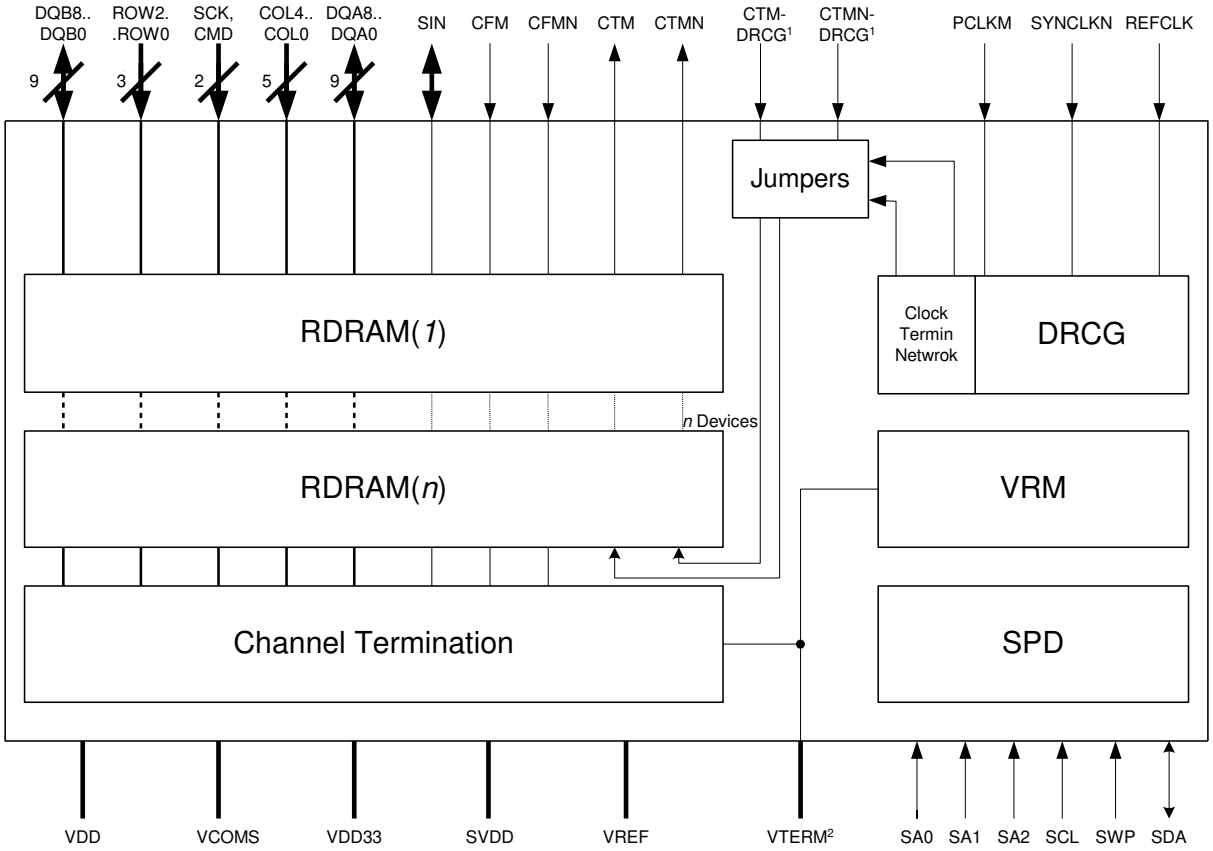


128MB NexMod with BGA connector vertical dimensions



64MB NexMod with BGA connector vertical dimensions

Functional Block Diagram



1. Used if internal DRCG not used (contact Viking for ordering options and application notes)
2. Used if internal VRM not used (contact Viking for ordering options and application notes)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage applied to any RSL or CMOS signal pad with respect to Gnd	V_{IABS}	-0.3 ~ V_{DD} + 0.3	V
Voltage on VDD with respect to Gnd	$V_{DD,ABS}$	-0.5 ~ V_{DD} + 1.0	V
Storage temperature	T_{STORE}	-50 ~ 100	°C
Operating junction temperature	T_{JMAX}	100	°C
Operating heat spreader surface temperature	TC_{MAX}	92	°C
Operating and storage humidity (non-condensing)	RH_{STORE}, RH_{OP}	95	%RH

Note: Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltages referenced to GND, TA = 0 to 70°C, VDD / VCMOS = 2.5 ± 0.13V)

Parameter and Conditions		Symbol	Min	Max	Unit
Supply voltage (Note 1)		V_{DD}	2.50 - 0.13	2.50 + 0.13	V
CMOS I/O power supply for 2.5V controllers (Note 2)		V_{CMOS}	V_{DD}	V_{DD}	V
CMOS I/O power supply for 1.8V controllers (Note 2)			1.80 - 0.1	1.80 + 0.2	
Reference voltage (Note 1)		V_{REF}	1.4 - 0.2	1.4 + 0.2	V
Serial Presence Detect- positive power supply		V_{SPD}	1.8	3.6	V
RSL input low voltage	800 MHz versions (A,B)	V_{DIL}	V_{REF} – 0.5	V_{REF} – 0.2	V
	1066 MHz versions (L)			V_{REF} – 0.15	
RSL input high voltage	800 MHz versions (A,B)	V_{DIH}	V_{REF} + 0.2	V_{REF} + 0.5	V
	1066 MHz versions (L)		V_{REF} + 0.15		
CMOS input low voltage (Note 3)		VIL, CMOS	-0.3	V_{CMOS} / 2 – 0.25	V
CMOS input high voltage (Note 4)		VIH, CMOS	V_{CMOS} / 2 + 0.25	V_{CMOS} + 0.3	V
CMOS output low voltage @ IOL = 1mA		VOL, CMOS	-	0.3	V
CMOS output high voltage @ IOH = -0.25mA		VOH, CMOS	V_{CMOS} – 0.3	-	V
Reference current @ V_{REF} max		IREF	-10xno.RDRAMs[6]	10xno.RDRAMs[6]	µA
RSL output low current (Note 5)	800 MHz versions (A,B)	I_{OL}		90.0	mA
	1066 MHz versions (L)			90.0	
RSL output high current @ (0<= VOUT <=Vdd)		IOH	-10	10	µA
CMOS input leakage current @ (0<= V_{CMOS} <=Vdd)		I_L, CMOS	-160	160	µA

Notes:
1. See Direct RDRAM component datasheet for more details
2. VCMOS must be present at all times Vdd is applied.
3. Undershoot is limited to –0.7V for a duration less than 5ns.
4. Overshoot is limited to VCMOS + 0.7V for a duration less than 5ns.
5. Devices in manual current control mode, i.e. all output device legs of one device are sinking current.
6. Number of RDRAM devices in a NexMod: 8 for 256/288MB; 4 for 128/144MB; 2 for 64/72MB

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted, TA = 0 to 70 °C)

Parameter	Symbol	Test Condition	Freq.	288MB	144MB	72MB	Unit	Note
				Max	Max	Max		
Read Current	$I_{DD}1$	One RDRAM in Read, balance in NAP mode	800	628	612	604	mA	1, 2
			1066	778	762	754		
Read Current	$I_{DD}2$	One RDRAM in Read, balance in Standby mode	800	1265	885	695	mA	1, 2
			1066	1485	1065	855		
Read Current	I_{DD} 3	One RDRAM in Read, balance in Active mode	800	1545	1005	735	mA	1, 2
			1066	1870	1230	910		
Write Current	I_{DD} 4	One RDRAM in Write, balance in NAP mode	800	608	592	584	mA	1, 2
			1066	768	752	74		
Write Current	I_{DD} 5	One RDRAM in Write, balance in Standby mode	800	1245	865	675	mA	1, 2
			1066	1475	1055	845		
Write Current	I_{DD} 6	One RDRAM in Write, balance in Active mode	800	1525	985	715	mA	1, 2
			1066	1860	1220	900		

Notes:

1. Actual power will depend on individual RDRAM component specifications, memory controller and usage patterns. Power does not include Refresh Current.
2. I/O current is a function of the number of bits=1. Add 290mA assuming 50% of data bits=1 and the following conditions: V_{DD} = 2.5V, V_{TERM} = 1.8V, V_{REF} = 1.4V and V_{DIL} = V REF - 0.5V.

AC ELECTRICAL SPECIFICATIONS

Symbol	Parameter and Conditions		Min	Typ	Max	Unit
Z_L	Module Impedance of RSL Signals		25.2	28	30.8	Ω
$Z_{UL-CMOS}$	Module Impedance of SCK and CMD signals		23.8	28	32.2	Ω
T_{PD}	Propagation Delay, all RSL signals		-	2.5	3.0	ns
ΔT_{PD}	Propagation delay variation of RSL signals with respect to $T_{PD\ a,b}$		-30		30	ps
$\Delta T_{PD\ -CMOS}$	Propagation delay variation of SCK signal with respect to an average clock delay ***a***		-250		250	ps
$\Delta T_{PD\ -SCK,CMD}$	Propagation delay variation of CMD signal with respect to SCK signal		-200		200	ps
$V_{\_}/V_{IN}$	Attenuation Limit	800MHz	-	-	27	%
		1066MHz	-	-	35	
V_{XF}/V_{IN}	Forward crosstalk coefficient (300ps input rise time @ 20%-80%)		-	10.0	12.0	%
V_{XB}/V_{IN}	Backward crosstalk coefficient (300ps input rise time @ 20%-80%)		-	2.0	4.0	%
R_{DC}	DC Resistance Limit		-	1.5	1.9	Ω

Notes:

1. TPD or Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN)
2. If the NexMod™ module meets the following specification, then it is compliant to the specification. If an actual NexMod™ module does not meet these specifications, the specification can be adjusted by using the "Adjusted ΔTPD Specification" table.

ADJUSTED ΔTpd SPECIFICATION

(Note 1)

Symbol	Parameter and Conditions	Adjusted Min/Max	Absolute Min / Max		Unit
ΔT_{PD}	Propagation delay variation of RSL signals with respect to TPD for 4 and 8 device modules	+/-[17+(18*N*ΔZ0)]	-30	30	ps

Notes:

1. Where: N = number of RDRAM devices installed on the NexMod™ module, ΔZ0 = delta Z0% = (max Z0 – min Z0)/(min Z0) Max Z0 and min Z0 are obtained from the loaded (high) impedance coupons of all RSL layers on the module

Viking NexMod™ Part Numbering Scheme

VR A B CCC D E F GG H I (J K) / (L M)

(Example: VRNR512ET016LCSE)

	Form Factor	Technology	Capacity	Correction	Data Termination	Connector	IC Qty	Module Speed	Temp	Chip Manufacturer & Die Revision	Customer Specific
	A	B	CCC	D	E	F	GG	H	I	JK	LM
VI = Viking Tin Lead	**N = NexMod TM**	**R = RAMBUS**	064 = 64MB	E = ECC	T = On board term	0 = BGA Interposer	02	A= 40ns/800MHz	C = Commercial	S = Samsung	As required
VR = Viking Lead Free			128 = 128Mb	N = Non ECC		2 = 2 PGA connectors	04	B = 45ns/800MHz	I = Industrial	E = Elpida	
			256 = 256MB				08	L = 32ns/1066MHz			
			512 = 512MB				**16**				

REVISION HISTORY

Revision	Release Date	Description of Change	Checked By (Full Name)
A	May 5, 2006	Release combined PS002028 and PS002029 under new family spec number	Brian Ouellette
B	June 8, 2006	Remove PGA part numbers	Brian Ouellette
C	February 13, 2007	Add AC part numbers to configuration table	Brian Ouellette
C1	September 4, 2007	Correct 244MB to 288MB on page 11	Brian Ouellette
C2	November 21, 2011	Update header and footer	Brian Ouellette
D	January 17, 2018	Revise logo and company address. Add 512MB and only VINR128ET004LCEB-C VINR256ET008LCEB-C VRNR512ET216LCEB	

STATEMENT OF COMPLIANCE

Viking Technology(tm), Sanmina-SCI Corporation ("Viking") shall use commercially reasonable efforts to provide components, parts, materials, products and processes to Customer that do not contain: (i) lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) above 0.1% by weight in homogeneous material or (ii) cadmium above 0.01% by weight of homogeneous material, except as provided in any exemption(s) from RoHS requirements (including the most current version of the "Annex" to Directive 2002/95/EC of 27 January, 2003), as codified in the specific laws of the EU member countries. Viking strives to obtain appropriate contractual protections from its suppliers in connection with the RoHS Directives.

All printed circuit boards (PCBs) have a flammability rating of UL94V-0.