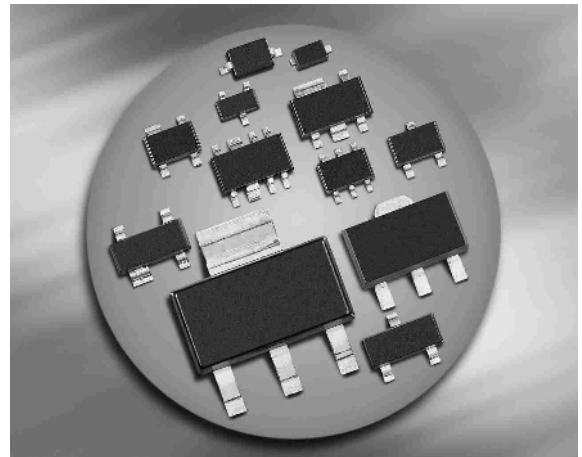


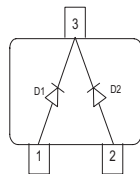
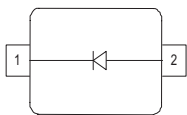
**Silicon Tuning Diode**

- High Q hyperabrupt tuning diode
- Designed for low tuning voltage operation
- For VCO's in mobile communications equipment
- Pb-free (RoHS compliant) package



**BBY51-02L**  
**BBY51-02V**  
**BBY51-02W**  
**BBY51-03W**

**BBY51**



Type	Package	Configuration	Marking
BBY51	SOT23	common cathode	S3s
BBY51-02L	TSLP-2-1	single, leadless	ll
BBY51-02V	SC79	single	f
BBY51-02W*	SCD80	single	ll
BBY51-03W	SOD323	single	white H

\* Not for new design

**Maximum Ratings at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

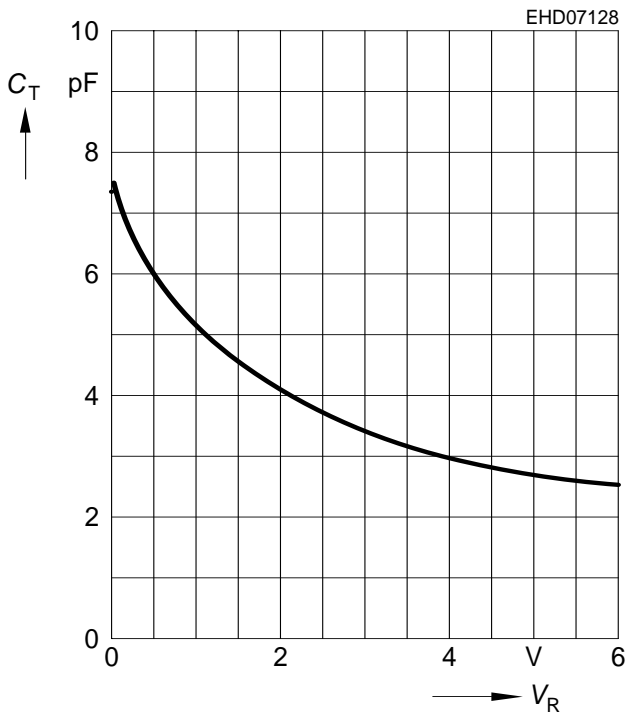
Parameter	Symbol	Value	Unit
Diode reverse voltage	$V_R$	7	V
Forward current	$I_F$	20	mA
Operating temperature range	$T_{op}$	-55 ... 125	°C
Storage temperature	$T_{stg}$	-55 ... 150	

**Electrical Characteristics at  $T_A = 25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>DC Characteristics</b>					
Reverse current $V_R = 6\text{ V}$ $V_R = 6\text{ V}, T_A = 85\text{ °C}$	$I_R$	-	-	10 200	nA
<b>AC Characteristics</b>					
Diode capacitance $V_R = 1\text{ V}, f = 1\text{ MHz}$ $V_R = 2\text{ V}, f = 1\text{ MHz}$ $V_R = 3\text{ V}, f = 1\text{ MHz}$ $V_R = 4\text{ V}, f = 1\text{ MHz}$	$C_T$	5.05 3.4 2.7 2.5	5.4 4.2 3.5 3.1	5.75 5.2 4.6 3.7	pF
Capacitance ratio $V_R = 1\text{ V}, V_R = 4\text{ V}, f = 1\text{ MHz}$	$C_{T1}/C_{T4}$	1.55	1.75	2.2	
Capacitance difference $V_R = 1\text{ V}, V_R = 3\text{ V}, f = 1\text{ MHz}$	$C_{1V}-C_{3V}$	1.4	1.78	2.2	pF
Capacitance difference $V_R = 3\text{ V}, V_R = 4\text{ V}, f = 1\text{ MHz}$	$C_{3V}-C_{4V}$	0.3	0.5	0.7	
Series resistance $V_R = 1\text{ V}, f = 1\text{ GHz}$	$r_S$	-	0.37	-	$\Omega$

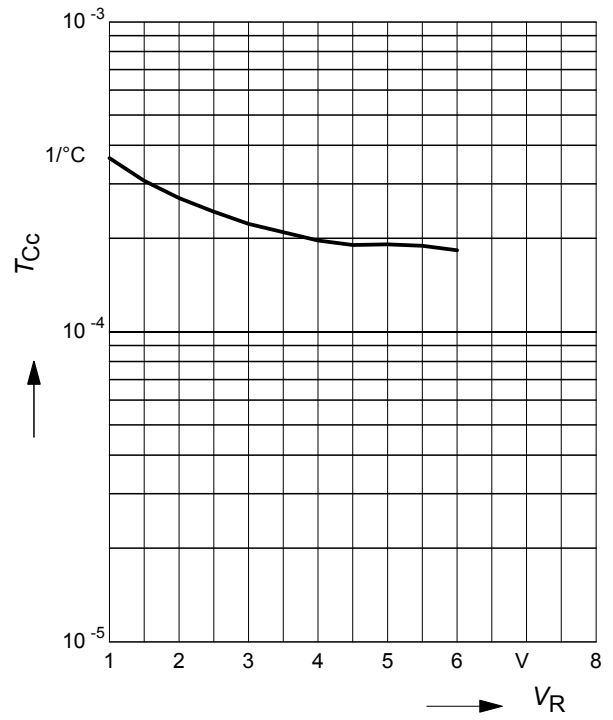
Diode capacitance  $C_T = f(V_R)$

$f = 1\text{MHz}$

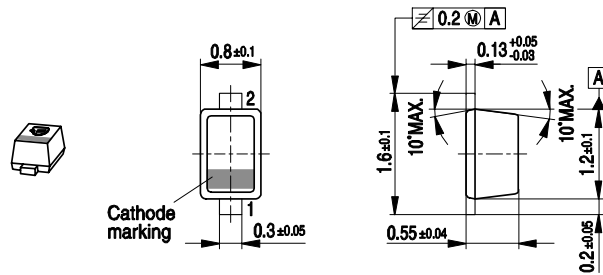


Temperature coefficient of the diode

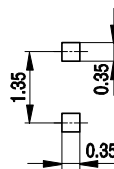
capacitance  $T_{Cc} = f(V_R)$



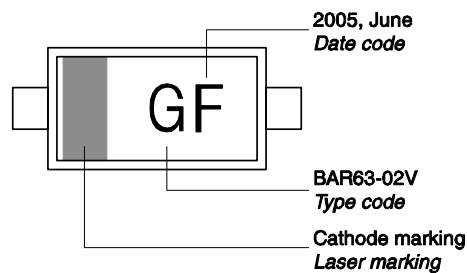
### Package Outline



### Foot Print

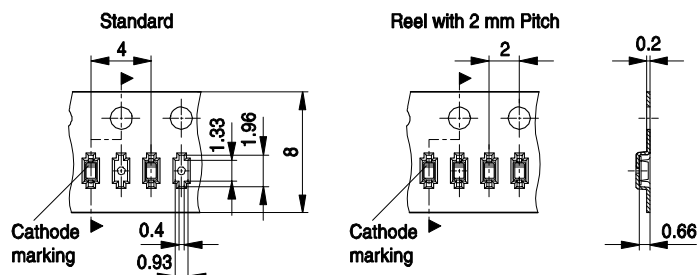


### Marking Layout (Example)

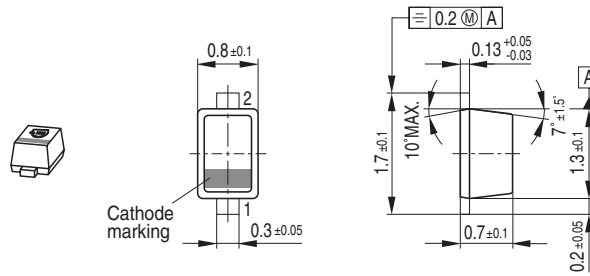


### Standard Packing

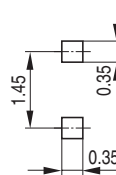
- Reel  $\varnothing$ 180 mm = 3.000 Pieces/Reel
- Reel  $\varnothing$ 180 mm = 8.000 Pieces/Reel (2 mm Pitch)
- Reel  $\varnothing$ 330 mm = 10.000 Pieces/Reel



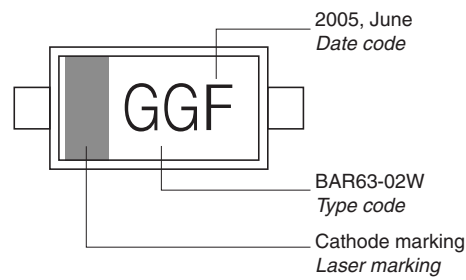
Package Outline



Foot Print

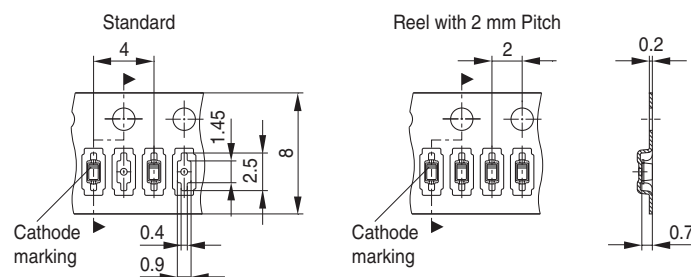


Marking Layout (Example)



Standard Packing

Reel  $\varnothing$ 180 mm = 3.000 Pieces/Reel  
 Reel  $\varnothing$ 180 mm = 8.000 Pieces/Reel (2 mm Pitch)  
 Reel  $\varnothing$ 330 mm = 10.000 Pieces/Reel

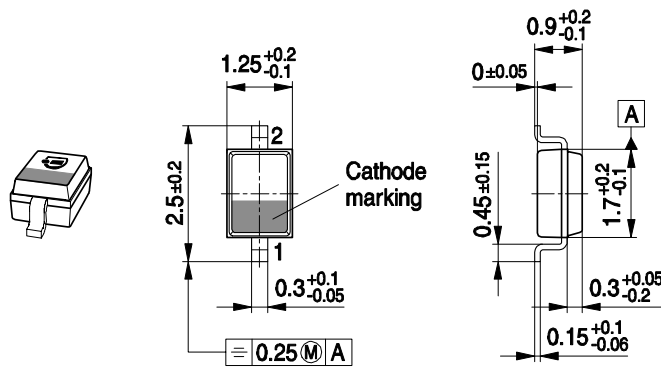


Date Code marking for discrete packages with one digit (SCD80, SC79, SC75<sup>1)</sup>) CES-Code

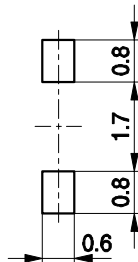
Month	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
01	a	p	A	P	a	p	A	P	a	p	A	P
02	b	q	B	Q	b	q	B	Q	b	q	B	Q
03	c	r	C	R	c	r	C	R	c	r	C	R
04	d	s	D	S	d	s	D	S	d	s	D	S
05	e	t	E	T	e	t	E	T	e	t	E	T
06	f	u	F	U	f	u	F	U	f	u	F	U
07	g	v	G	V	g	v	G	V	g	v	G	V
08	h	x	H	X	h	x	H	X	h	x	H	X
09	j	y	J	Y	j	y	J	Y	j	y	J	Y
10	k	z	K	Z	k	z	K	Z	k	z	K	Z
11	l	2	L	4	l	2	L	4	l	2	L	4
12	n	3	N	5	n	3	N	5	n	3	N	5

1) New Marking Layout for SC75, implemented at October 2005.

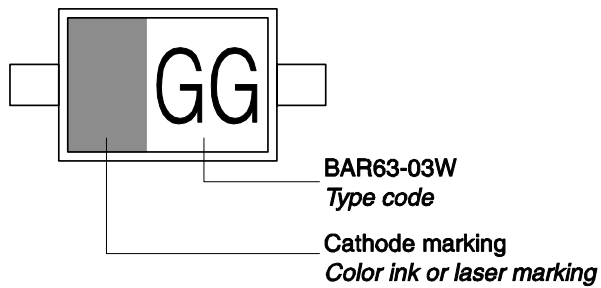
### Package Outline



### Foot Print

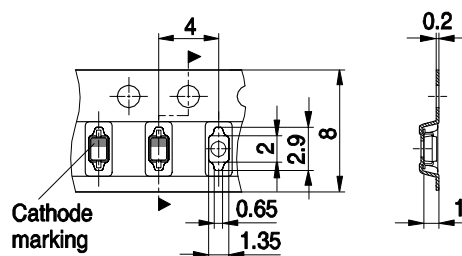


### Marking Layout (Example)

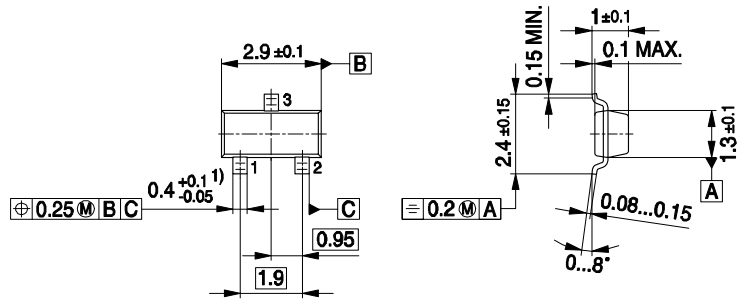


### Standard Packing

Reel  $\varnothing$ 180 mm = 3.000 Pieces/Reel  
 Reel  $\varnothing$ 330 mm = 10.000 Pieces/Reel



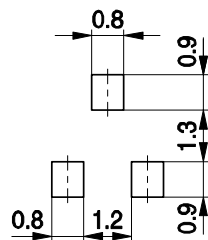
Package Outline



1) Lead width can be 0.6 max. in dambar area

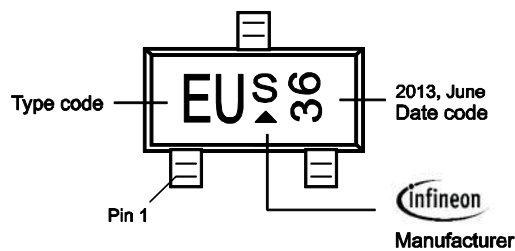
SOT23-PO V08

Foot Print



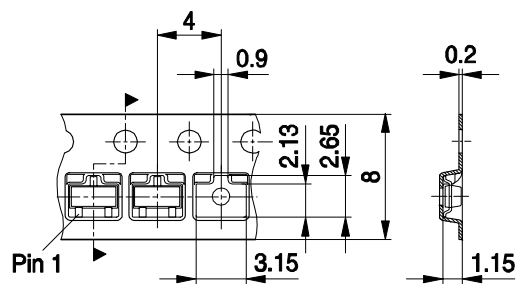
SOT23-FPR V08

Marking Layout



Standard Packing

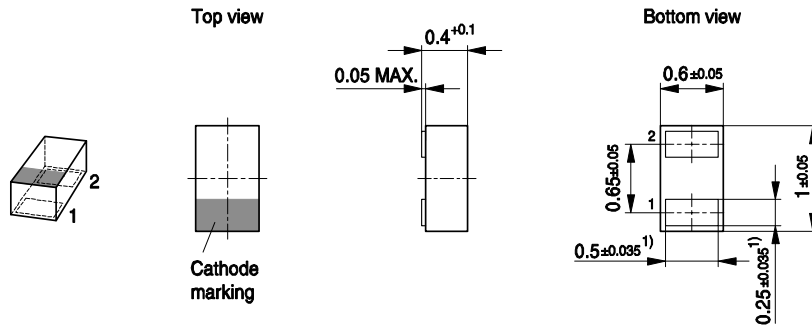
Reel o 180 mm: 3.000 Pieces / Reel  
 Reel o 330 mm = 10.000 Pieces / Reel



SOT23-TP V02



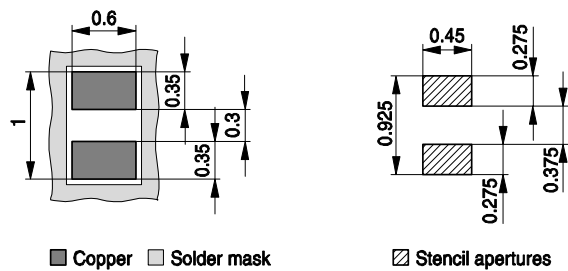
### Package Outline



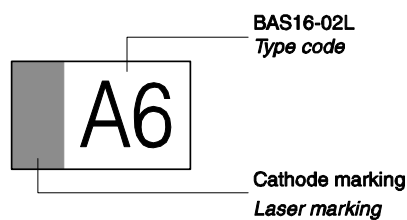
1) Dimension applies to plated terminal

### Foot Print

For board assembly information please refer to Infineon website "Packages"

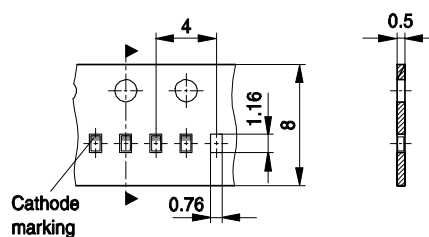


### Marking Layout (Example)



### Standard Packing

Reel  $\varnothing$ 180 mm = 15.000 Pieces/Reel  
 Reel  $\varnothing$ 330 mm = 50.000 Pieces/Reel (optional)



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