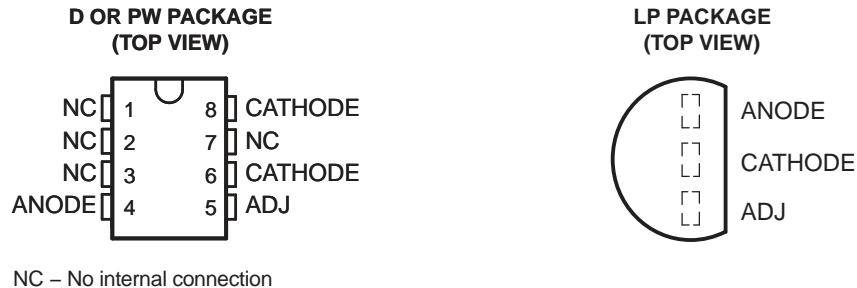


2.5-V INTEGRATED REFERENCE CIRCUIT

FEATURES

- Excellent Temperature Stability
- Initial Tolerance: 0.2% Max
- Dynamic Impedance: 0.6 Ω Max
- Wide Operating Current Range
- Directly Interchangeable With LM136
- Needs No Adjustment for Minimum Temperature Coefficient



DESCRIPTION/ORDERING INFORMATION

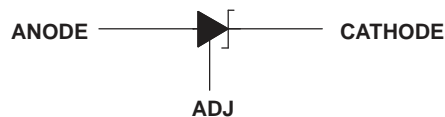
The LT1009 reference circuit is a precision-trimmed 2.5-V shunt regulator featuring low dynamic impedance and a wide operating current range. The maximum initial tolerance is ± 5 mV in the LP package and ± 10 mV in the D and PW packages. The reference tolerance is achieved by on-chip trimming, which minimizes the initial voltage tolerance and the temperature coefficient, α_{VZ} .

Although the LT1009 needs no adjustments, a third terminal (ADJ) allows the reference voltage to be adjusted $\pm 5\%$ to eliminate system errors. In many applications, the LT1009 can be used as a terminal-for-terminal replacement for the LM136-2.5, which eliminates the external trim network.

The LT1009 uses include 5-V system references, 8-bit analog-to-digital converter (ADC) and digital-to-analog converter (DAC) references, and power-supply monitors. The device also can be used in applications such as digital voltmeters and current-loop measurement and control systems.

The LT1009C is characterized for operation from 0°C to 70°C. The LT1009I is characterized for operation from –40°C to 85°C.

SYMBOL



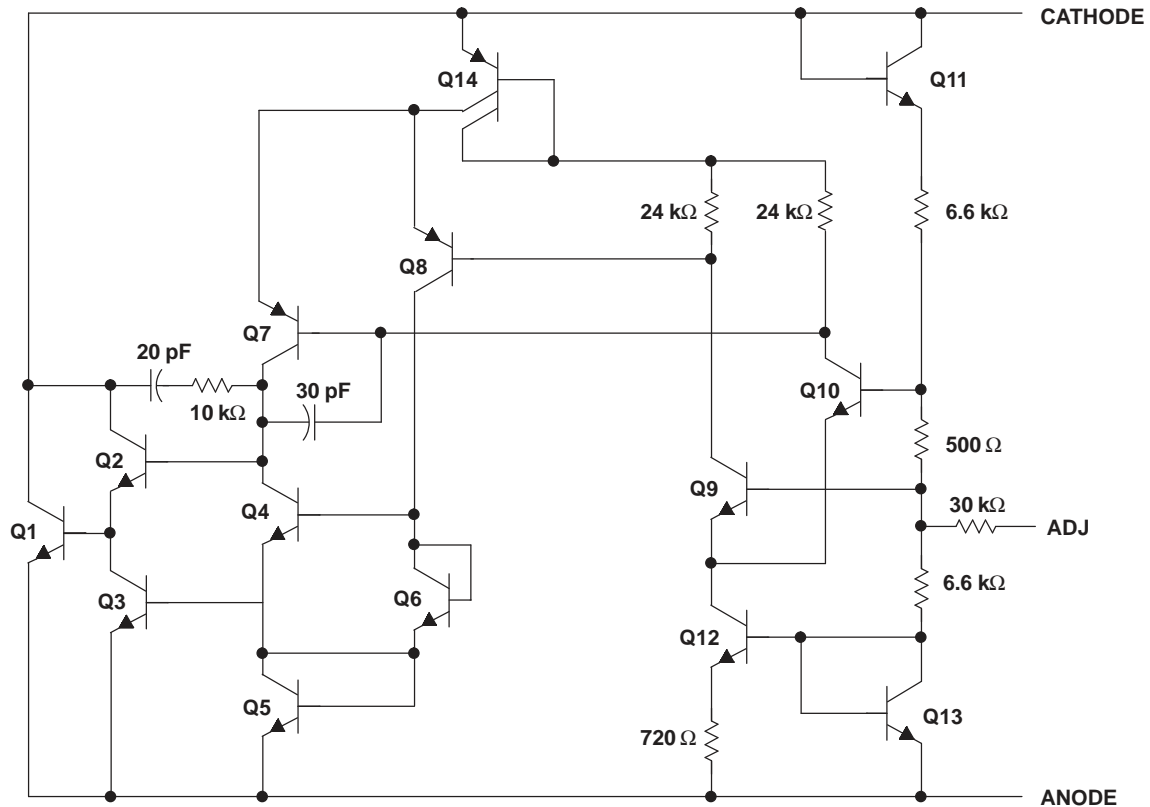
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION⁽¹⁾

| T _A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| 0°C to 70°C | SOIC – D | Tube of 75 | LT1009CD | 1009C |
| | | Reel of 2500 | LT1009CDR | |
| | TO-226/TO-92 – LP | Bulk of 1000 | LT1009CLP | LT1009C |
| | | Ammo of 2000 | LT1009CLPM | |
| | | Reel of 2000 | LT1009CLPR | |
| | TSSOP – PW | Tube of 150 | LT1009CPW | 1009C |
| Reel of 2000 | | LT1009CPWR | | |
| –40°C to 85°C | SOIC – D | Tube of 75 | LT1009ID | 1009I |
| | | Reel of 2500 | LT1009IDR | |
| | TO-226/TO-92 – LP | Bulk of 1000 | LT1009ILP | LT1009I |
| | | Ammo of 2000 | LT1009ILPM | |
| | | Reel of 2000 | LT1009ILPR | |
| | TSSOP – PW | Tube of 150 | LT1009IPW | 1009I |
| | | Reel of 2000 | LT1009IPWR | |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

SCHEMATIC



NOTE: All component values shown are nominal.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|---------------------------------------------|------------|-----|------|
| I_R | Reverse current | | 20 | mA |
| I_F | Forward current | | 10 | mA |
| θ_{JA} | Package thermal impedance ⁽²⁾⁽³⁾ | D package | 97 | °C/W |
| | | LP package | 140 | |
| | | PW package | 149 | |
| T_J | Operating virtual junction temperature | | 150 | °C |
| T_{stg} | Storage temperature range | –65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT |
|-------|--------------------------------------|---------|-----|------|
| T_A | Operating free-air temperature range | LT1009C | 0 | 70 |
| | | LT1009I | –40 | 85 |

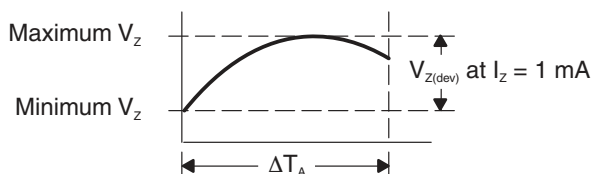
ELECTRICAL CHARACTERISTICS

at specified free-air temperature

| PARAMETER | TEST CONDITIONS | T _A ⁽¹⁾ | LT1009C | | | LT1009I | | | UNIT | | | | |
|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------|-------------------------------|--------------|-----|-------|---------|-------|-------|---------|-------|--------|-------|--|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | | | | | |
| V _Z Reference voltage | I _Z = 1 mA | 25°C | D/PW package | | 2.49 | 2.5 | 2.51 | 2.49 | 2.5 | 2.51 | V | | |
| | | | LP package | | 2.495 | 2.5 | 2.505 | 2.495 | 2.5 | 2.505 | | | |
| | | Full range | D/PW package | | 2.485 | | 2.515 | | 2.475 | | | 2.525 | |
| | | | LP package | | 2.491 | | 2.509 | | 2.48 | | | 2.52 | |
| V _F Forward voltage | I _F = 2 mA | 25°C | 0.4 | | 1 | | 0.4 | | 1 | | V | | |
| Adjustment range | I _Z = 1 mA, V _{ADJ} = GND to V _Z | 25°C | 125 | | 125 | | 125 | | 125 | | mV | | |
| | I _Z = 1 mA, V _{ADJ} = 0.6 V to V _Z - 0.6 V | | 45 | | 45 | | 45 | | 45 | | | | |
| ΔV _{Z(temp)} Change in reference voltage with temperature | D/PW package | | Full range | | | 5 | | 15 | | mV | | | |
| | LP package | | Full range | | | 4 | | 15 | | | | | |
| αV _Z Average temperature coefficient of reference voltage ⁽²⁾ | I _Z = 1 mA, V _{ADJ} = open | 0°C to 70°C | 15 | | 25 | | 15 | | 25 | | ppm/°C | | |
| | | -40°C to 85°C | | | | | 20 | | 35 | | | | |
| ΔV _Z Change in reference voltage with current | I _Z = 400 μA to 10 mA | 25°C | 2.6 | | 10 | | 2.6 | | 6 | | mV | | |
| | | Full range | | | 12 | | | | 10 | | | | |
| ΔV _Z /Δt Long-term change in reference voltage | I _Z = 1 mA | 25°C | 20 | | 20 | | 20 | | ppm/khr | | | | |
| Z _Z Reference impedance | I _Z = 1 mA | 25°C | 0.3 | | 1 | | 0.3 | | 1 | | Ω | | |
| | | Full range | | | 1.4 | | | | 1.4 | | | | |

- (1) Full range is 0°C to 70°C for the LT1009C and -40°C to 85°C for the LT1009I.
- (2) The deviation parameter V_{Z(dev)} is defined as the difference between the maximum and minimum values obtained over the recommended operating temperature range, measured at I_Z = 1 mA. The average full-range temperature coefficient of the reference voltage (αV_Z) is defined as:

$$|\alpha V_Z| \left(\frac{\text{ppm}}{^\circ\text{C}} \right) = \frac{\left(\frac{V_{Z(\text{dev})}}{V_Z \text{ at } 25^\circ\text{C}} \right) \times 10^6}{\Delta T_A}$$



αV_Z can be positive or negative, depending upon whether the minimum V_Z or maximum V_Z, respectively, occurs at the lower temperature.

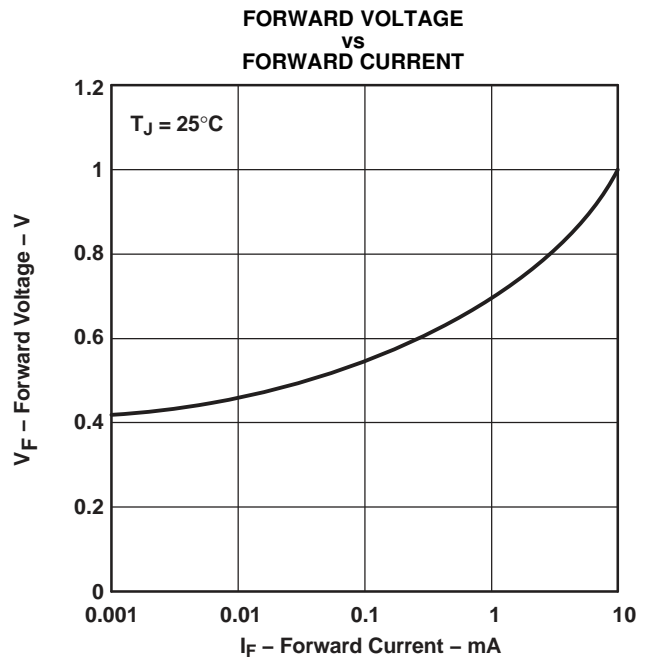
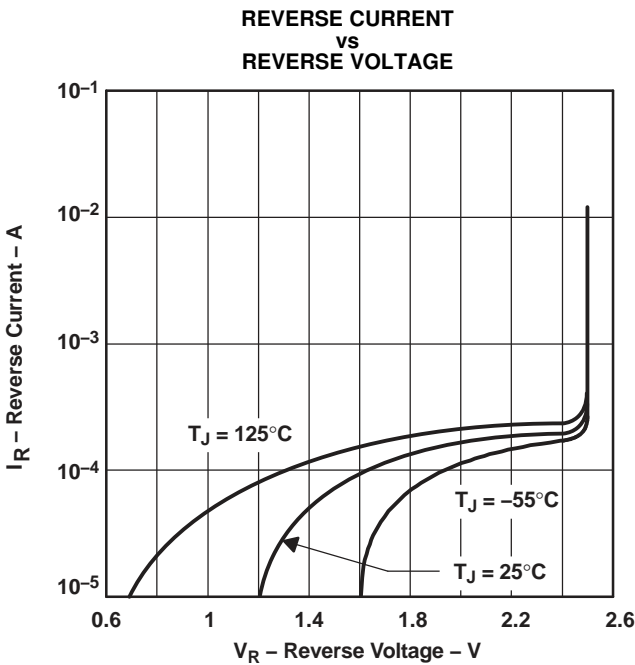
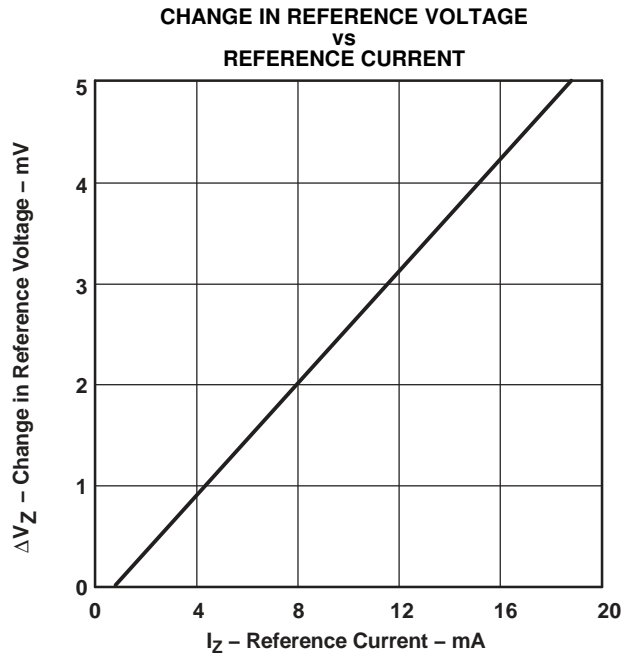
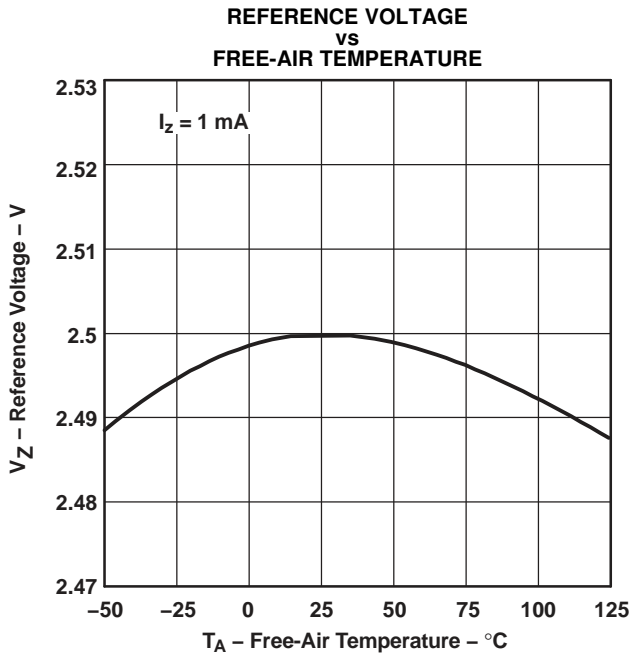
For example, at I_Z = 1 mA, maximum V_Z = 2501 mV at 30°C, minimum V_Z = 2497 mV at 0°C, V_Z = 2500 mV at 25°C, ΔT_A = 70°C for LT1009C:

$$|\alpha V_Z| = \frac{\left(\frac{4 \text{ mV}}{2500 \text{ mV}} \right) \times 10^6}{70^\circ\text{C}} \approx 23 \frac{\text{ppm}}{^\circ\text{C}}$$

Because minimum V_Z occurs at the lower temperature, the coefficient in this example is positive.

TYPICAL CHARACTERISTICS

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS (continued)

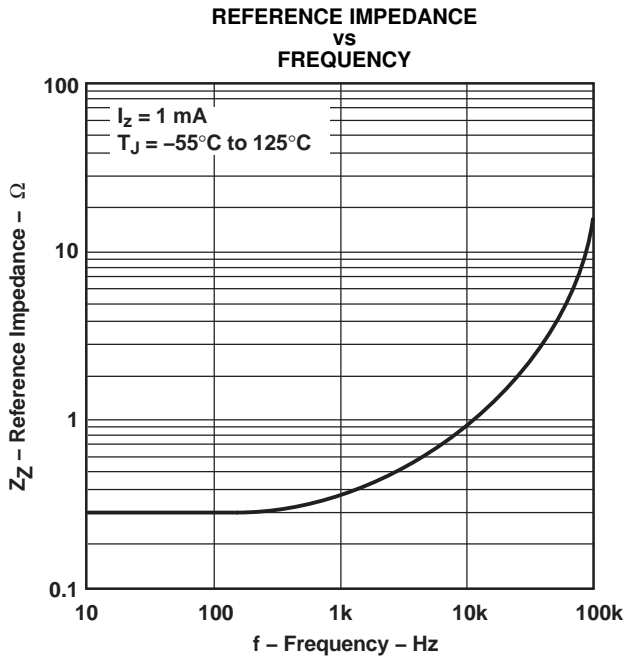


Figure 5.

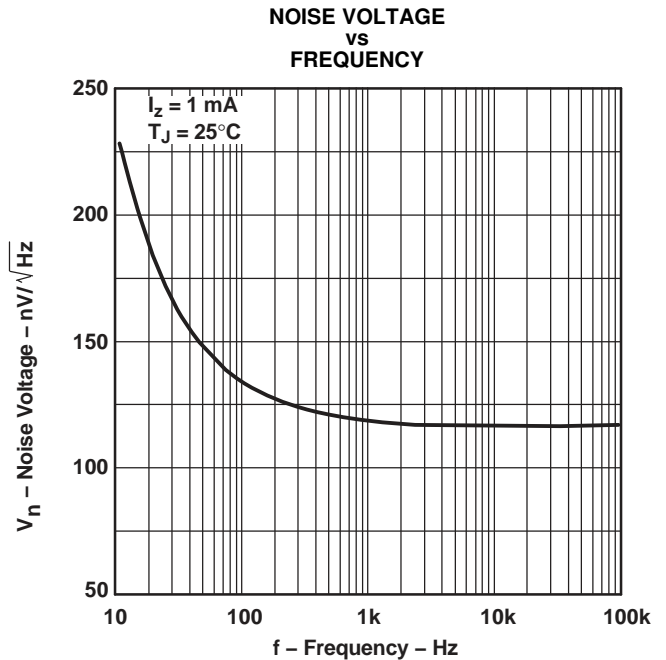


Figure 6.

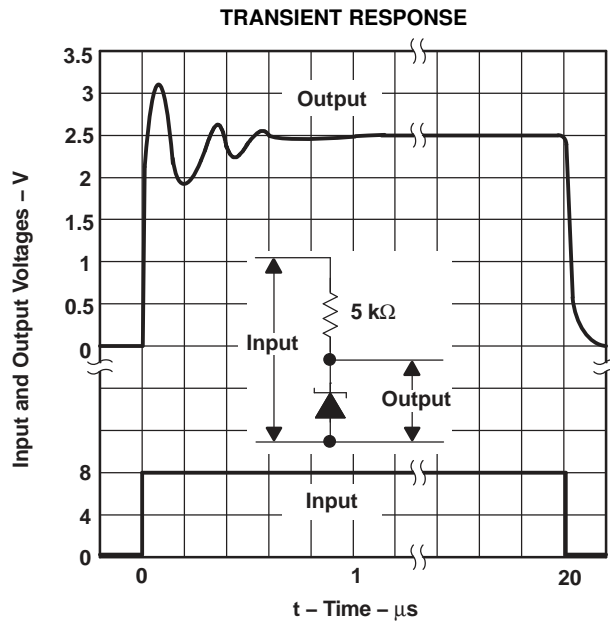
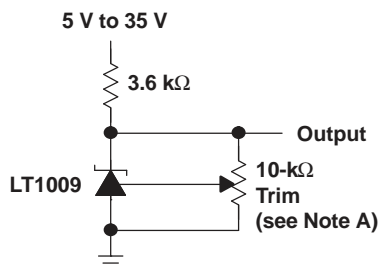


Figure 7.

APPLICATION INFORMATION



A. This does not affect temperature coefficient. It provides $\pm 5\%$ trim range.

Figure 8. 2.5-V Reference

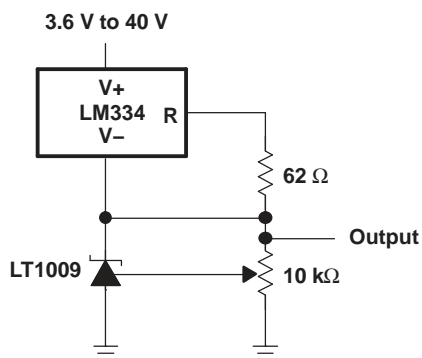


Figure 9. Adjustable Reference With Wide Supply Range

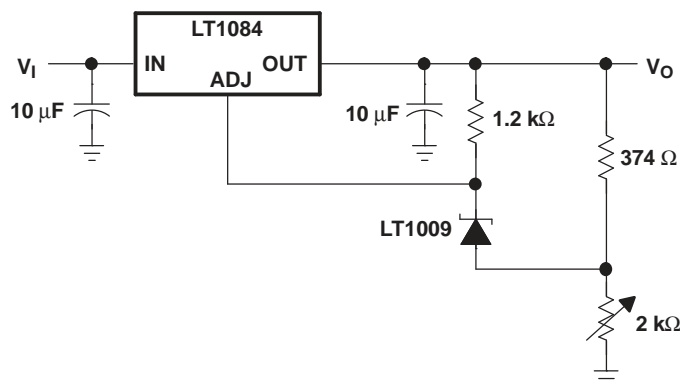


Figure 10. Power Regulator With Low Temperature Coefficient

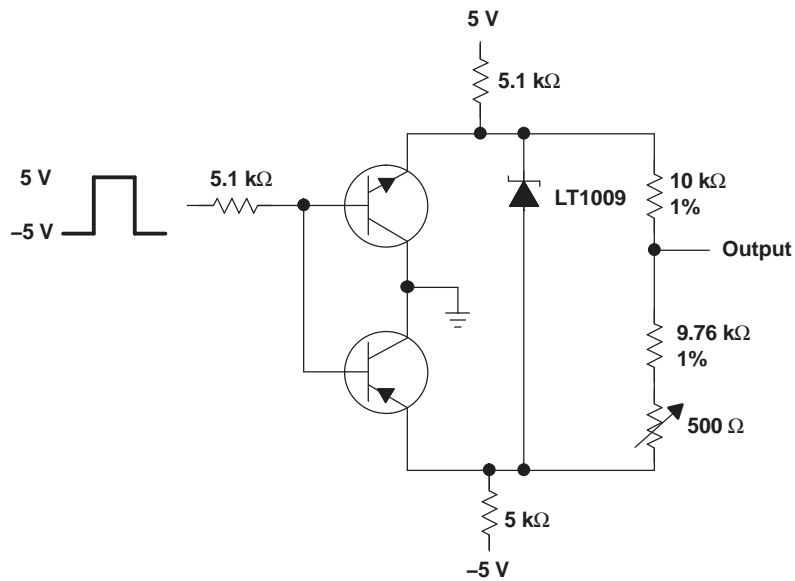


Figure 11. Switchable $\pm 1.25\text{-V}$ Bipolar Reference

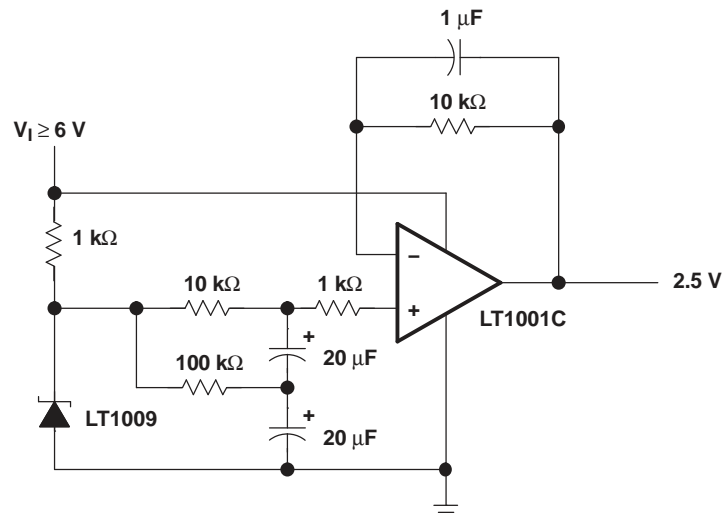


Figure 12. Low-Noise 2.5-V Buffered Reference

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| LT1009CD | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 1009C | Samples |
| LT1009CDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 1009C | Samples |
| LT1009CDRG4 | LIFEBUY | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 1009C | |
| LT1009CLP | ACTIVE | TO-92 | LP | 3 | 1000 | RoHS & Green | SN | N / A for Pkg Type | 0 to 70 | LT1009C | Samples |
| LT1009CLPE3 | LIFEBUY | TO-92 | LP | 3 | 1000 | RoHS & Green | SN | N / A for Pkg Type | 0 to 70 | LT1009C | |
| LT1009CLPM | ACTIVE | TO-92 | LP | 3 | 2000 | RoHS & Green | SN | N / A for Pkg Type | 0 to 70 | LT1009C | Samples |
| LT1009CLPR | ACTIVE | TO-92 | LP | 3 | 2000 | RoHS & Green | SN | N / A for Pkg Type | 0 to 70 | LT1009C | Samples |
| LT1009CPWR | ACTIVE | TSSOP | PW | 8 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 1009C | Samples |
| LT1009ID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 1009I | Samples |
| LT1009IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 1009I | Samples |
| LT1009ILP | ACTIVE | TO-92 | LP | 3 | 1000 | RoHS & Green | SN | N / A for Pkg Type | -40 to 85 | LT1009I | Samples |
| LT1009ILPR | ACTIVE | TO-92 | LP | 3 | 2000 | RoHS & Green | SN | N / A for Pkg Type | -40 to 85 | LT1009I | Samples |
| LT1009ILPRE3 | LIFEBUY | TO-92 | LP | 3 | 2000 | RoHS & Green | SN | N / A for Pkg Type | -40 to 85 | LT1009I | |
| LT1009IPWR | ACTIVE | TSSOP | PW | 8 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 1009I | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LT1009 :

- Military : [LT1009M](#)

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

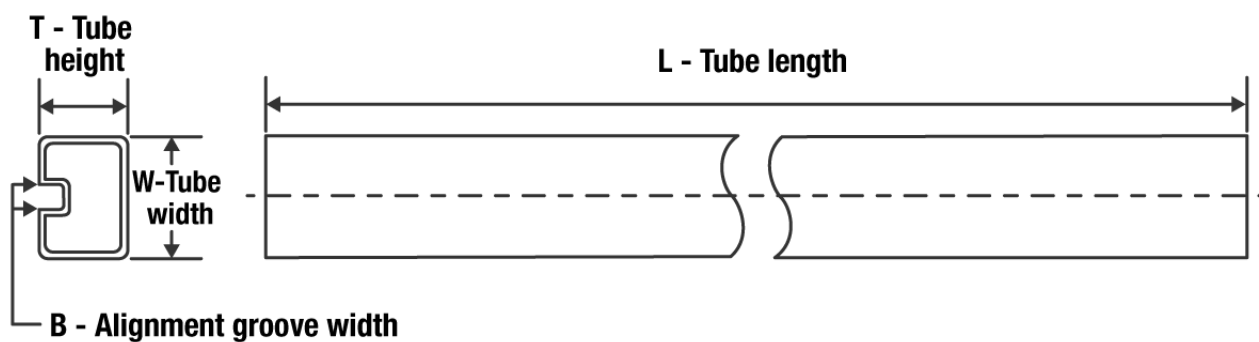

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LT1009CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| LT1009CPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| LT1009IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| LT1009IPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LT1009CDR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| LT1009CPWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |
| LT1009IDR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| LT1009IPWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------|--------------|--------------|------|-----|--------|--------|--------|--------|
| LT1009CD | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| LT1009ID | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

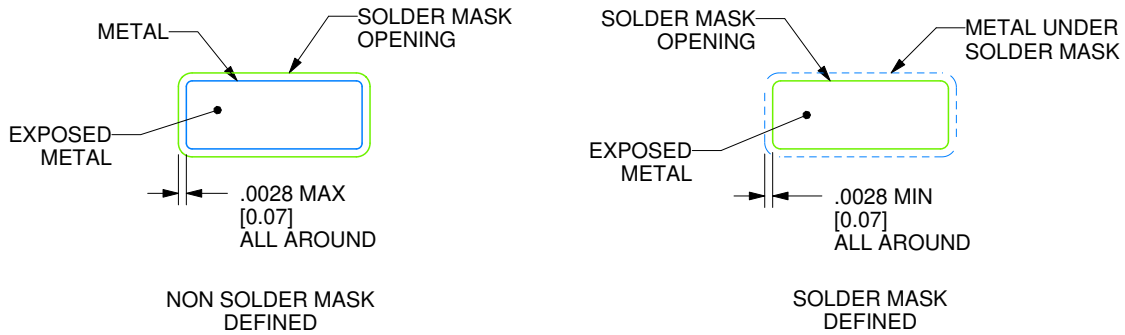
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

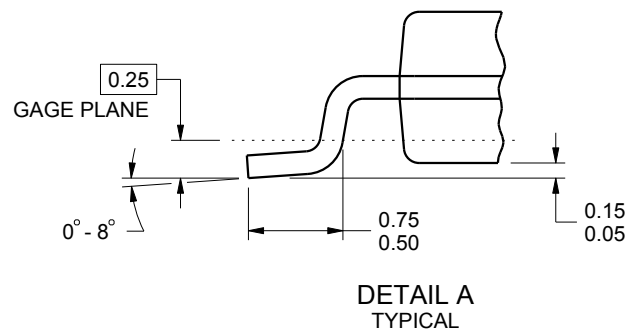
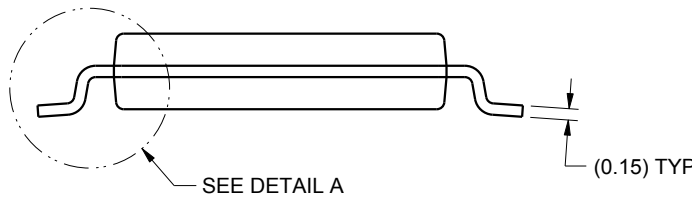
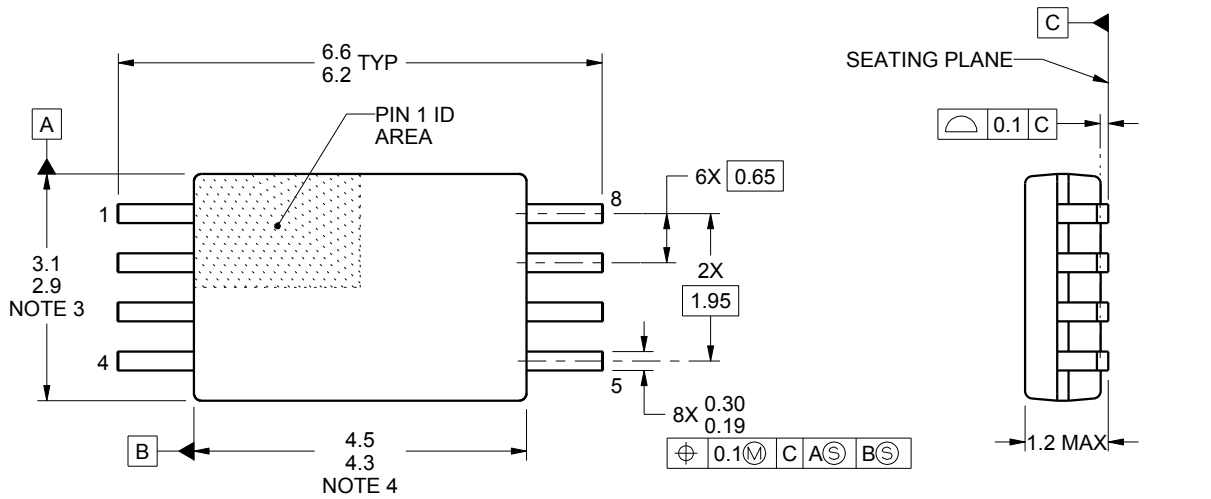
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

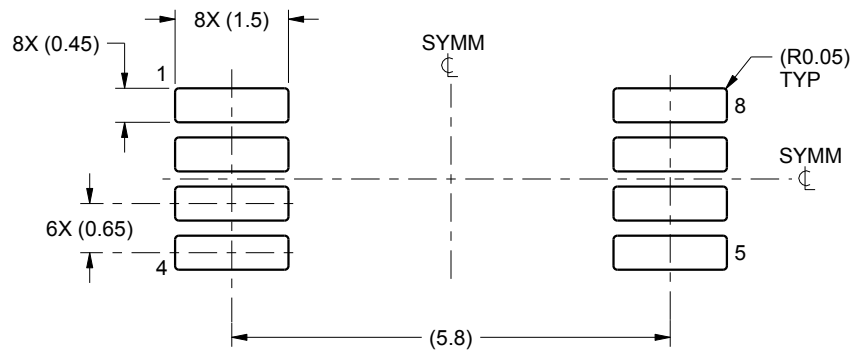
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

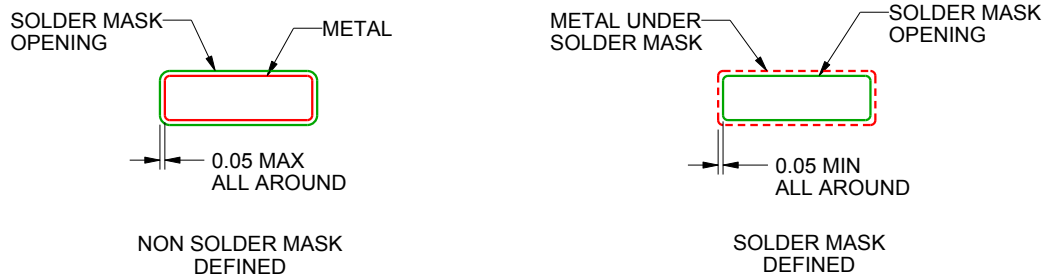
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

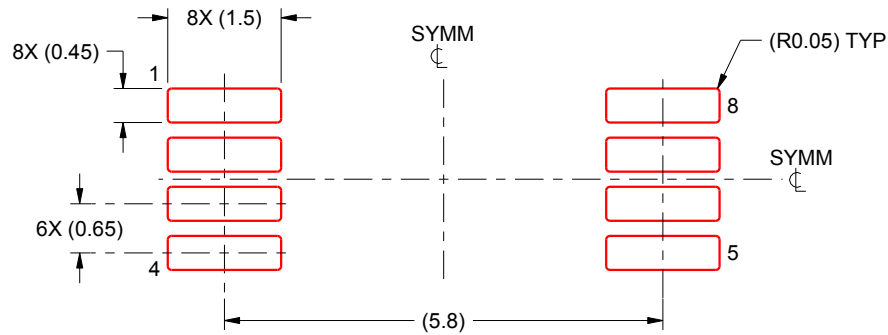
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

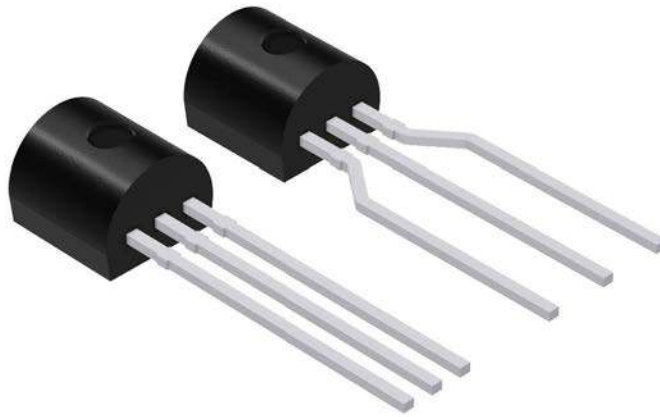
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

LP 3

TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040001-2/F

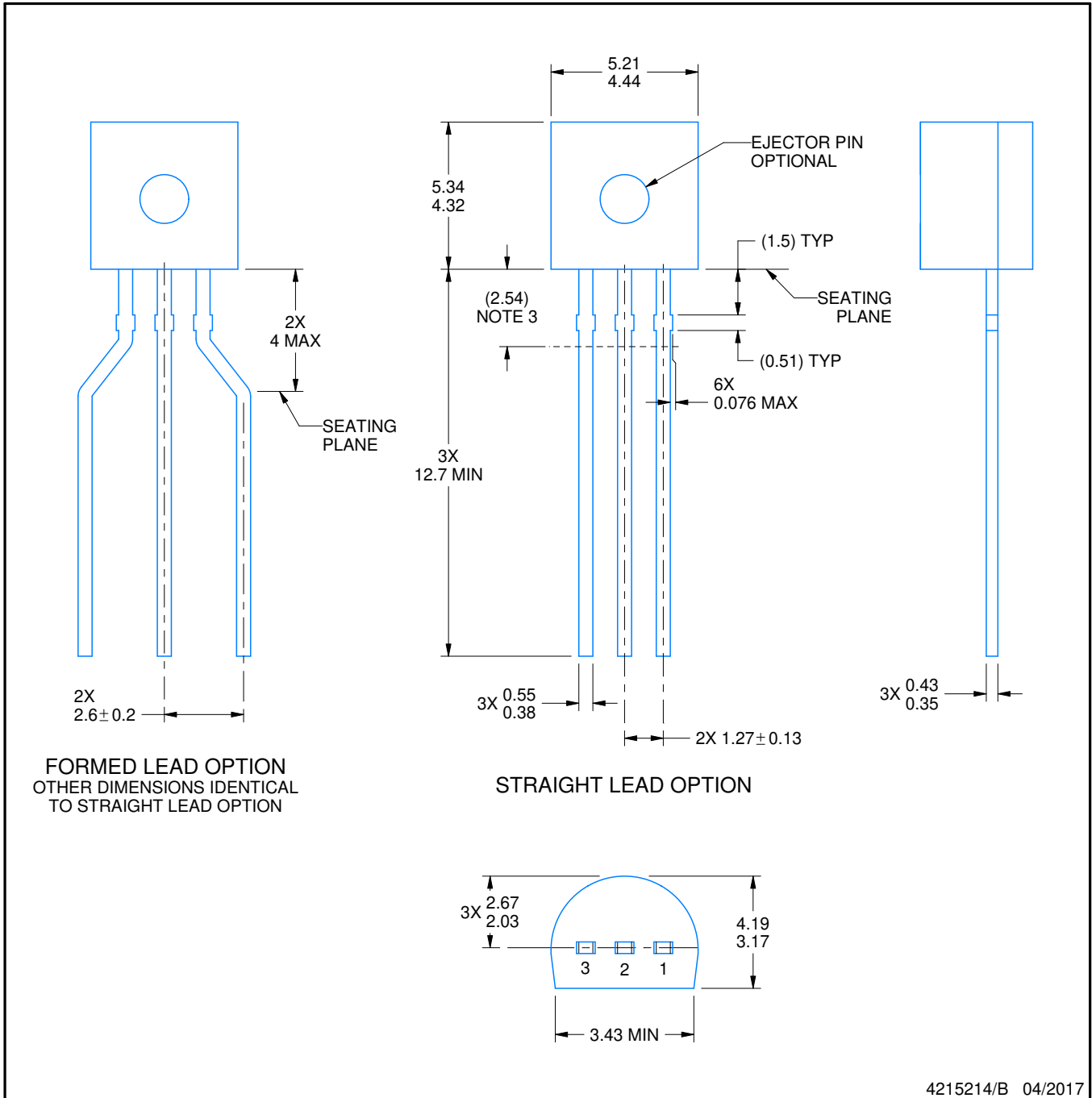
LP0003A



PACKAGE OUTLINE

TO-92 - 5.34 mm max height

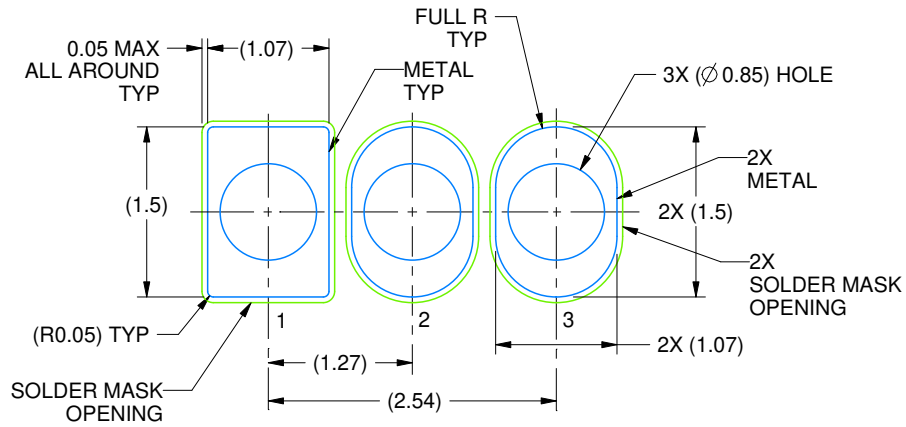
TO-92



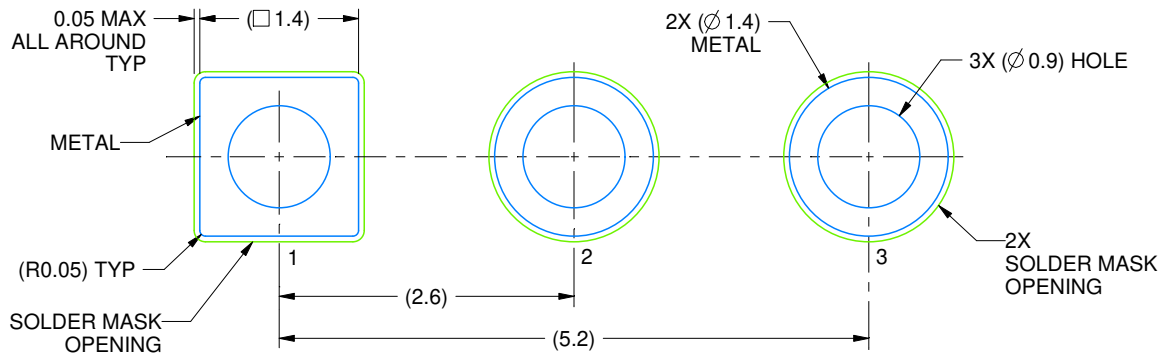
4215214/B 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
 - a. Straight lead option available in bulk pack only.
 - b. Formed lead option available in tape and reel or ammo pack.
 - c. Specific products can be offered in limited combinations of shipping medium and lead options.
 - d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



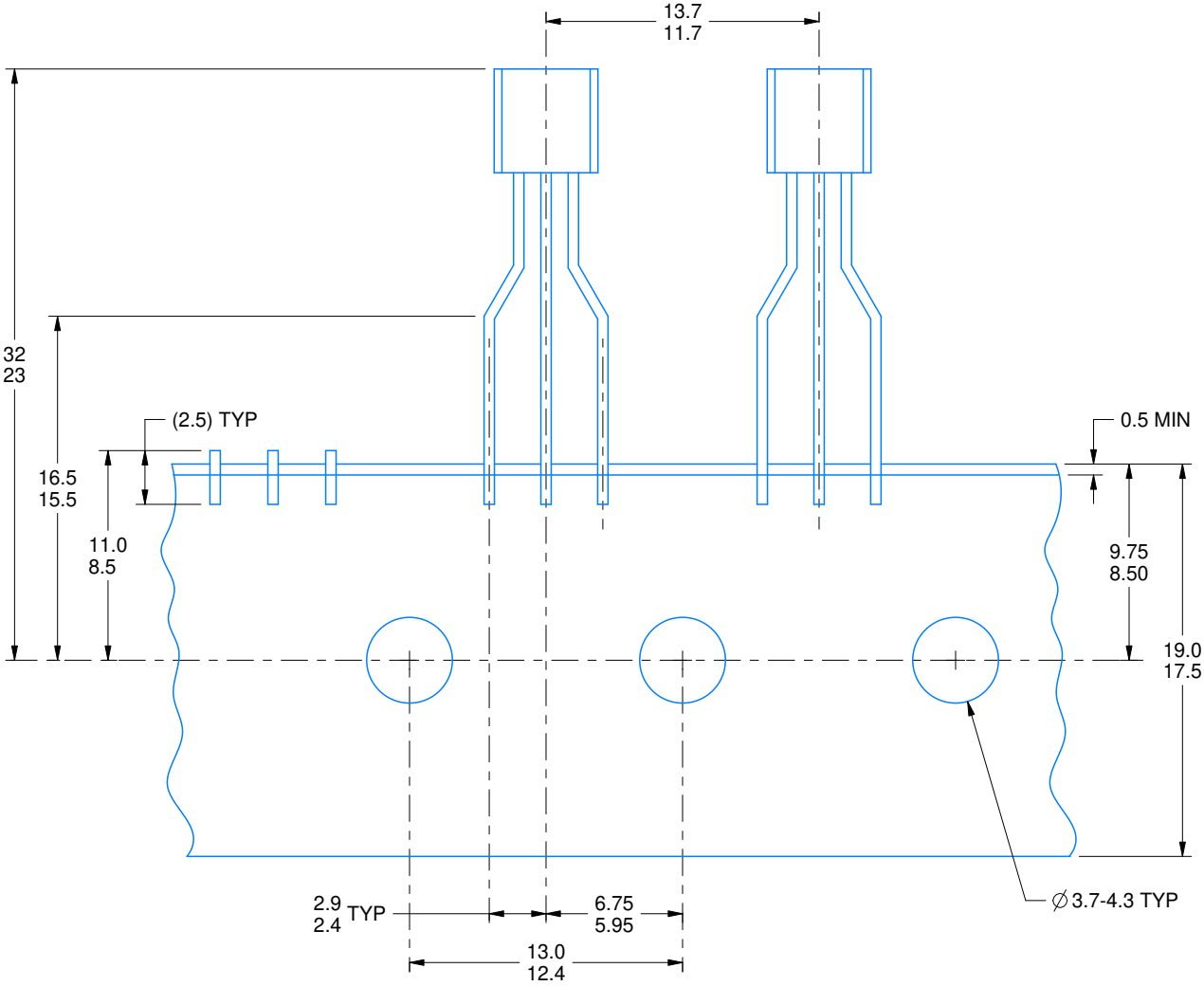
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

TAPE SPECIFICATIONS

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017

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