

FEATURES

High Off Isolation –80 dB at 30 MHz
–3 dB Signal Bandwidth 250 MHz
+1.8 V to +5.5 V Single Supply
Low On-Resistance (15 Ω Typically)
Low On-Resistance Flatness
Fast Switching Times
t_{ON} Typically 8 ns
t_{OFF} Typically 3 ns
Typical Power Consumption < 0.01 μ W
TTL/CMOS Compatible

APPLICATIONS

Audio and Video Switching
RF Switching
Networking Applications
Battery Powered Systems
Communication Systems
Relay Replacement
Sample-and-Hold Systems

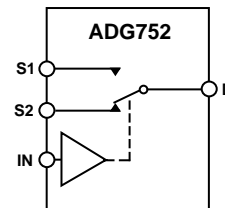
GENERAL DESCRIPTION

The ADG752 is a low voltage SPDT (single pole, double throw) switch. It is constructed using switches in a T-switch configuration, which results in excellent Off Isolation while maintaining good frequency response in the ON condition.

High off isolation and wide signal bandwidth make this part suitable for switching RF and video signals. Low power consumption and operating supply range of +1.8 V to +5.5 V make it ideal for battery powered, portable instruments.

The ADG752 is designed on a submicron process that provides low power dissipation yet gives high switching speed and low on resistance. This part is a fully bidirectional switch and can handle signals up to and including the supply rails. Break-before-make switching action ensures the input signals are protected against momentary shorting when switching between channels.

The ADG752 is available in 6-lead SOT-23 and 8-lead μ SOIC packages.

FUNCTIONAL BLOCK DIAGRAM

SWITCH SHOWN FOR A LOGIC "1" INPUT

PRODUCT HIGHLIGHTS

1. High Off Isolation –80 dB at 30 MHz.
2. –3 dB Signal Bandwidth 250 MHz.
3. Low On Resistance (15 Ω).
4. Low Power Consumption, typically <0.01 μ W.
5. Break-Before-Make Switching Action.
6. Tiny 6-lead SOT-23 and 8-lead μ SOIC packages.

REV. A

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ADG752—SPECIFICATIONS (V_{DD} = +5 V ± 10%, GND = 0 V, unless otherwise noted.)

| Parameter | B Version | | Units | Test Conditions/Comments |
|--|-----------|------------------------|---------|--|
| | +25°C | -40°C to +85°C | | |
| ANALOG SWITCH | | | | |
| Analogue Signal Range | | 0 V to V _{DD} | V | |
| On-Resistance (R _{ON}) | 15 | | Ω typ | V _S = 0 V to V _{DD} , I _{DS} = 10 mA; |
| | 18 | 20 | Ω max | Test Circuit 1 |
| On-Resistance Match Between Channels (ΔR _{ON}) | 0.1 | | Ω typ | V _S = 0 V to V _{DD} , I _{DS} = 10 mA |
| | 0.6 | 0.6 | Ω max | |
| On-Resistance Flatness (R _{FLAT(ON)}) | 2 | | Ω typ | V _S = 0 V to 2.5 V, I _{DS} = 10 mA |
| | | 3 | Ω max | V _{DD} = + 4.5 V |
| LEAKAGE CURRENTS | | | | |
| Source OFF Leakage I _S (OFF) | ±0.01 | | nA typ | V _D = 4.5 V/1 V, V _S = 1 V/4.5 V; |
| | ±0.25 | ±3.0 | nA max | Test Circuit 2 |
| Channel ON Leakage I _D , I _S (ON) | ±0.01 | | nA typ | V _D = V _S = 1 V, or 4.5 V; |
| | ±0.25 | ±3.0 | nA max | Test Circuit 3 |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V _{INH} | | 2.4 | V min | |
| Input Low Voltage, V _{INL} | | 0.8 | V max | |
| Input Current | | | | |
| I _{INL} or I _{INH} | 0.001 | | μA typ | V _{IN} = V _{INL} or V _{INH} |
| | | ±0.5 | μA max | |
| C _{IN} , Digital Input Capacitance | 2 | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | |
| t _{ON} | 8 | | ns typ | R _L = 300 Ω, C _L = 35 pF; |
| | | 13 | ns max | V _S = 3 V, Test Circuit 4 |
| t _{OFF} | 3 | | ns typ | R _L = 300 Ω, C _L = 35 pF; |
| | | 5 | ns max | V _S = 3 V, Test Circuit 4 |
| Break-Before-Make Time Delay | 6 | | ns typ | R _L = 300 Ω, C _L = 35 pF; |
| | | 1 | ns min | V _S = 3 V, Test Circuit 5 |
| Off Isolation | -80 | | dB typ | R _L = 50 Ω, C _L = 5 pF, f = 30 MHz; |
| | | | | Test Circuit 6 |
| Crosstalk | -80 | | dB typ | R _L = 50 Ω, C _L = 5 pF, f = 30 MHz; |
| | | | | Test Circuit 7 |
| -3 dB Bandwidth | 250 | | MHz typ | R _L = 50 Ω, C _L = 5 pF, Test Circuit 8 |
| C _S (OFF) | 4 | | pF typ | |
| C _D , C _S (ON) | 15 | | pF typ | |
| POWER REQUIREMENTS | | | | |
| I _{DD} | 0.001 | | μA typ | V _{DD} = +5.5 V |
| | 0.1 | 0.5 | μA max | Digital Inputs = 0 V or +5.5 V |

NOTES

¹Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS ($V_{DD} = +3\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.)

ADG752

| Parameter | B Version | | Units | Test Conditions/Comments |
|--|--------------------------|-------------------|--|---|
| | +25°C | -40°C to +85°C | | |
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 V to V_{DD} | V | |
| On-Resistance (R_{ON}) | 35 | 50 | Ω typ Ω max | $V_S = 0\text{ V}$ to V_{DD} , $I_{DS} = 10\text{ mA}$; Test Circuit 1 |
| On-Resistance Match Between Channels (ΔR_{ON}) | 0.2 2.5 | 2.5 | Ω typ Ω max | $V_S = 0\text{ V}$ to V_{DD} , $I_{DS} = 10\text{ mA}$ |
| LEAKAGE CURRENTS | | | | |
| Source OFF Leakage I_S (OFF) | ± 0.01 ± 0.25 | ± 3.0 | nA typ nA max | $V_{DD} = +3.3\text{ V}$ $V_S = 3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3\text{ V}$; Test Circuit 2 |
| Channel ON Leakage I_D , I_S (ON) | ± 0.01 ± 0.25 | ± 3.0 | nA typ nA max | $V_S = V_D = 1\text{ V}$ or 3 V ; Test Circuit 3 |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | 0.4 | V max | |
| Input Current I_{INL} or I_{INH} | 0.001 | ± 0.5 | μA typ μA max | $V_{IN} = V_{INL}$ or V_{INH} |
| C_{IN} , Digital Input Capacitance | 2 | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | |
| t_{ON} | 10 | 18 | ns typ ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 2\text{ V}$, Test Circuit 4 |
| t_{OFF} | 4 | 8 | ns typ ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 2\text{ V}$, Test Circuit 4 |
| Break-Before-Make Time Delay | 6 | 1 | ns typ ns min | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 2\text{ V}$, Test Circuit 5 |
| Off Isolation | -80 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 30\text{ MHz}$; Test Circuit 6 |
| Crosstalk | -80 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 30\text{ MHz}$; Test Circuit 7 |
| -3 dB Bandwidth | 250 | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 8 |
| C_S (OFF) | 4 | | pF typ | |
| C_D , C_S (ON) | 15 | | pF typ | |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.001 0.1 | 0.5 | μA typ μA max | $V_{DD} = +3.3\text{ V}$ Digital Inputs = 0 V or +3.3 V |

NOTES

¹Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG752

ABSOLUTE MAXIMUM RATINGS¹

(T_A = +25°C unless otherwise noted)

| | |
|---|---|
| V _{DD} to GND | −0.3 V to +6 V |
| Analog, Digital Inputs ² | −0.3 V to V _{DD} +0.3 V or 30 mA, Whichever Occurs First |
| Peak Current, S or D | 100 mA (Pulsed at 1 ms, 10% Duty Cycle Max) |
| Continuous Current, S or D | 30 mA |
| Operating Temperature Range | |
| Industrial (B Version) | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Power Dissipation | (T _J Max−T _A)/θ _{JA} |
| Junction Temperature (T _J Max) | +150°C |
| μSOIC Package | |
| θ _{JA} Thermal Impedance | 206°C/W |
| θ _{JC} Thermal Impedance | 44°C/W |
| SOT-23 Package | |
| θ _{JA} Thermal Impedance | 229.6°C/W |
| θ _{JC} Thermal Impedance | 91.99°C/W |
| Lead Temperature, Soldering | |
| Vapor Phase (60 sec) | +215°C |
| Infrared (15 sec) | +220°C |

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overtypes at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

PIN CONFIGURATIONS

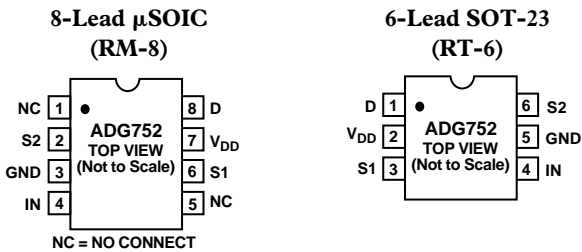


Table I. Truth Table

| ADG752 IN | Switch S1 | Switch S2 |
|-----------|-----------|-----------|
| 0 | ON | OFF |
| 1 | OFF | ON |

TERMINOLOGY

| | |
|--------------------------------------|--|
| V _{DD} | Most positive power supply potential. |
| GND | Ground (0 V) reference. |
| S | Source terminal. May be an input or output. |
| D | Drain terminal. May be an input or output. |
| IN | Logic control input. |
| R _{ON} | Ohmic resistance between D and S. |
| ΔR _{ON} | On resistance match between channels, i.e., R _{ONmax} −R _{ONmin} . |
| R _{FLAT(ON)} | Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range. |
| I _S (OFF) | Source leakage current with the switch “OFF.” |
| I _D , I _S (ON) | Channel leakage current with the switch “ON.” |
| V _D (V _S) | Analog voltage on terminals D and S. |
| C _S (OFF) | “OFF” switch source capacitance. |
| C _D , C _S (ON) | “ON” switch capacitance. |
| t _{ON} | Delay between applying the digital control input and the output switching on. See Test Circuit 4. |
| t _{OFF} | Delay between applying the digital control input and the output switching off. |
| t _D | “OFF” time or “ON” time measured between the 90% points of both switches, when switching from one address state to another. |
| Off Isolation | A measure of unwanted signal coupling through an “OFF” switch. |
| Crosstalk | A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. |
| Bandwidth | The frequency at which the output is attenuated by −3 dBs. |
| On Response | The frequency response of the “ON” switch. |
| Insertion Loss | Loss due to the ON resistance of the switch. |
| V _{INL} | Maximum input voltage for Logic “0.” |
| V _{INH} | Minimum input voltage for Logic “1.” |
| I _{INL} (I _{INH}) | Input current of the digital input. |
| I _{DD} | Positive supply current. |

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG752 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Typical Performance Characteristics—ADG752

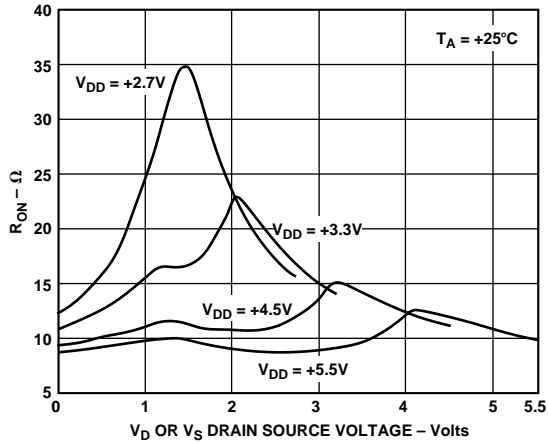


Figure 1. On Resistance as a Function of V_D (V_S) Single Supplies

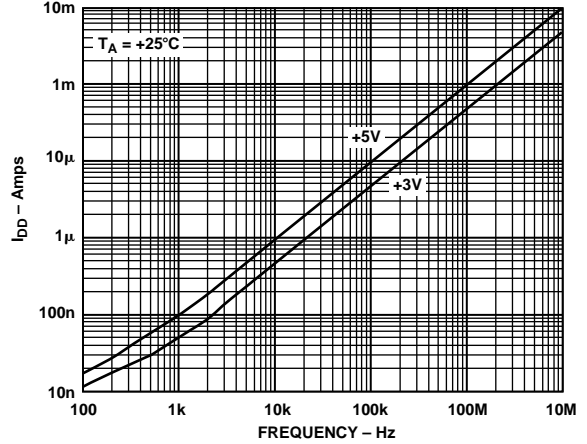


Figure 4. Supply Current vs. Input Switching Frequency

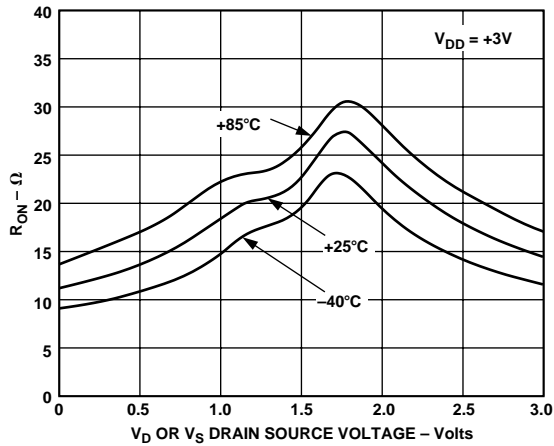


Figure 2. On Resistance as a Function of V_D (V_S) for Different Temperatures $V_{DD} = 3\text{V}$

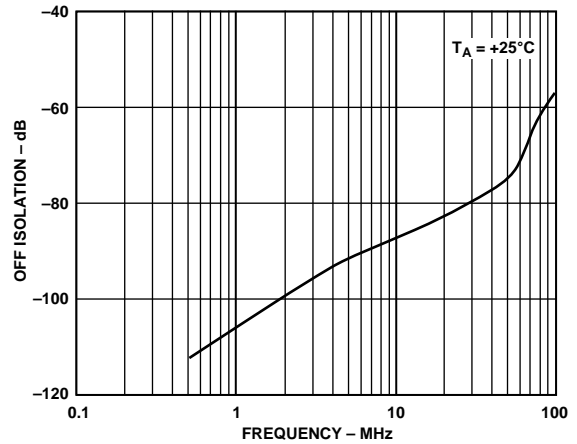


Figure 5. Off Isolation vs. Frequency

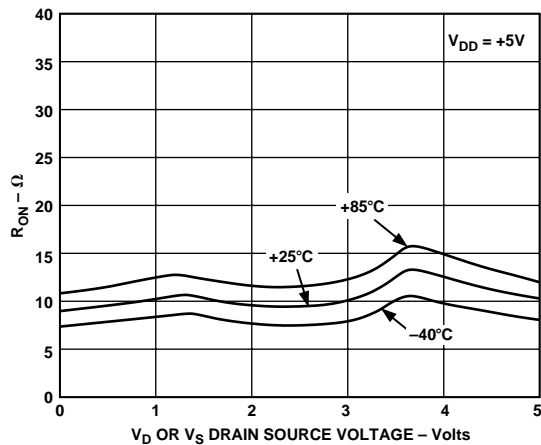


Figure 3. On Resistance as a Function of V_D (V_S) for Different Temperatures $V_{DD} = 5\text{V}$

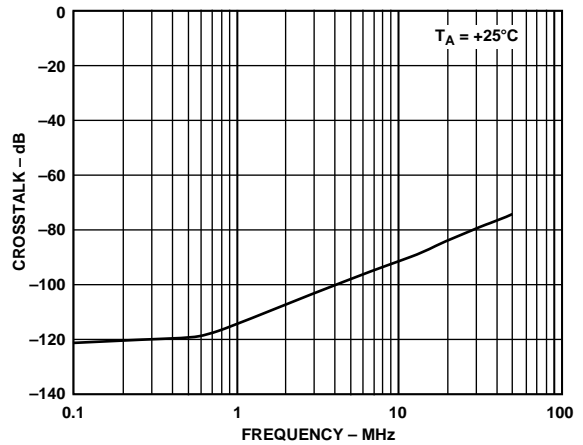


Figure 6. Crosstalk vs. Frequency

ADG752

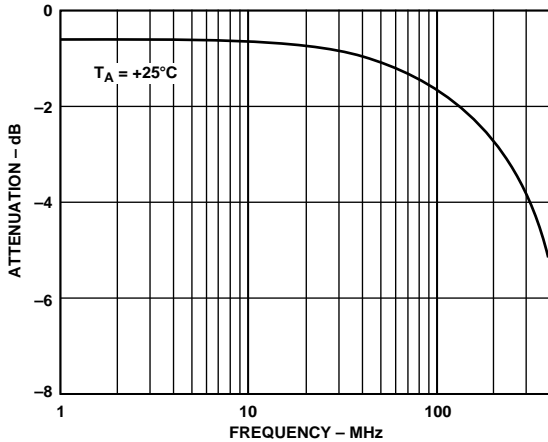


Figure 7. On Response vs. Frequency

GENERAL DESCRIPTION

The ADG752 is an SPDT switch constructed using switches in a T configuration to obtain high “OFF” isolation while maintaining good frequency response in the “ON” condition.

Figure 8 shows the T-switch configuration. While the switch is in the OFF state, the shunt switch is closed and the two series switches are open. The closed shunt switch provides a signal path to ground for any of the unwanted signals that find their way through the off capacitances of the series’ MOS devices. This results in more improved isolation between the input and output than with an ordinary series switch. When the switch is in the ON condition, the shunt switch is open and the signal path is through the two series switches which are now closed.

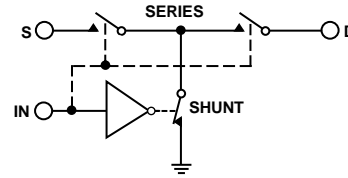


Figure 8. Basic T-Switch Configuration

LAYOUT CONSIDERATIONS

Where accurate high frequency operation is important, careful consideration should be given to the printed circuit board layout and to grounding. Wire wrap boards, prototype boards and sockets are not recommended because of their high parasitic inductance and capacitance. The part should be soldered directly to a printed circuit board. A ground plane should cover all unused areas of the component side of the board to provide a low impedance path to ground. Removing the ground planes from the area around the part reduces stray capacitance.

Good decoupling is important in achieving optimum performance. V_{DD} should be decoupled with a 0.1 μF surface mount capacitor to ground mounted as close as possible to the device itself.

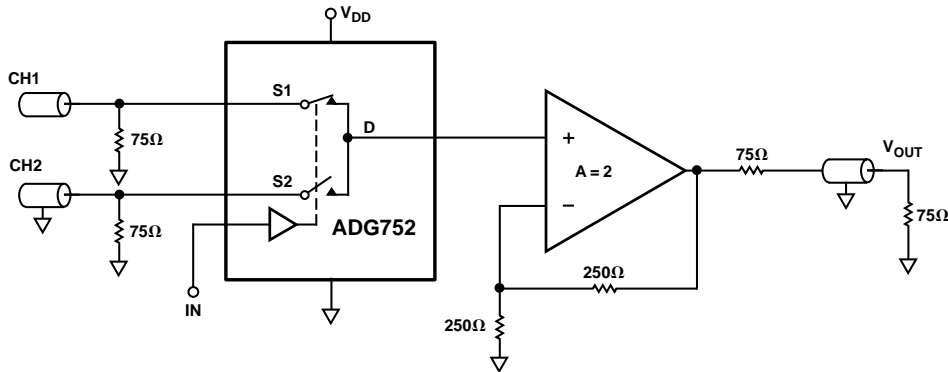
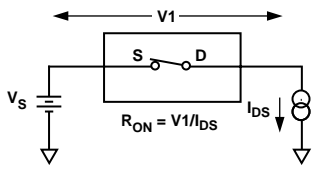
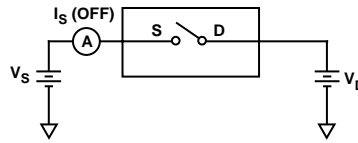


Figure 9. Multiplexing Between Two Video Signals

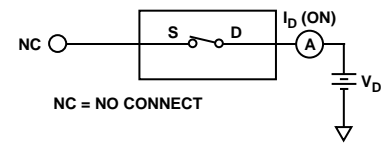
Test Circuits



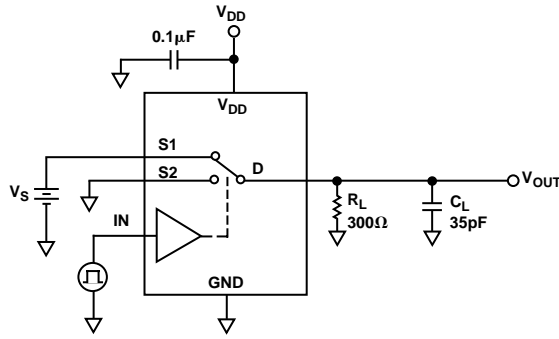
Test Circuit 1. On Resistance



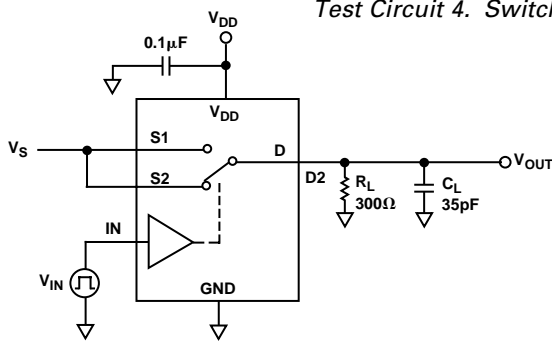
Test Circuit 2. Off Leakage



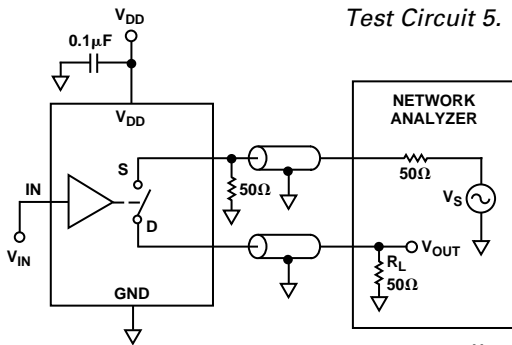
Test Circuit 3. On Leakage



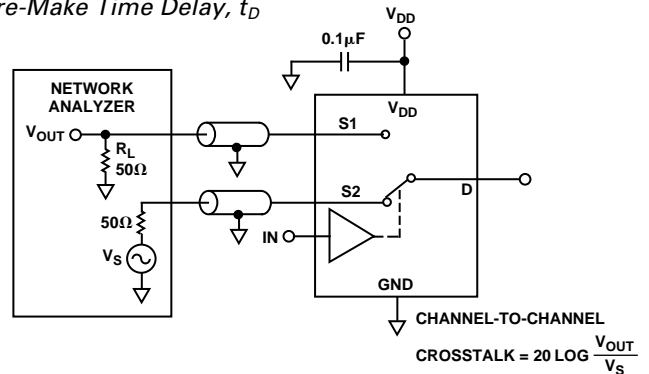
Test Circuit 4. Switching Times



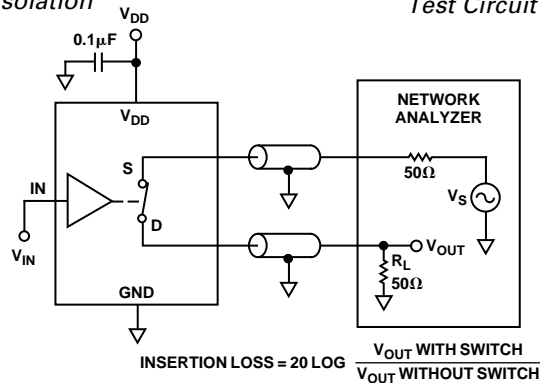
Test Circuit 5. Break-Before-Make Time Delay, t_D



Test Circuit 6. Off Isolation

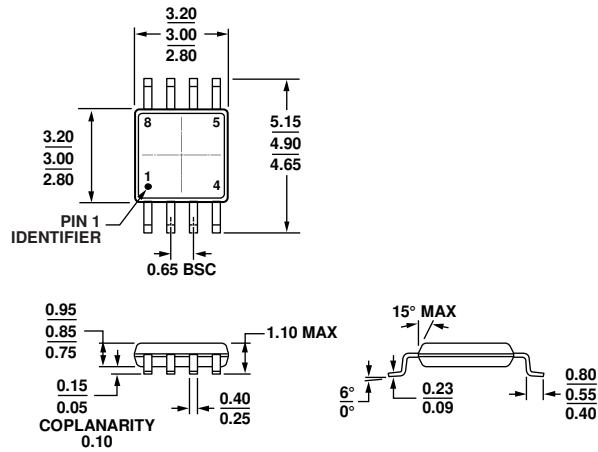


Test Circuit 7. Channel-to-Channel Crosstalk



Test Circuit 8. Bandwidth

OUTLINE DIMENSIONS

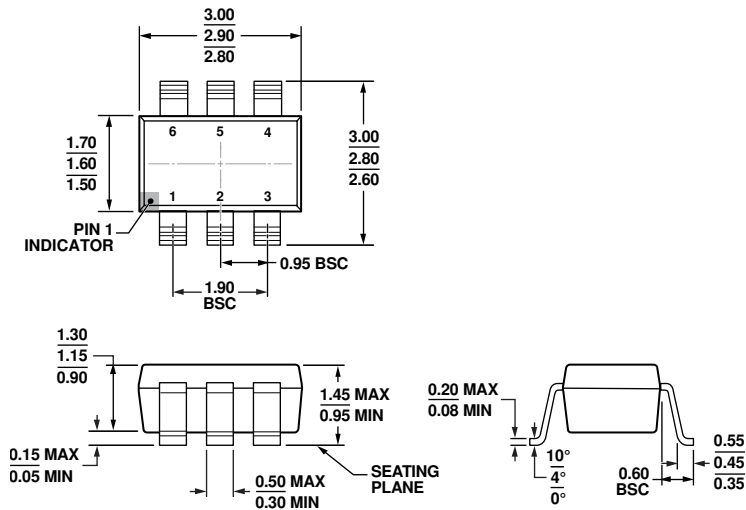


COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 10. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

10-07-2009-B



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 11. 6-Lead Small Outline Transistor Package [SOT-23] (RJ-6)

Dimensions shown in millimeters

12-16-2009-A

ORDERING GUIDE

| Model ¹ | Temperature Range | Brand | Package Description | Package Option |
|--------------------|-------------------|-------|--|----------------|
| ADG752BRM-REEL | -40°C to +85°C | SEB | 8-Lead Mini Small Outline Package [MSOP] | RM-8 |
| ADG752BRMZ | -40°C to +85°C | S1H | 8-Lead Mini Small Outline Package [MSOP] | RM-8 |
| ADG752BRT-REEL | -40°C to +85°C | SEB | 6-Lead Small Outline Transistor Package [SOT-23] | RJ-6 |
| ADG752BRT-REEL7 | -40°C to +85°C | SEB | 6-Lead Small Outline Transistor Package [SOT-23] | RJ-6 |
| ADG752BRTZ-REEL | -40°C to +85°C | SEB# | 6-Lead Small Outline Transistor Package [SOT-23] | RJ-6 |
| ADG752BRTZ-REEL7 | -40°C to +85°C | SEB# | 6-Lead Small Outline Transistor Package [SOT-23] | RJ-6 |

¹ Z = RoHS Compliant Part.

REVISION HISTORY**10/13—Rev. 0 to Rev. A**

| | |
|----------------------------------|---|
| Updated Outline Dimensions | 8 |
| Changes to Ordering Guide | 9 |

4/99—Revision 0: Initial Version