MOTOROLA

Dual 2-Wide AND/OR/INVERT Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/30401

Military 54LS51

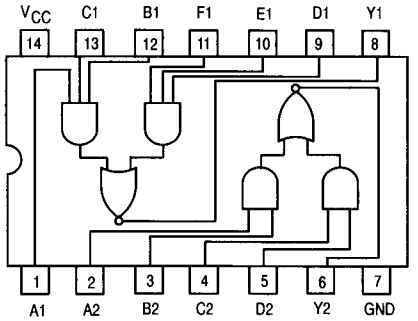
AVAILABLE AS:

1) JAN: JM38510/30401BXA
2) SMD: N/A
3) 883: 54LS51/BXAJC

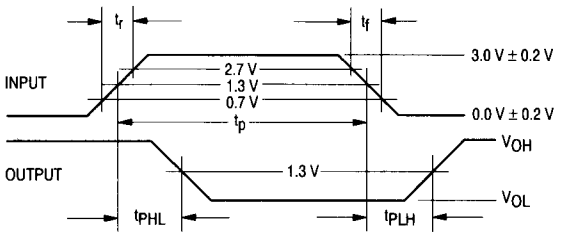
X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

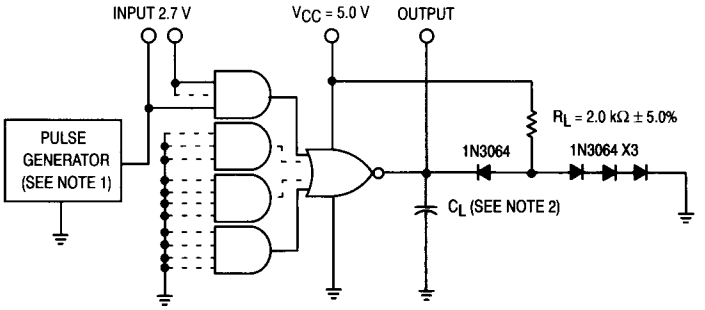
LOGIC DIAGRAM



WAVEFORMS



AC TEST CIRCUIT



PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
A1	1	1	2	V_{CC}
A2	2	2	3	GND
B2	3	3	4	V_{CC}
C2	4	4	6	V_{CC}
D2	5	5	8	GND
Y2	6	6	9	V_{CC}
GND	7	7	10	GND
Y1	8	8	12	V_{CC}
D1	9	9	13	V_{CC}
E1	10	10	14	GND
F1	11	11	16	V_{CC}
B1	12	12	18	V_{CC}
C1	13	13	19	GND
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

NOTES:
1. The pulse generator has the following characteristics: $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, PRR ≤ 1.0 MHz, $t_p = 0.5$ µs and $Z_{OUT} \approx 50\ \Omega$.
2. $C_L = 50$ pF ± 10%, including scope probe, wiring and stray capacitance, without package in test fixture.
3. $R_L = 2.0$ kΩ ± 5.0%.
4. Voltage measurements are to be made with respect to network ground terminal.
5. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

5

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = – 400 µA, V_{IL} = 0.7 V, V_{IN} = 5.5 V on other inputs.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IH} = 2.0 V, V_{IN} = 0 V on other inputs.
V_{IC}	Input Clamping Voltage		– 1.5					V	V_{CC} = 4.5 V, I_{IN} = – 18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs = 0 V.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs = 0 V.
I_{IL}	Logical "0" Input Current	– 150	– 380	– 150	– 380	– 150	– 380	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs = 5.5 V.
I_{OS}	Output Short Circuit Current	– 15	– 100	– 15	– 100	– 15	– 100	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs), V_{OUT} = 0 V.
I_{CCH}	Power Supply Current		1.6		1.6		1.6	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs).
I_{CCL}	Power Supply Current		2.8		2.8		2.8	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL} t_{PHL}	Propagation Delay /Data-Output Output High-Low	3.0 —	22 20	3.0 —	30 25	3.0 —	30 25	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ.
t_{PLH} t_{PLH}	Propagation Delay /Data-Output Output Low-High	3.0 —	19 20	3.0 —	30 25	3.0 —	30 25	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ.

NOTE:
1. The limits specified for C_L = 15 pF are guaranteed but not tested.

5