NCS2002, NCV2002

Sub-One Volt Rail-to-Rail Operational Amplifier with Enable Feature

The NCS2002 is an industry first sub−one volt operational amplifier that features a rail−to−rail common mode input voltage range, along with rail−to−rail output drive capability. This amplifier is guaranteed to be fully operational down to 0.9 V, providing an ideal solution for powering applications from a single cell Nickel Cadmium (NiCd) or Nickel Metal Hydride (NiMH) battery. Additional features include no output phase reversal with overdriven inputs, trimmed input offset voltage of 0.5 mV, extremely low input bias current of 40 pA, and a unity gain bandwidth of 1.1 MHz at 5.0 V.

The NCS2002 also has an active high enable pin that allows external shutdown of the device. In the standby mode, the supply current is typically 1.9 μA at 1.0 V. Because of its small size and enable feature, this amplifier represents the ideal solution for small portable electronic applications. The NCS2002 is available in the space saving SOT23−6 (TSOP−6) package with two industry standard pinouts.

Features

- 0.9 V Guaranteed Operation
- Standby Mode: I_D = 1.9 μA at 1.0 V, Typical
- Rail−to−Rail Common Mode Input Voltage Range
- Rail−to−Rail Output Drive Capability
- No Output Phase Reversal for Over−Driven Input Signals
- 0.5 mV Trimmed Input Offset
- 10 pA Input Bias Current
- 1.1 MHz Unity Gain Bandwidth at ±2.5 V, 1.0 MHz at ±0.5 V
- Tiny SOT23−6 (TSOP−6) Package
- NCV Parts − AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Single Cell NiCd / NiMH Battery Powered Applications
- Cellular Telephones
- Pagers
- Personal Digital Assistants
- Electronic Games
- Digital Cameras
- Camcorders
- Hand Held Instruments

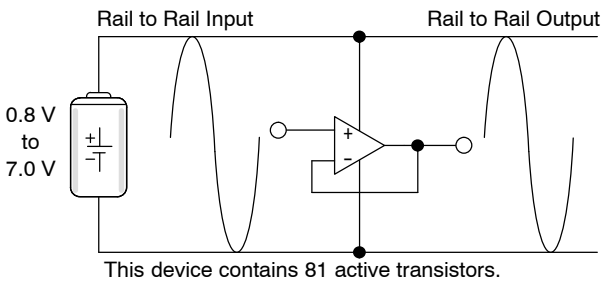


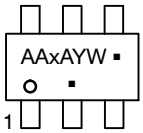
Figure 1. Typical Application

ON Semiconductor®

http://onsemi.com

TSSOP−6
SN SUFFIX
CASE 318G

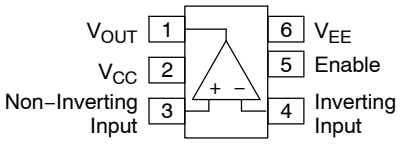
MARKING DIAGRAM



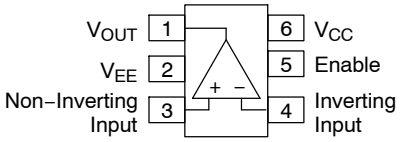
AA = Device Code
x = Marking Defined on Page 15 in Ordering Information
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



Style 1 Pinout (SN1T1)



Style 2 Pinout (SN2T1)

ORDERING AND MARKING INFORMATION

See detailed ordering, marking, and shipping information in the package dimensions section on page 15 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	7.0	V
Input Differential Voltage Range (Note 1)	V_{IDR}	V_{EE} − 300 mV to 7.0 V	V
Input Common Mode Voltage Range (Note 1)	V_{ICR}	V_{EE} − 300 mV to 7.0 V	V
Output Short Circuit Duration (Note 2)	t_{Sc}	Indefinite	sec
Junction Temperature	T_J	150	°C
Power Dissipation and Thermal Characteristics SOT23−6 Package Thermal Resistance, Junction−to−Air Power Dissipation @ T_A = 70°C	 $R_{\theta JA}$ P_D	 235 340	 °C/W mW
Operating Ambient Temperature Range NCS2002 NCV2002 (Note 3)	T_A	 −40 to 105 −40 to 125	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C
ESD Protection at any Pin Human Body Model (Note 4)	V_{ESD}	1500	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Either or both inputs should not exceed the range of V_{EE} − 300 mV to V_{EE} + 7.0 V.
2. Maximum package power dissipation limits must be observed to ensure that the maximum junction temperature is not exceeded. $T_J T_A + (P_D R_{\theta JA})$
3. NCV prefix is for automotive and other applications requiring site and change control.
4. ESD data available upon request.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.5 V, V_{EE} = −2.5 V, V_{CM} = V_O = 0 V, R_L to GND, T_A = 25°C, unless otherwise noted)

Rating	Symbol	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}				mV
V_{CC} = 0.45 V, V_{EE} = −0.45 V					
T_A = 25°C		−6.0	0.5	6.0	
T_A = 0°C to 70°C		−8.5	–	8.5	
T_A = −40 to +125°C		−9.5	–	9.5	
V_{CC} = 1.5 V, V_{EE} = −1.5 V					
T_A = 25°C		−6.0	0.5	6.0	
T_A = 0°C to 70°C		−7.0	–	7.0	
T_A = −40 to +125°C		−7.5	–	7.5	
V_{CC} = 2.5 V, V_{EE} = −2.5 V					
T_A = 25°C		−6.0	0.5	6.0	
T_A = 0°C to 70°C		−7.5	–	7.5	
T_A = −40 to +125°C		−7.5	–	7.5	
Input Offset Voltage Temperature Coefficient (R_S = 50) T_A = −40 to +125°C	$\Delta V_{IO} / \Delta T$	–	8.0	–	μV/°C
Input Bias Current (V_{CC} = 1.0 V to 5.0 V)	I_{IB}	–	10	–	pA
Input Common Mode Voltage Range	V_{ICR}	–	V_{EE} to V_{CC}	–	V
Large Signal Voltage Gain	A_{VOL}				kV/V
V_{CC} = 0.45 V, V_{EE} = −0.45 V					
R_L = 10 k		–	40	–	
V_{CC} = 1.5 V, V_{EE} = −1.5 V					
R_L = 10 k		–	40	–	
V_{CC} = 2.5 V, V_{EE} = −2.5 V					
R_L = 10 k		10	40	–	
Output Voltage Swing, High State Output (V_{ID} = + 0.5 V) T_A = T_{low} to T_{high}	V_{OH}				V
V_{CC} = 0.45 V, V_{EE} = −0.45 V					
R_L = 10 k		0.40	0.442	–	
R_L = 2.0 k		0.35	0.409	–	
V_{CC} = 1.5 V, V_{EE} = −1.5 V					
R_L = 10 k		1.45	1.494	–	
R_L = 2.0 k		1.40	1.473	–	
V_{CC} = 2.5 V, V_{EE} = −2.5 V					
R_L = 10 k		2.45	2.493	–	
R_L = 2.0 k		2.40	2.469	–	

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.5 V, V_{EE} = −2.5 V, V_{CM} = V_O = 0 V, R_L to GND, T_A = 25°C, unless otherwise noted)

Rating	Symbol	Min	Typ	Max	Unit
Output Voltage Swing, Low State Output (V_{ID} = − 0.5 V) T_A = −40 to +125°C V_{CC} = 0.45 V, V_{EE} = −0.45 V R_L = 10 k R_L = 2.0 k V_{CC} = 1.5 V, V_{EE} = −1.5 V R_L = 10 k R_L = 2.0 k V_{CC} = 2.5 V, V_{EE} = −2.5 V R_L = 10 k R_L = 2.0 k	V_{OL}	 – – – – – –	 −0.446 −0.432 −1.497 −1.484 −2.496 −2.481	 −0.40 −0.35 −1.45 −1.40 −2.45 −2.40	V
Common Mode Rejection Ratio (V_{in} = 0 to 5.0 V)	CMRR	60	82	–	dB
Power Supply Rejection Ratio (V_{CC} = 0.5 V to 2.5 V, V_{EE} = −2.5 V)	PSRR	60	85	–	dB
Output Short Circuit Current V_{CC} = 0.45 V, V_{EE} = −0.45 V, V_{ID} = ±0.4 V Source Current High Output State Sink Current Low Output State V_{CC} = 1.5 V, V_{EE} = −1.5 V, V_{ID} = ±0.5 V Source Current High Output State Sink Current Low Output State V_{CC} = 2.5 V, V_{EE} = −2.5 V, V_{ID} = ±0.5 V Source Current High Output State Sink Current Low Output State	I_{SC}	 0.5 – 25 – 65 –	 1.0 −3.0 32 −58 86 −128	 – −2.0 – −45 – −100	mA
Power Supply Current (Per Amplifier, V_O = 0 V) T_A = −40 to +125°C V_{CC} = 0.5 V to V_{EE} = −0.5 V Venable = V_{CC} Venable = V_{EE} V_{CC} = 1.5 V to V_{EE} = −1.5 V Venable = V_{CC} Venable = V_{EE} V_{CC} = 2.5 V to V_{EE} = −2.5 V Venable = V_{CC} Venable = V_{EE}	I_D	 – – – – – –	 480 1.5 720 2.2 820 2.5	 600 3.0 900 5.0 1000 5.0	μA
Enable Input Threshold Voltage (V_{CC} = 2.5 V, V_{EE} = −2.5 V) Operating Disabled	$V_{th(EN)}$	 – 1.7 V + V_{EE}	 2.7 V + V_{EE} 1.9	 2.8 V + V_{EE} –	V
Enable Input Current (V_{CC} = 5.0 V, V_{EE} = 0) Enable = 5.0 V Enable = GND	I_{Enable}	 – –	 1.1 1.1	 2.0 2.0	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.5 V, V_{EE} = −2.5 V, V_{CM} = V_O = 0 V, R_L to GND, T_A = 25°C, unless otherwise noted)

Rating	Symbol	Min	Typ	Max	Unit
Differential Input Resistance (V_{CM} = 0 V)	R_{in}	–	>1.0	–	tera Ω
Differential Input Capacitance (V_{CM} = 0 V)	C_{in}	–	3.0	–	pf
Equivalent Input Noise Voltage (f = 1.0 kHz)	e_n	–	100	–	nV/√Hz
Gain Bandwidth Product (f = 100 kHz) V_{CC} = 0.45 V, V_{EE} = −0.45 V V_{CC} = 1.5 V, V_{EE} = −1.5 V V_{CC} = 2.5 V, V_{EE} = −2.5 V	GBW	 – – 0.6	 0.8 0.8 0.9	 – – –	MHz
Gain Margin (R_L = 10 k, C_L = 5.0 pf)	Am	–	6.5	–	dB
Phase Margin (R_L = 10 k, C_L = 5.0 pf)	ϕm	–	60	–	Deg
Power Bandwidth (V_O = 4.0 V_{PP}, R_L = 2.0 k, THD = 1.0 %, A_V = 1.0)	BW_P	–	80	–	kHz
Total Harmonic Distortion (V_O = 4.0 V_{PP}, R_L = 2.0 k, A_V = 1.0) f = 1.0 kHz f = 10 kHz	THD	 – –	 0.008 0.08	 – –	%
Slew Rate (V_S = ±2.5 V, V_O = −2.0 V to 2.0 V, R_L = 2.0 k, A_V = 1.0) Positive Slope Negative Slope	SR	 0.85 0.85	 1.2 1.3	 – –	V/μs
Time Delay for Device to Turn On (R_L = 10 k)	t_{on}	–	5.5	7.5	μs
Time Delay for Device to Turn Off (R_L = 10 k)	t_{off}	–	2.5	3.0	μs

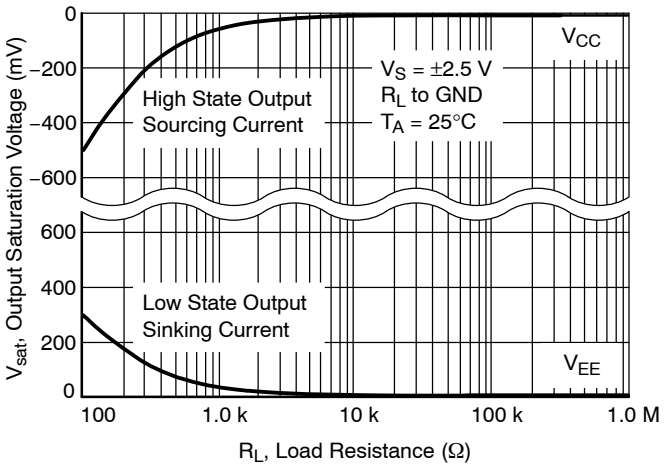


Figure 2. Output Saturation Voltage versus Load Resistance

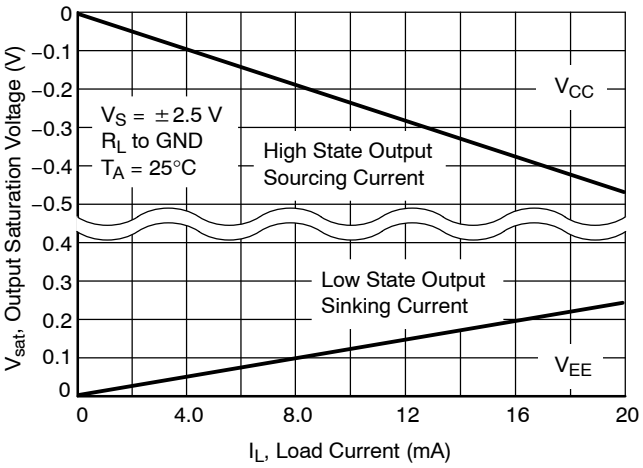


Figure 3. Output Saturation Voltage versus Load Current

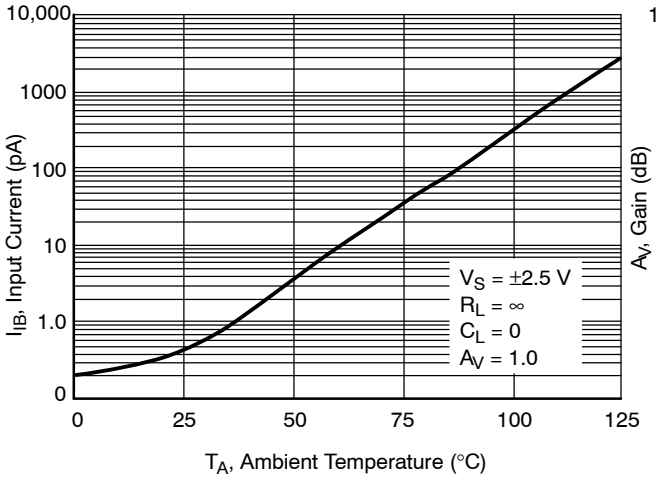


Figure 4. Input Bias Current versus Temperature

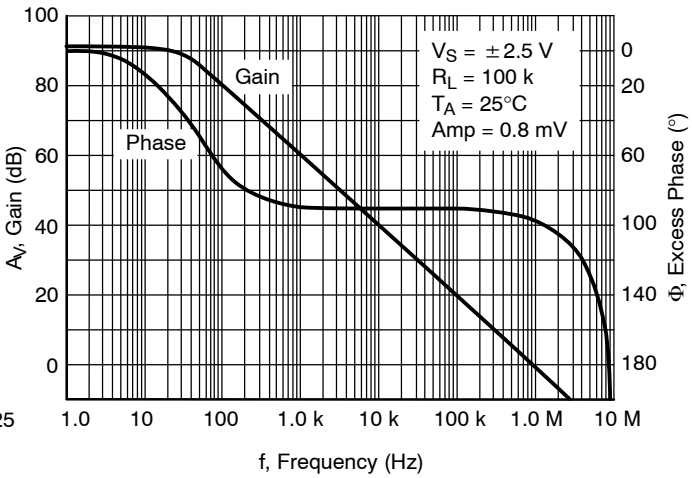


Figure 5. Gain and Phase versus Frequency

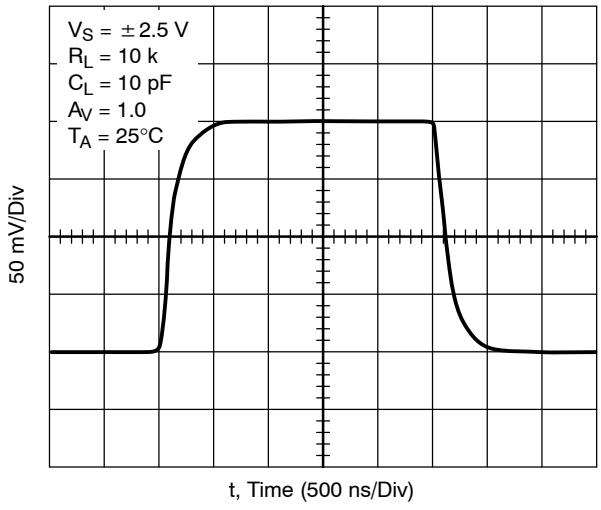


Figure 6. Transient Response

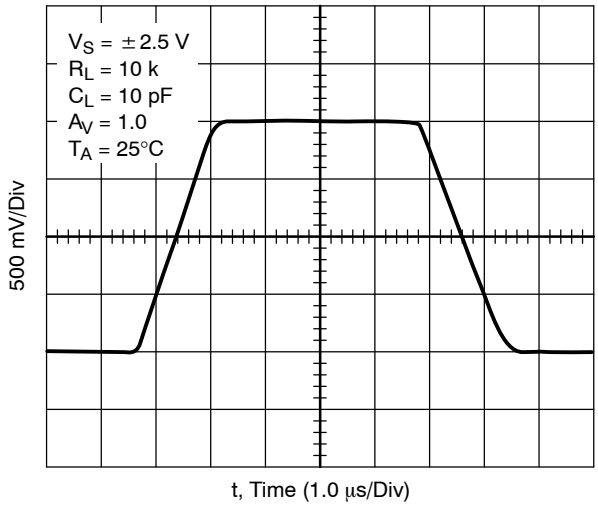


Figure 7. Slew Rate

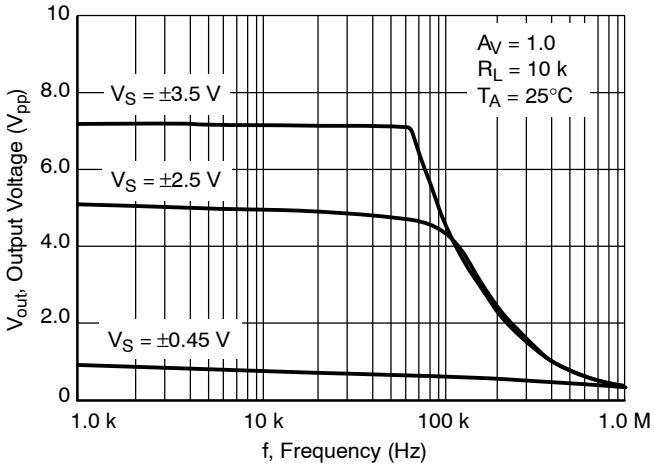


Figure 8. Output Voltage versus Frequency

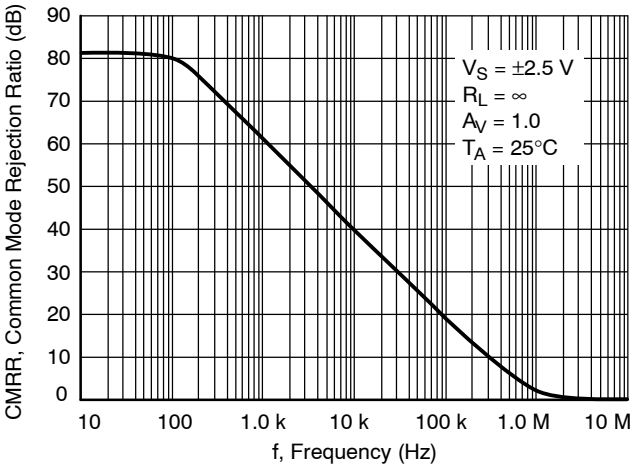


Figure 9. Common Mode Rejection Ratio versus Frequency

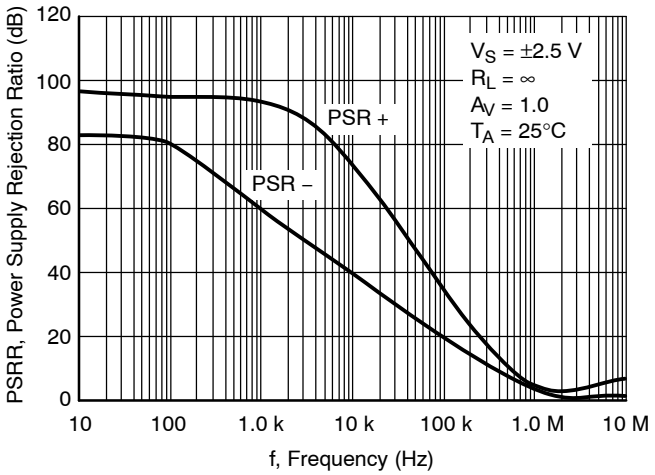


Figure 10. Power Supply Rejection Ratio versus Frequency

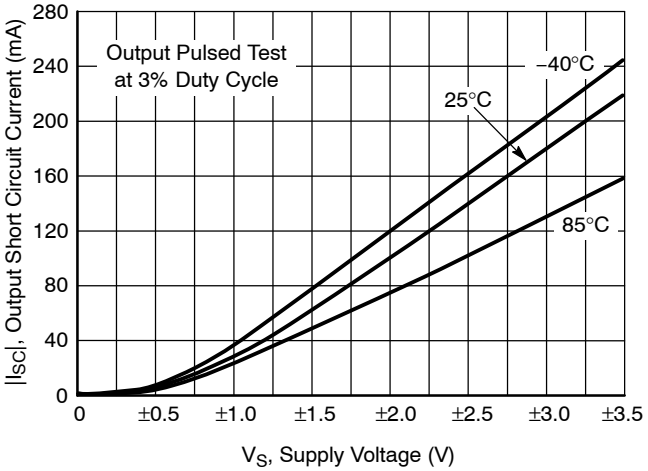


Figure 11. Output Short Circuit Sinking Current versus Supply Voltage

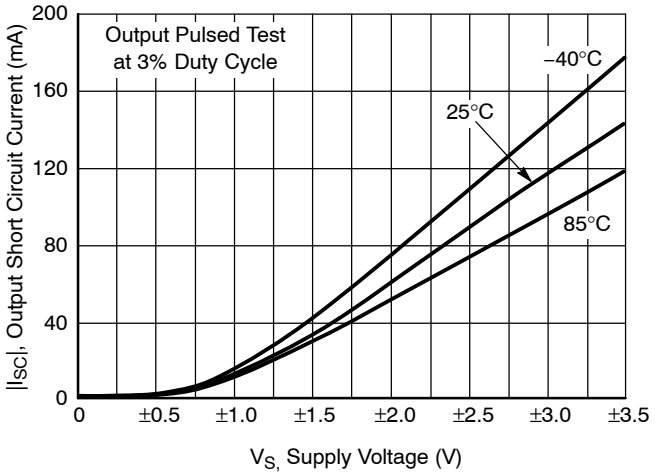


Figure 12. Output Short Circuit Sourcing Current versus Supply Voltage

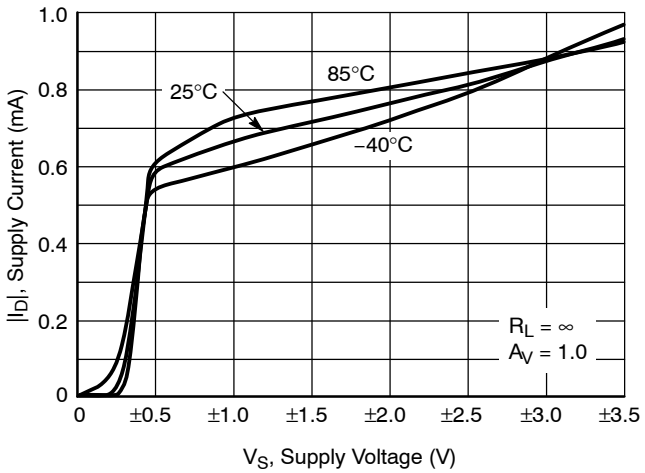


Figure 13. Supply Current versus Supply Voltage with No Load

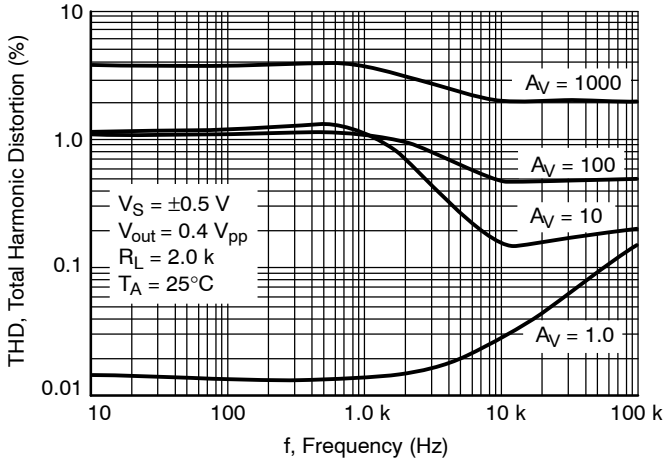


Figure 14. Total Harmonic Distortion versus Frequency with 1.0 V Supply

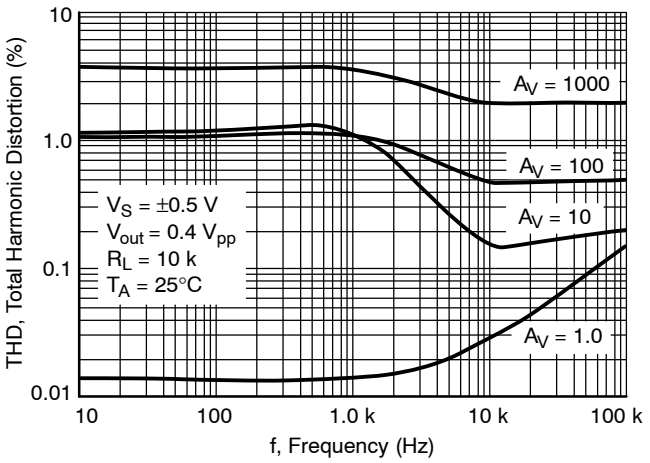


Figure 15. Total Harmonic Distortion versus Frequency with 1.0 V Supply

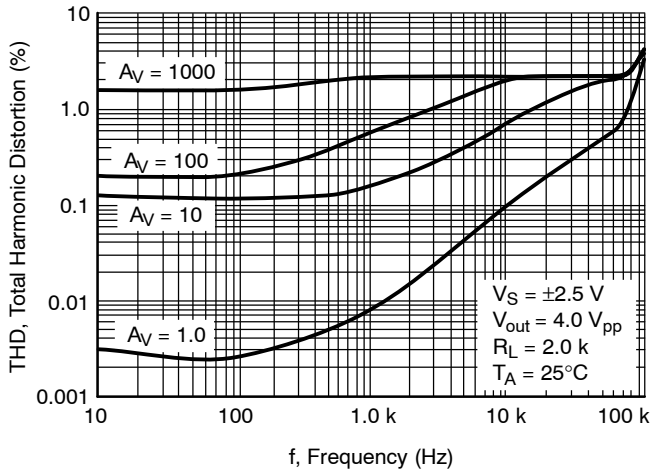


Figure 16. Total Harmonic Distortion versus Frequency with 5.0 V Supply

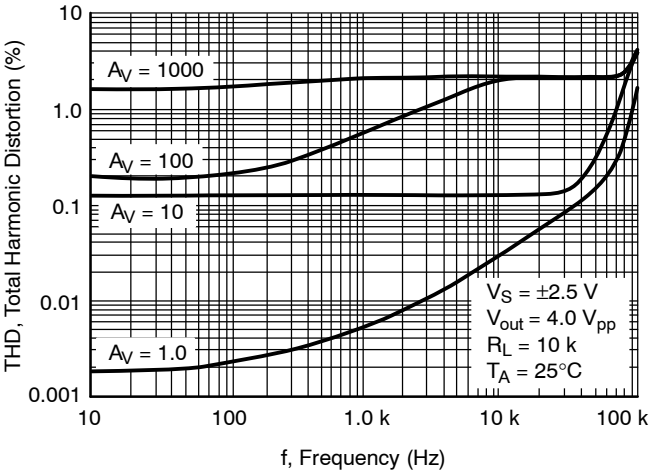


Figure 17. Total Harmonic Distortion versus Frequency with 5.0 V Supply

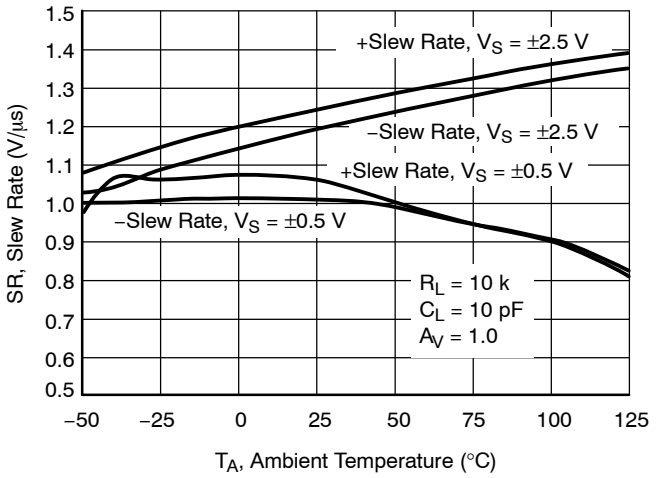


Figure 18. Slew Rate versus Temperature

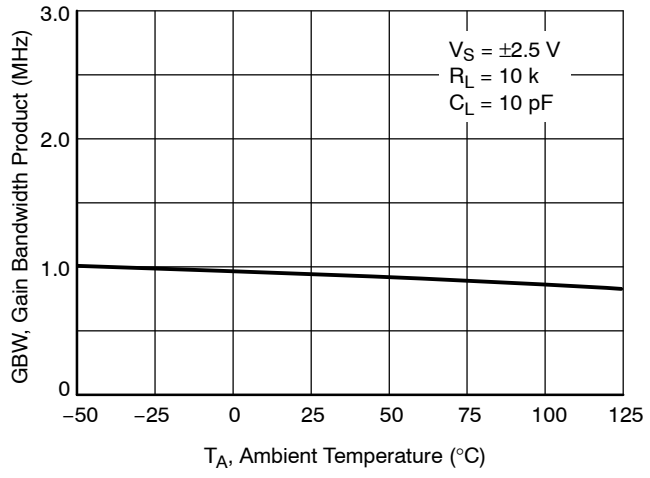


Figure 19. Gain Bandwidth Product versus Temperature

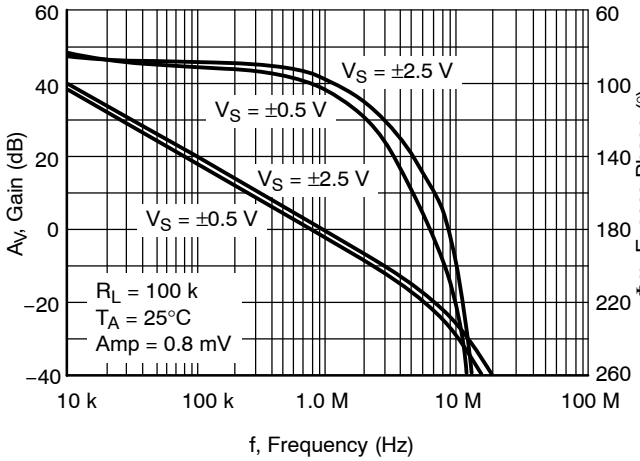


Figure 20. Voltage Gain and Phase versus Frequency

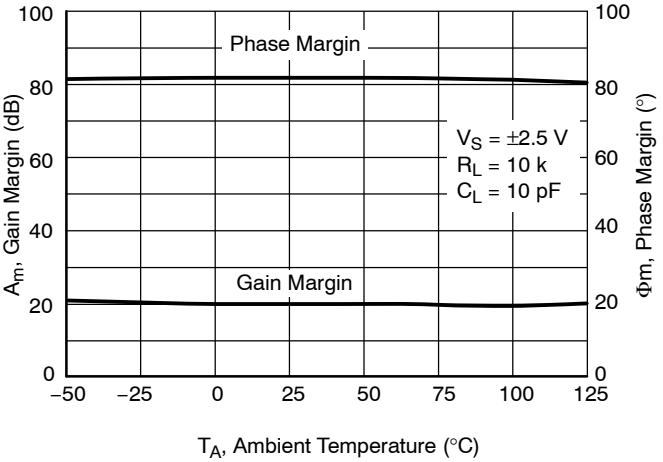


Figure 21. Gain and Phase Margin versus Temperature

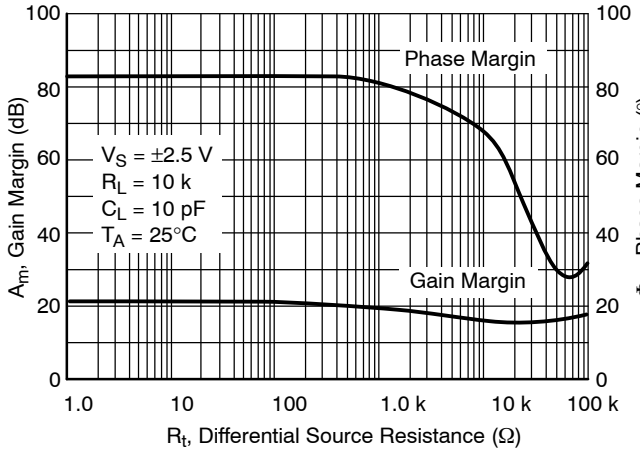


Figure 22. Gain and Phase Margin versus Differential Source Resistance

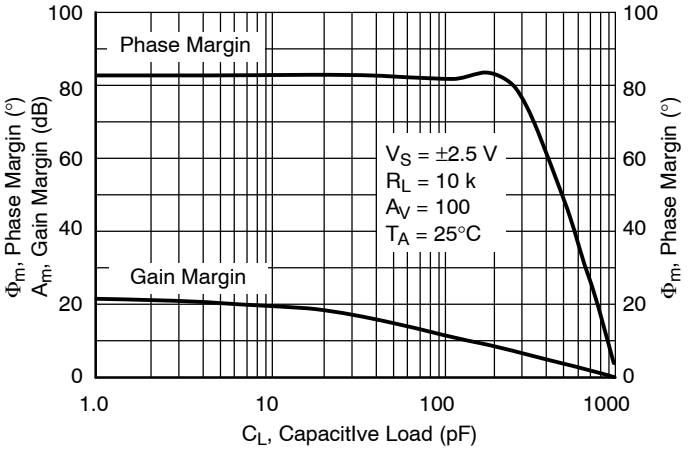


Figure 23. Gain and Phase Margin versus Output Load Capacitance

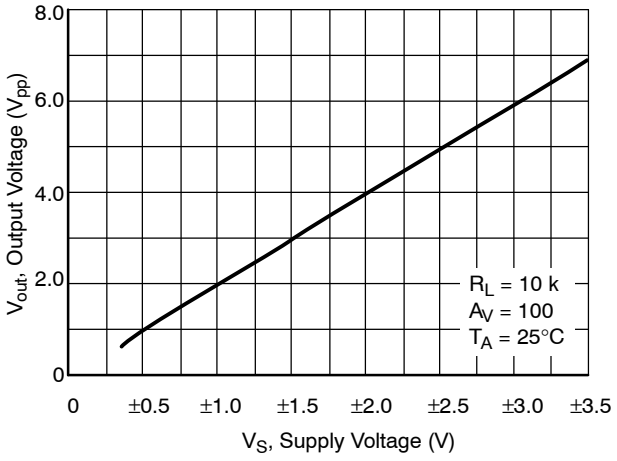


Figure 24. Output Voltage Swing versus Supply Voltage

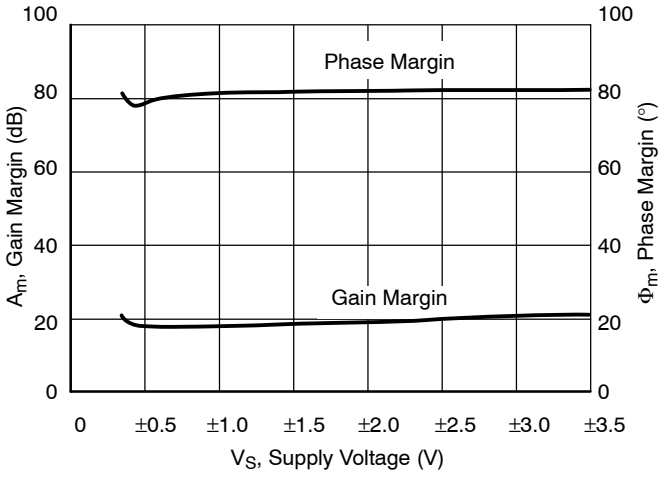


Figure 25. Gain and Phase Margin versus Supply Voltage

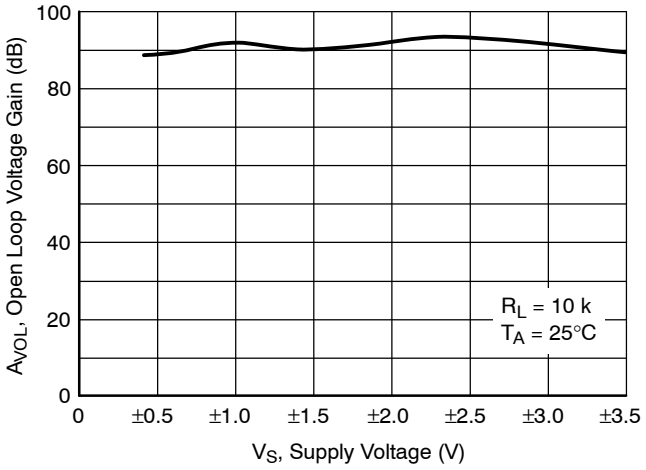


Figure 26. Open Loop Voltage Gain versus Supply Voltage

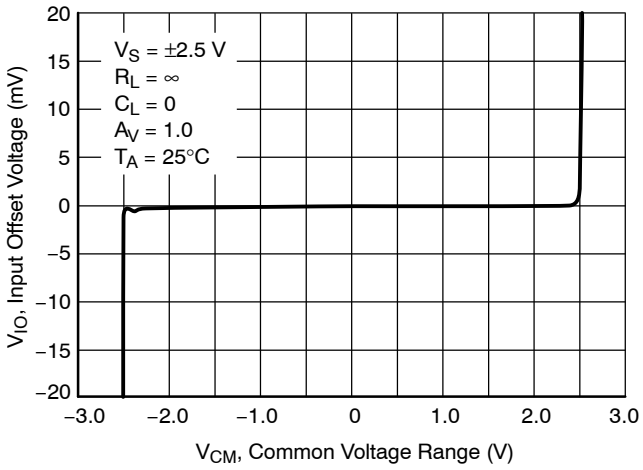


Figure 27. Input Offset Voltage versus Common Mode Input Voltage Range, V_S = ±2.5 V

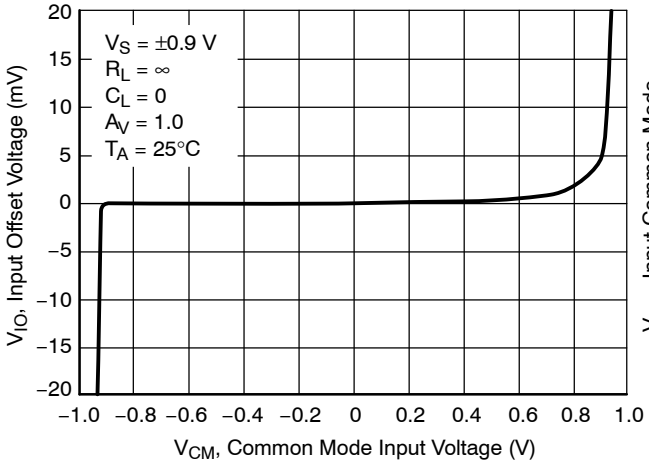


Figure 28. Input Offset Voltage versus Common Mode Input Voltage Range, V_S = ±0.9 V

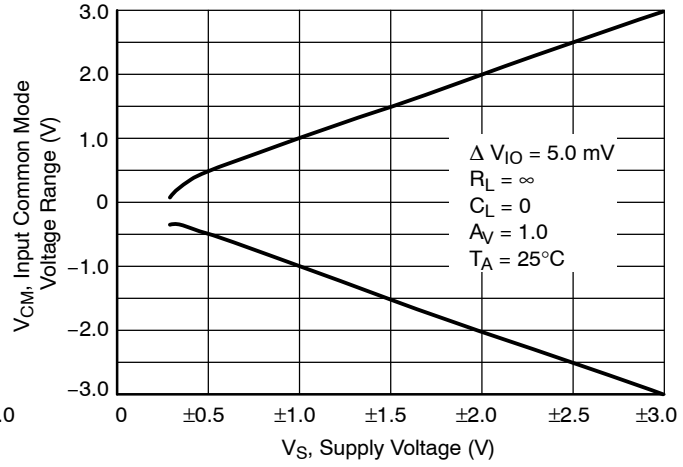


Figure 29. Common−Mode Input Voltage Range versus Power Supply Voltage

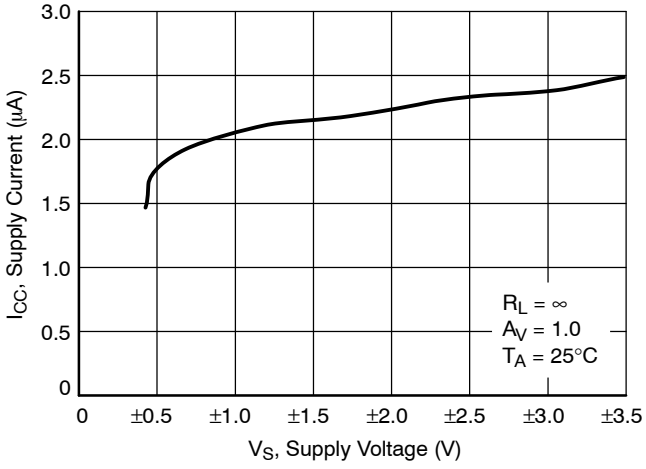


Figure 30. Supply Current versus Supply Voltage (Disabled)

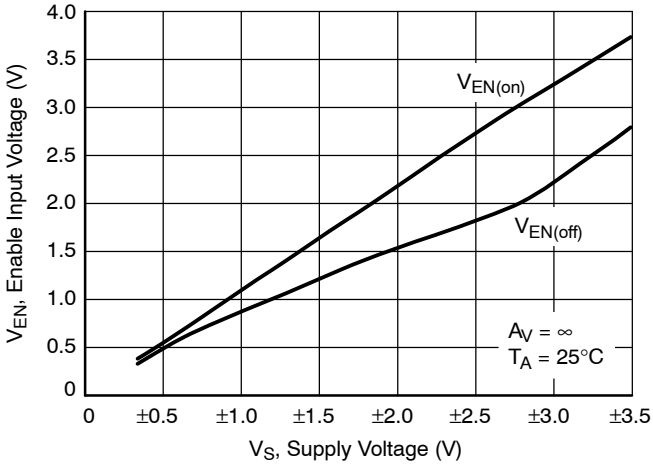


Figure 31. Enable Input Voltage versus Supply Voltage

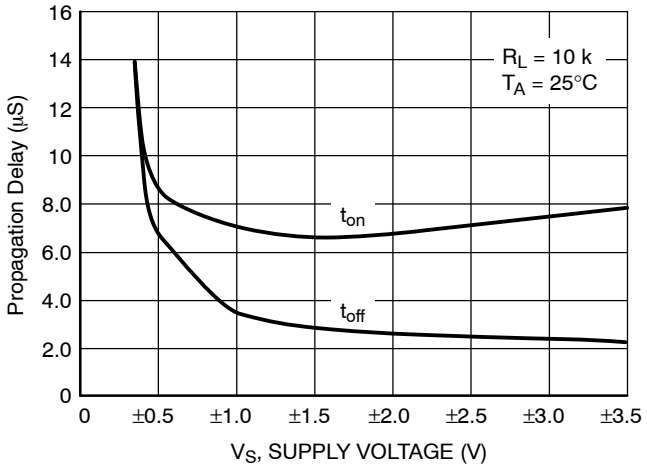


Figure 32. Propagation Delay versus Supply Voltage

APPLICATION INFORMATION AND OPERATING DESCRIPTION

GENERAL INFORMATION

The NCS2002 is an industry first rail−to−rail input, rail−to−rail output amplifier that features guaranteed sub one volt operation. This unique feature set is achieved with the use of a modified analog CMOS process that allows the implementation of depletion MOSFET devices. The amplifier has a 1.0 MHz gain bandwidth product, 1.2 V/μs slew rate and is operational over a power supply range less than 0.9 V to as high as 7.0 V.

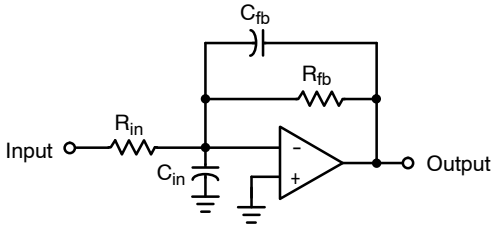
Inputs

The input topology chosen for this device series is unconventional when compared to most low voltage operational amplifiers. It consists of an N−channel depletion mode differential transistor pair that drives a folded cascade stage and current mirror. This configuration extends the input common mode voltage range to encompass the V_{EE} and V_{CC} power supply rails, even when powered from a combined total of less than 0.9 volts. Figures 27, 28 and 29 show the input common mode voltage range versus power supply voltage.

The differential input stage is laser trimmed in order to minimize offset voltage. The N−channel depletion mode MOSFET input stage exhibits an extremely low input bias current of less than 10 pA. The input bias current versus temperature is shown in Figure 4. Either one or both inputs can be biased as low as V_{EE} minus 300 mV to as high as 7.0 V without causing damage to the device. If the input common mode voltage range is exceeded, the output will not display a phase reversal. If the maximum input positive or negative voltage ratings are to be exceeded, a series resistor must be used to limit the input current to less than 2.0 mA.

The ultra low input bias current of the NCS2002 allows the use of extremely high value source and feedback resistor without reducing the amplifier's gain accuracy. These high value resistors, in conjunction with the device input and printed circuit board parasitic capacitances C_{in}, will add an additional pole to the single pole amplifier in Figure 33. If low enough in frequency, this additional pole can reduce the phase margin and significantly increase the output settling time. The effects of C_{in}, can be canceled by placing a zero into the feedback loop. This is accomplished with the addition of capacitor C_{fb}. An approximate value for C_{fb} can be calculated by:

$$C_{fb} = \frac{R_{in} \times C_{in}}{R_{fb}}$$



C_{in} = Input and printed circuit board capacitance

Figure 33. Input Capacitance Pole Cancellation

Output

The output stage consists of complementary P and N channel devices connected to provide rail−to−rail output drive. With a 2.0 k load, the output can swing within 50 mV of either rail. It is also capable of supplying over 75 mA when powered from 5.0 V and 1.0 mA when powered from 0.9 V.

When connected as a unity gain follower, the NCS2002 can directly drive capacitive loads in excess of 820 pF at room temperature without oscillating but with significantly reduced phase margin. The unity gain follower configuration exhibits the highest bandwidth and is most prone to oscillations when driving a high value capacitive load. The capacitive load in combination with the amplifier's output impedance, creates a phase lag that can result in an under−damped pulse response or a continuous oscillation. Figure 35 shows the effect of driving a large capacitive load in a voltage follower type of setup. When driving capacitive loads exceeding 820 pF, it is recommended to place a low value isolation resistor between the output of the op amp and the load, as shown in Figure 34. The series resistor isolates the capacitive load from the output and enhances the phase margin. Refer to Figure 36. Larger values of R will result in a cleaner output waveform but excessively large values will degrade the large signal rise and fall time and reduce the output amplitude. Depending upon the capacitor characteristics, the isolation resistor value will typically be between 50 to 500 Ω. The output drive capability for resistive and capacitive loads is shown in Figures 2, 3, and 23.

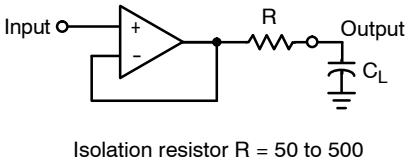


Figure 34. Capacitance Load Isolation

Note that the lowest phase margin is observed at cold temperature and low supply voltage.

Enable Pin

The enable pin allows the user to externally control the device. if the enable pin is pulled below the input disable threshold voltage (V_{EN} < 45% V_{CC}), the amplifier is disabled. Once the enable pin is taken above the threshold voltage (V_{EN} = 60% V_{CC}), the amplifier will turn on. In the event the enable pin is not connected, the amplifier will remain on by default

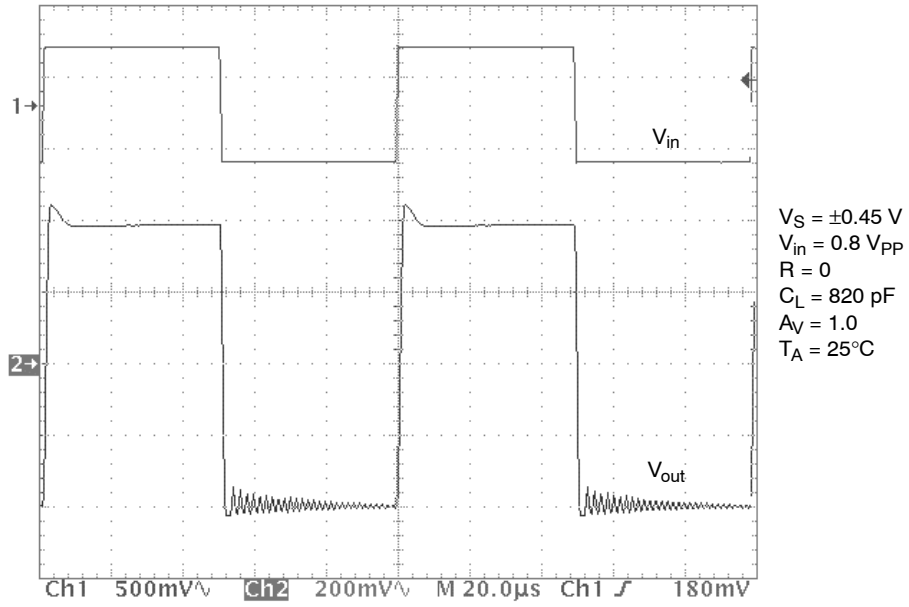


Figure 35. Small Signal Transient Response with Large Capacitive Load

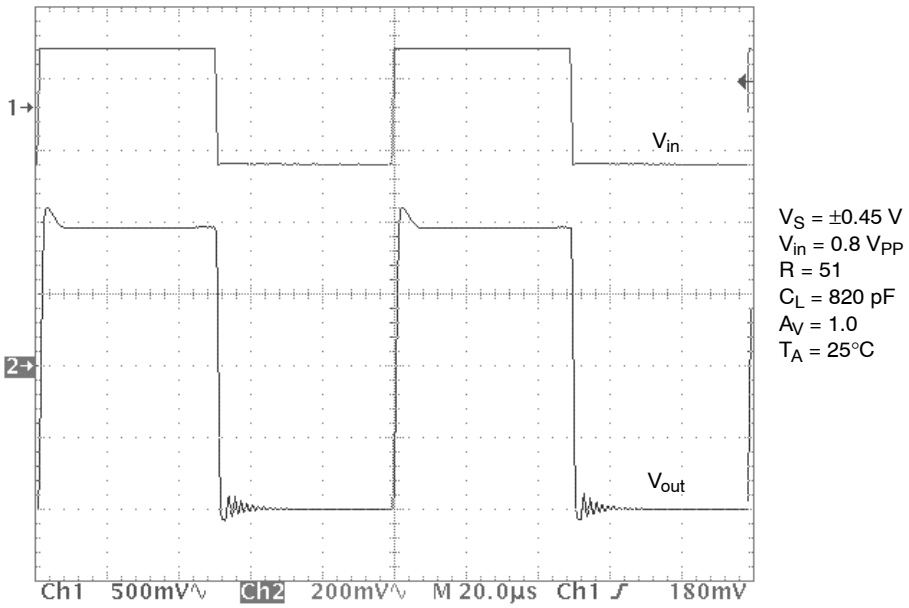
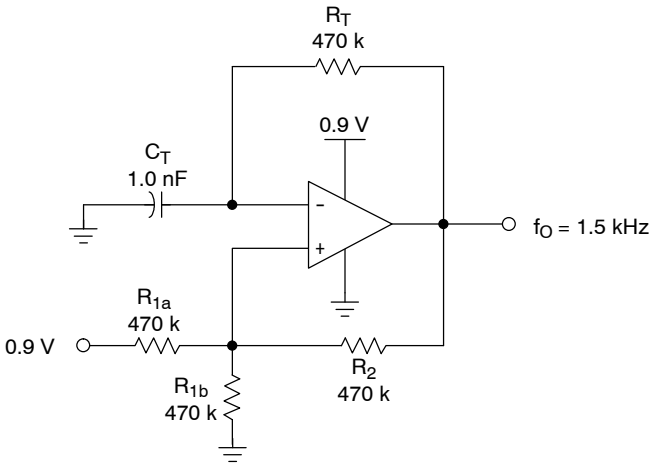
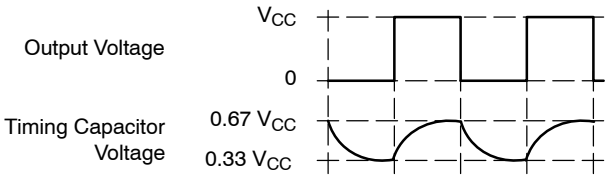


Figure 36. Small Signal Transient Response with Large Capacitive Load and Isolation Resistor.

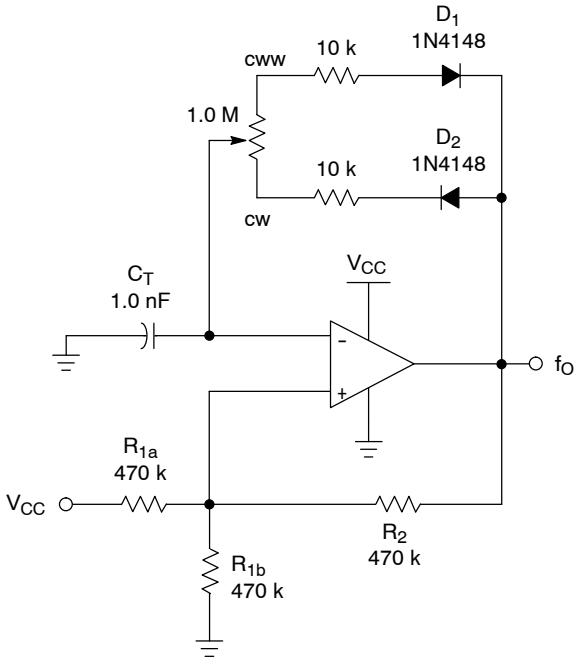


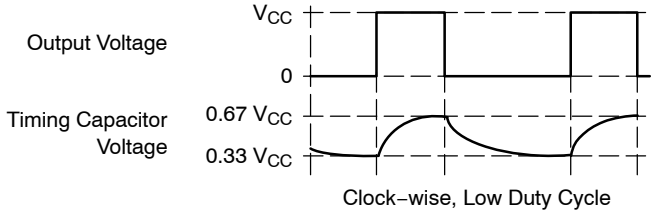


The non−inverting input threshold levels are set so that the capacitor voltage oscillates between 1/3 and 2/3 of V_{CC}. This requires the resistors R_{1a}, R_{1b} and R_2 to be of equal value. The following formula can be used to approximate the output frequency.

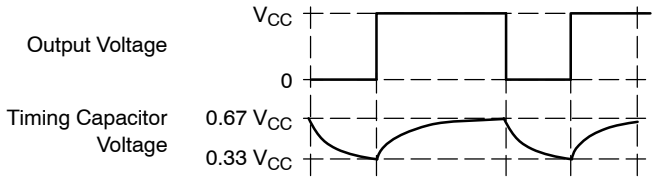
$$f_O = \frac{1}{1.39\ R_T C_T}$$

Figure 37. 0.9 V Square Wave Oscillator





Clock−wise, Low Duty Cycle



Counter−Clock−wise, High Duty Cycle

The timing capacitor C_T will charge through diode D_2 and discharge through diode D_1, allowing a variable duty cycle. The pulse width of the signal can be programmed by adjusting the value of the trimpot. The capacitor voltage will oscillate between 1/3 and 2/3 of V_{CC}, since all the resistors at the non−inverting input are of equal value.

Figure 38. Variable Duty Cycle Pulse Generator

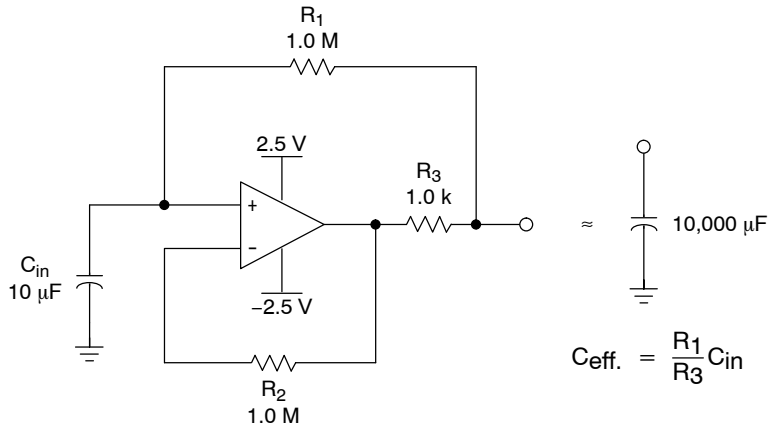


Figure 39. Positive Capacitance Multiplier

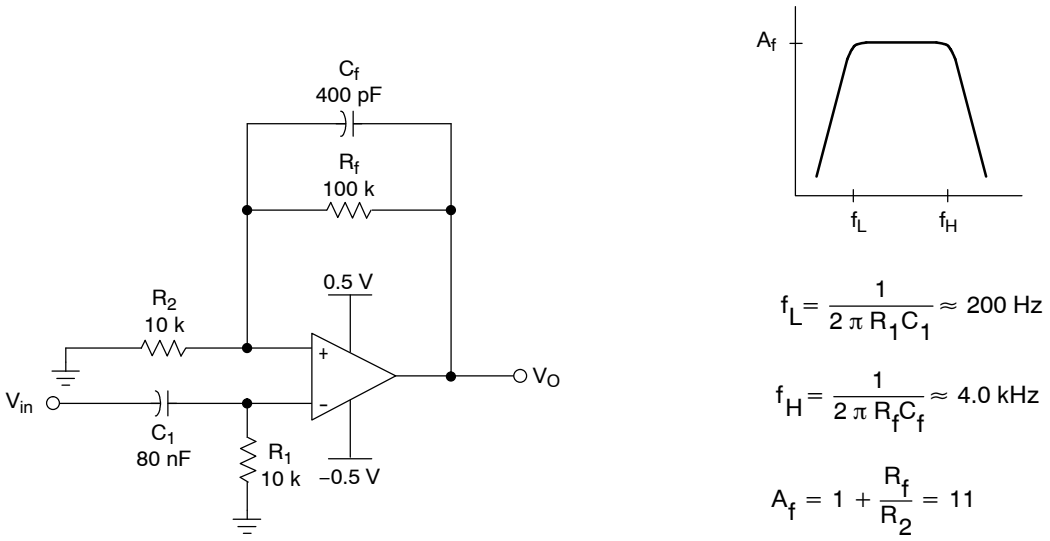


Figure 40. 1.0 V Voiceband Filter

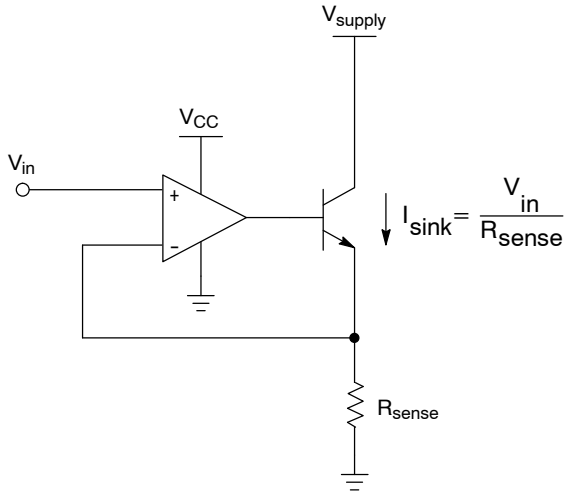
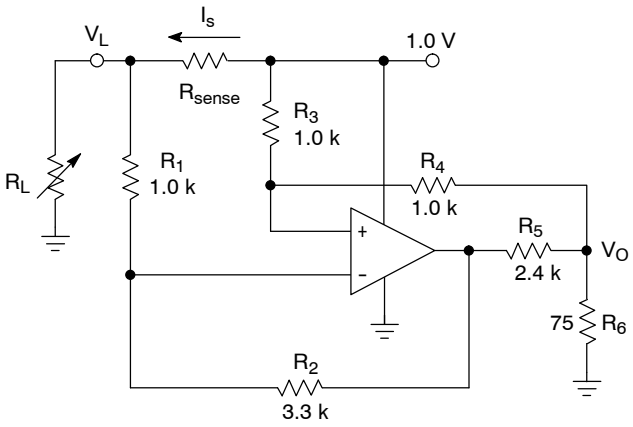


Figure 41. High Compliance Current Sink



I_s	V_O
435 mA	34.7 mV
212 mA	36.9 mV

For best performance, use low tolerance resistors.

Figure 42. High Side Current Sense

ORDERING INFORMATION1

Device	Marking	Package	Shipping†
NCS2002SN1T1G	P	TSOP−6 (Pb−Free)	3000 / Tape & Reel
NCS2002SN2T1G	Q		
NCV2002SN1T1G	P		
NCV2002SN2T1G	Q		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

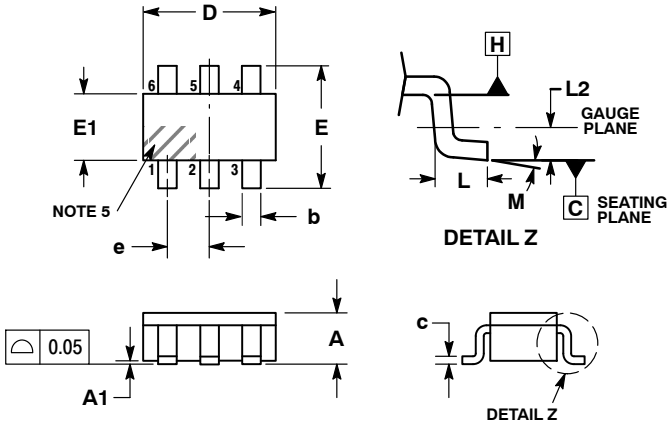
*NCV2002: T_{low} = −40°C, T_{high} = +125°C. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control. AEC−Q100 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 2:1

TSOP−6
CASE 318G−02
ISSUE V

DATE 12 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	–	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

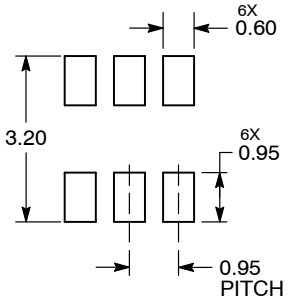
STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

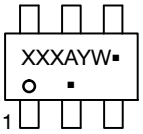
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

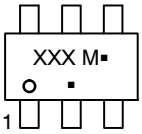
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



STANDARD

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASB14888C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSOP−6**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales