

74AC1181

Arithmetic Logic Units/Function Generators

The 'AC1181 is an arithmetic logic unit (ALU)/function generator that has a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade outputs \overline{G} and \overline{P} for the four bits in the package. When used in conjunction with the 'AC11882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The method of cascading 'AC11882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

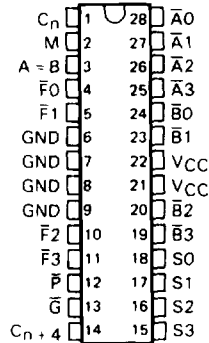
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54AC11181, 74AC11181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

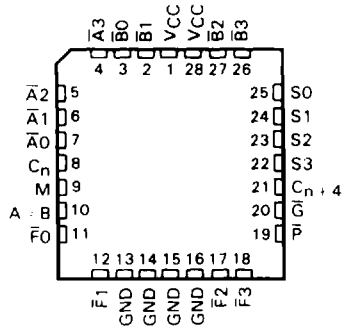
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- Flow-Through Architecture to Optimize PCB Layout
- Center-Pin VCC and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:
 - Addition
 - Subtraction
 - Shift Operand A One Position
 - Magnitude Comparison
 - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
 - Exclusive-OR
 - Comparator
 - AND, NAND, OR, NOR
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

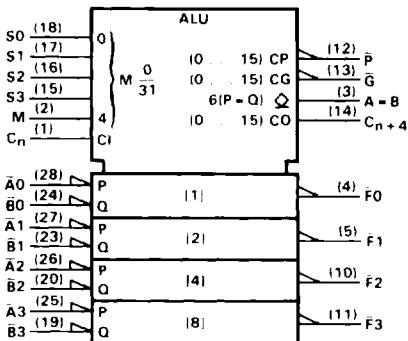
**54AC11181 ... JT PACKAGE
74AC11181 ... DW OR NT PACKAGE
(TOP VIEW)**



**54AC11181 ... FK PACKAGE
(TOP VIEW)**



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

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54AC11181, 74AC11181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

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signal designations

In both Figures 1 and 2, the polarity indicators (∇) indicate that the associated input or output is active-low with respect to the function shown inside the symbol, and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data and should be used with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'AC11181 and 'AC11881 together with the 'AC11882 can be used with the signal designation of either Figure 1 or Figure 2.

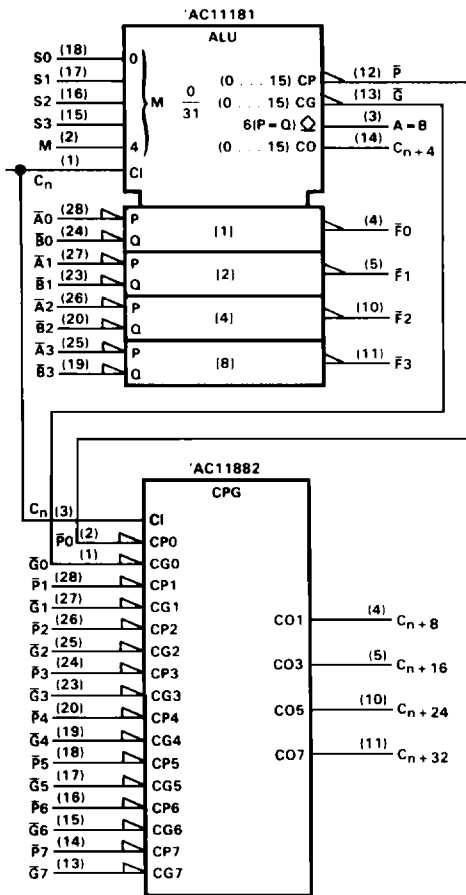


FIGURE 1
(USE WITH TABLE 1)

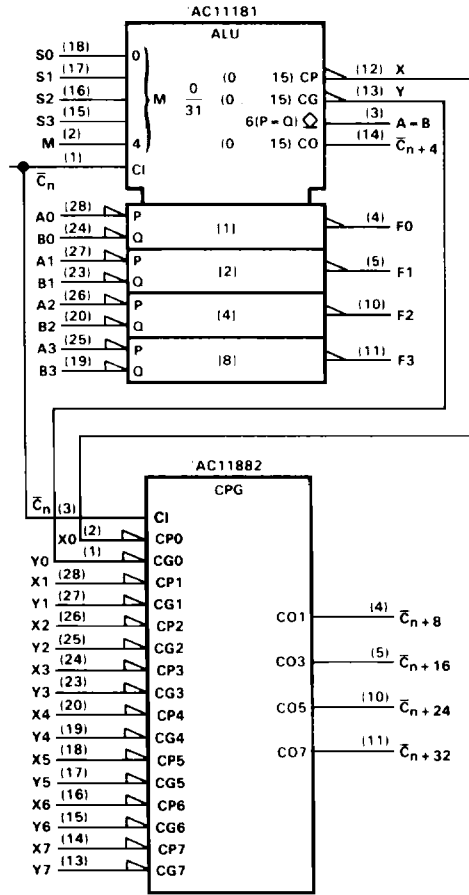


FIGURE 2
(USE WITH TABLE 2)

Pin numbers shown are for DW, JT, and NT packages.



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54AC11181, 74AC11181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

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description

The 'AC11181 is an arithmetic logic unit (ALU)/function generator that has a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade outputs \bar{C} and \bar{P} for the four bits in the package. When used in conjunction with the 'AC11882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The method of cascading 'AC11882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 'AC11181 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PACKAGE	PIN NUMBERS AND DESIGNATIONS															
DW, JT, or NT FK	25 4	26 5	27 6	28 7	19 26	20 27	23 2	24 3	11 18	10 17	5 12	4 11	1 8	14 2	12 19	13 20
Active-low data (Table 1)	$\bar{A}3$	$\bar{A}2$	$\bar{A}1$	$\bar{A}0$	$\bar{B}3$	$\bar{B}2$	$\bar{B}1$	$\bar{B}0$	$\bar{F}3$	$\bar{F}2$	$\bar{F}1$	$\bar{F}0$	C_n	C_{n+4}	\bar{P}	\bar{C}
Active-high data (Table 2)	A3	A2	A1	A0	B3	B2	B1	B0	F3	F2	F1	F0	\bar{C}_n	\bar{C}_{n+4}	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is $A \oplus B - 1$, which requires an end-around or forced carry to provide $A - B$.

The 'AC11181 can also be used as a comparator. The $A = B$ output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality ($A = B$). When performing this comparison, the ALU must be in the subtract mode with $C_n = H$. The $A = B$ output is open drain so that it can be wired-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	$A < B$	$A < B$
H	L	$A = B$	$A = B$
L	H	$A > B$	$A < B$
L	L	$A > B$	$A > B$

These circuits have been designed not only to incorporate all of the designer's requirements for arithmetic operations but also to provide 16 possible functions of two Boolean variables without using external circuitry. These logic functions are selected using the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR and OR functions.

54AC11181, 74AC11181
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

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TABLE 1

SELECTION				ACTIVE-LOW DATA		
				M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0		C _n = L (no carry)	C _n = H (with carry)
L	L	L	L	$F = \bar{A}$	F = A MINUS 1	F = A
L	L	L	H	$F = \bar{A}\bar{B}$	F = AB MINUS 1	F = AB
L	L	H	L	$F = \bar{A} + B$	F = $\bar{A}\bar{B}$ MINUS 1	F = $\bar{A}\bar{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \overline{A + B}$	F = A PLUS (A + \bar{B})	F = A PLUS (A + \bar{B}) PLUS 1
L	H	L	H	$F = \bar{B}$	F = AB PLUS (A + \bar{B})	F = AB PLUS (A + \bar{B}) PLUS 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A + \bar{B}$	F = A + \bar{B}	F = (A + \bar{B}) PLUS 1
H	L	L	L	$F = \bar{A}\bar{B}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A \oplus B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = $\bar{A}\bar{B}$ PLUS (A + B)	F = $\bar{A}\bar{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A [†]	F = A PLUS A PLUS 1
H	H	L	H	$F = \bar{A}\bar{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = $\bar{A}\bar{B}$ PLUS A	F = $\bar{A}\bar{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0		C _n = H (no carry)	C _n = L (with carry)
L	L	L	L	$F = \bar{A}$	F = A	F = A PLUS 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	$F = \bar{A}\bar{B}$	F = A + \bar{B}	F = (A + \bar{B}) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \bar{A}\bar{B}$	F = A PLUS $\bar{A}\bar{B}$	F = A PLUS $\bar{A}\bar{B}$ PLUS 1
L	H	L	H	$F = \bar{B}$	F = (A + B) PLUS $\bar{A}\bar{B}$	F = (A + B) PLUS $\bar{A}\bar{B}$ PLUS 1
L	H	H	L	F = A \oplus B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = \bar{A}\bar{B}$	F = $\bar{A}\bar{B}$ MINUS 1	F = $\bar{A}\bar{B}$
H	L	L	L	$F = \bar{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + \bar{B}) PLUS AB	F = (A + \bar{B}) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A [†]	F = A PLUS A PLUS 1
H	H	L	H	$F = A + \bar{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + \bar{B}) PLUS A	F = (A + \bar{B}) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

[†] Each bit is shifted to the next more significant position.

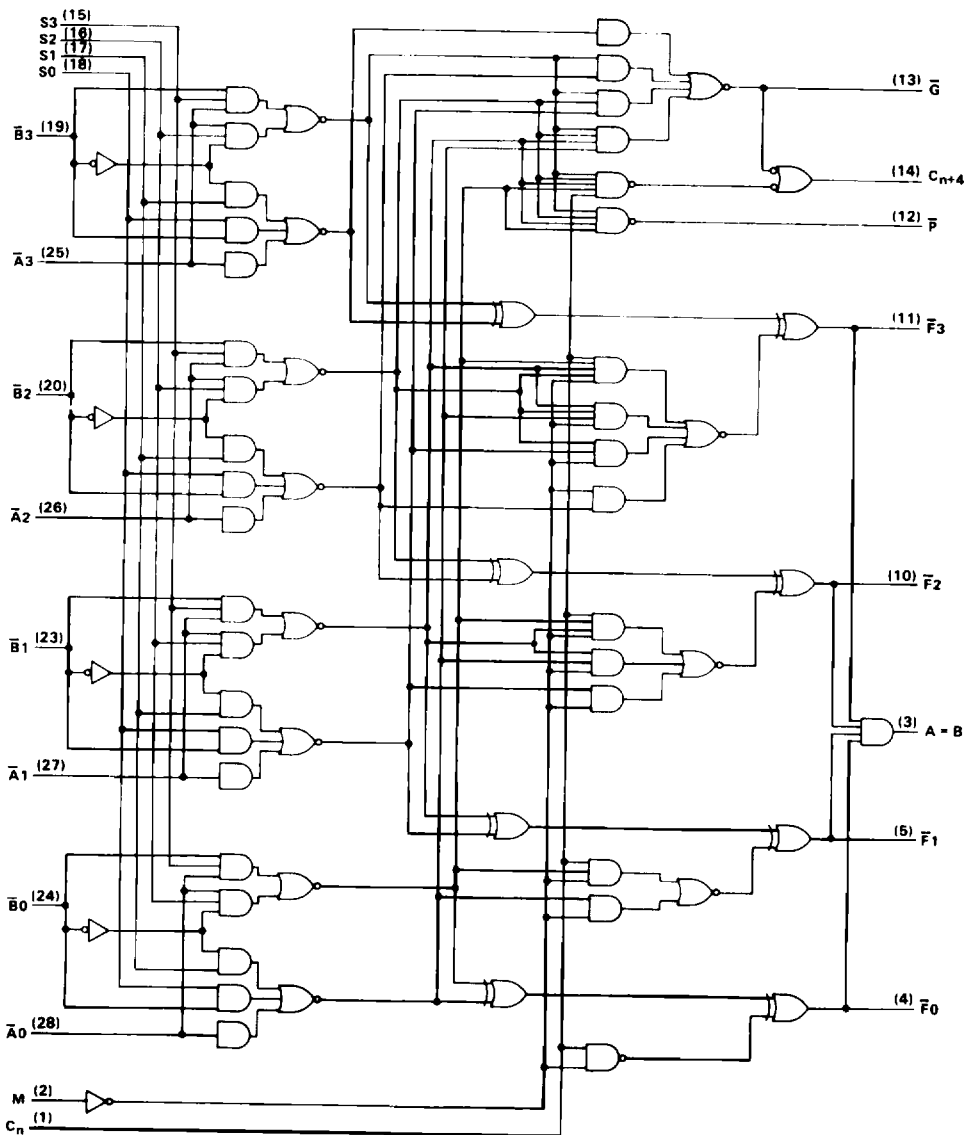


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54AC11181, 74AC11181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

D3119, APRIL 1989—REVISED MARCH 1990—T10184

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

54AC11181, 74AC11181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54AC11181			74AC11181			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V_{CC}	Supply voltage	3	5	5.5	3	5	5.5	V	
V_{IH}	High-level input voltage	$V_{CC} = 3$ V		2.1	$V_{CC} = 3$ V		2.1	V	
		$V_{CC} = 4.5$ V		3.15	$V_{CC} = 4.5$ V		3.15		
		$V_{CC} = 5.5$ V		3.85	$V_{CC} = 5.5$ V		3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V		0.9	$V_{CC} = 3$ V		0.9	V	
		$V_{CC} = 4.5$ V		1.35	$V_{CC} = 4.5$ V		1.35		
		$V_{CC} = 5.5$ V		1.65	$V_{CC} = 5.5$ V		1.65		
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V	
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V	
I_{OH}	High-level output current	All outputs except A = B	$V_{CC} = 3$ V		-4	$V_{CC} = 3$ V		-4	mA
			$V_{CC} = 4.5$ V		-24	$V_{CC} = 4.5$ V		-24	
			$V_{CC} = 5.5$ V		-24	$V_{CC} = 5.5$ V		-24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V		12	$V_{CC} = 3$ V		12	mA	
		$V_{CC} = 4.5$ V		24	$V_{CC} = 4.5$ V		24		
		$V_{CC} = 5.5$ V		24	$V_{CC} = 5.5$ V		24		
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V	
T_A	Operating free-air temperature	-55		125	-40		85	°C	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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54AC11181, 74AC11181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11521		74AC11521		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	Any output except A = B	I _{OH} = -50 μA	3 V	2.9			2.9		2.9	V	
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
			4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
I _{OH} = -50 mA [†]	5.5 V				3.85						
I _{OH} = -75 mA [†]	5.5 V						3.85				
I _{OH}	A = B	V _{CC} = 5.5 V, V _O = V _{CC}			0.5		10		5	μA	
V _{OL}		I _{OL} = 50 μA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
			4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
I _{OL} = 50 mA [†]	5.5 V					1.65					
I _{OL} = 75 mA [†]	5.5 V							1.65			
I _I		V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μA
C _i		V _I = V _{CC} or GND	5 V			4.5					pF
C _O	A = B	V _O = V _{CC} or GND	5 V			11					pF

[†] Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.

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**TEXAS
INSTRUMENTS**

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54AC11181, 74AC11181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 3)

SUM mode; $M = S1 = S2 = 0 \text{ V}$, $S0 = S3 = 4.5 \text{ V}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC11181		74AC11181		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	C_n	C_{n+4}	1.5	10.5	14.9	1.5	16.6	1.5	15.6	ns
t_{PHL}			1.5	8.1	11.6	1.5	16.8	1.5	15.1	
t_{PLH}	Any \bar{A}	C_{n+4}	1.5	13	18.5	1.5	21.1	1.5	19.7	ns
t_{PHL}			1.5	13.7	17.7	1.5	21.1	1.5	20.1	
t_{PLH}	Any \bar{B}	C_{n+4}	1.5	14.4	19.4	1.5	21.9	1.5	21.2	ns
t_{PHL}			1.5	13.5	17.6	1.5	21	1.5	19.8	
t_{PLH}	C_n	Any \bar{F}	1.5	13.2	21	1.5	24	1.5	22.4	ns
t_{PHL}			1.5	10.7	16.5	1.5	19.1	1.5	17.7	
t_{PLH}	Any \bar{A}	\bar{G}	1.5	14.2	19.6	1.5	21.7	1.5	21.3	ns
t_{PHL}			1.5	10.9	14.5	1.5	20.4	1.5	18.7	
t_{PLH}	Any \bar{B}	\bar{G}	1.5	13.8	19.2	1.5	21.5	1.5	20.8	ns
t_{PHL}			1.5	11.6	14.7	1.5	20.1	1.5	17.1	
t_{PLH}	Any \bar{A}	\bar{P}	1.5	12.6	15.9	1.5	19.1	1.5	17.6	ns
t_{PHL}			1.5	9.6	12.3	1.5	14.4	1.5	13.3	
t_{PLH}	Any \bar{B}	\bar{P}	1.5	12.4	15.7	1.5	18.7	1.5	17.2	ns
t_{PHL}			1.5	10.2	13.2	1.5	15.6	1.5	14.4	
t_{PLH}	\bar{A}_i	\bar{F}_i	1.5	14.4	18.4	1.5	21	1.5	19.7	ns
t_{PHL}			1.5	11.8	14.6	1.5	17.7	1.5	16.2	
t_{PLH}	\bar{B}_i	\bar{F}_i	1.5	13.7	17.7	1.5	21.2	1.5	19.4	ns
t_{PHL}			1.5	12.7	15.4	1.5	18.9	1.5	17.1	
t_{PLH}	\bar{A}_i	Any \bar{F} except \bar{F}_i	1.5	16.2	21.7	1.5	25.6	1.5	23.7	ns
t_{PHL}			1.5	13.9	18.4	1.5	22.6	1.5	20.7	
t_{PLH}	\bar{B}_i	Any \bar{F} except \bar{F}_i	1.5	16	21.5	1.5	25.6	1.5	23.6	ns
t_{PHL}			1.5	14.4	19.1	1.5	22.9	1.5	21.1	

mode switching; $S1 = S2 = 0 \text{ V}$, $S0 = S3 = 4.5 \text{ V}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC11181		74AC11181		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	M	Any \bar{F}	1.5	10.3	13.2	1.5	15.7	1.5	14.5	ns
t_{PHL}			1.5	9.2	11.2	1.5	13.6	1.5	12.2	
t_{PLH}	M	A = B	1.5	16.6	20.7	1.5	22.3	1.5	21.6	ns
t_{PHL}			1.5	12.2	14.8	1.5	19.4	1.5	17.1	

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54AC11181, 74AC11181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

D3119, APRIL 1989—REVISED MARCH 1990—TI0184

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 3)

DIFF mode; $M = S_0 = S_3 = 0 \text{ V}$, $S_1 = S_2 = 4.5 \text{ V}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC11181		74AC11181		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	C_n	C_{n+4}	1.5	10.5	14.9	1.5	16.6	1.5	15.6	ns
t_{PHL}			1.5	8.1	11.6	1.5	16.8	1.5	15.1	
t_{PLH}	Any \bar{A}	C_{n+4}	1.5	13.5	18.7	1.5	21.2	1.5	19.9	ns
t_{PHL}			1.5	13.6	17.9	1.5	21.8	1.5	20.6	
t_{PLH}	Any \bar{B}	C_{n+4}	1.5	15.4	20.3	1.5	22.4	1.5	21.8	ns
t_{PHL}			1.5	14	18.3	1.5	21.4	1.5	20.4	
t_{PLH}	C_n	Any \bar{F}	1.5	13.2	21	1.5	24	1.5	22.4	ns
t_{PHL}			1.5	10.7	16.5	1.5	19.1	1.5	17.7	
t_{PLH}	Any \bar{A}	\bar{G}	1.5	14.1	19.7	1.5	21.9	1.5	21.3	ns
t_{PHL}			1.5	10.8	14.6	1.5	19.3	1.5	17.4	
t_{PLH}	Any \bar{B}	\bar{G}	1.5	14.5	20	1.5	19.8	1.5	21.3	ns
t_{PHL}			1.5	12.4	15.7	1.5	21	1.5	18.9	
t_{PLH}	Any \bar{A}	\bar{P}	1.5	12.8	16.4	1.5	19.5	1.5	18	ns
t_{PHL}			1.5	9.9	12.5	1.5	14.6	1.5	13.5	
t_{PLH}	Any \bar{B}	\bar{P}	1.5	13.1	16.4	1.5	19.4	1.5	17.9	ns
t_{PHL}			1.5	11.2	14.1	1.5	16.9	1.5	15.6	
t_{PLH}	\bar{A}_i	\bar{F}_i	1.5	14.7	18.8	1.5	21.4	1.5	20.1	ns
t_{PHL}			1.5	11.9	14.9	1.5	17.6	1.5	16.1	
t_{PLH}	\bar{B}_i	\bar{F}_i	1.5	14.5	18.3	1.5	21.2	1.5	19.9	ns
t_{PHL}			1.5	13.5	16.2	1.5	20.2	1.5	18.4	
t_{PLH}	\bar{A}_i	Any \bar{F} except \bar{F}_i	1.5	16.4	22	1.5	26	1.5	24	ns
t_{PHL}			1.5	14.1	18.8	1.5	22.7	1.5	20.8	
t_{PLH}	\bar{B}_i	Any \bar{F} except \bar{F}_i	1.5	16.5	22.2	1.5	26.3	1.5	24.2	ns
t_{PHL}			1.5	15.3	19.8	1.5	23.7	1.5	21.6	
t_{PLH}	Any \bar{A}	A B	1.5	20.6	25.1	1.5	28.2	1.5	27.5	ns
t_{PHL}			1.5	15	18.2	1.5	23.2	1.5	21.5	
t_{PLH}	Any \bar{B}	A B	1.5	20.4	25	1.5	27.5	1.5	27	ns
t_{PHL}			1.5	16.7	19.7	1.5	24.6	1.5	22.1	

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**TEXAS
 INSTRUMENTS**

POST OFFICE BOX 655303 - DALLAS, TEXAS 75265

54AC11181, 74AC11181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

TI0184—D3119, APRIL 1989—REVISED MARCH 1990

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 3)**

LOGIC and ARITH modes

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			54AC11181		74AC11181		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	Any \bar{A}	Any \bar{F}	M = 4.5 V (LOGIC mode)	1.5	11.5	15.2	1.5	18	1.5	16.6	ns
t _{PHL}				1.5	12.2	15	1.5	18.7	1.5	16.6	
t _{PLH}	\bar{B}_i	\bar{F}_i	M = 4.5 V (LOGIC mode)	1.5	14.7	18.9	1.5	21.4	1.5	20.4	ns
t _{PHL}				1.5	13.3	16.5	1.5	19.7	1.5	18.2	
t _{PLH}	Any S	Any \bar{F}	M = 0 V, (ARITH mode)	1.5	16.1	20.5	1.5	22	1.5	21.2	ns
t _{PHL}				1.5	12.5	15.1	1.5	18.8	1.5	17.3	
t _{PLH}	Any S	A - B	M = 0 V, (ARITH mode)	1.5	22.8	27.1	1.5	31.1	1.5	29.5	ns
t _{PHL}				1.5	16	19	1.5	23.7	1.5	21.2	
t _{PLH}	Any S	C _n + 4	M = 4.5 V, (LOGIC mode)	1.5	14.9	20.3	1.5	23.7	1.5	21.4	ns
t _{PHL}				1.5	17	24	1.5	29.7	1.5	26.5	
t _{PLH}	Any S	\bar{G}	M = 0 V, (ARITH mode)	1.5	15.7	21.6	1.5	25.8	1.5	23.6	ns
t _{PHL}				1.5	12.6	17.8	1.5	24.2	1.5	21.3	
t _{PLH}	Any S	\bar{P}	M = 4.5 V, (LOGIC mode)	1.5	16.7	20	1.5	24.7	1.5	22.4	ns
t _{PHL}				1.5	12	15.5	1.5	19.5	1.5	17.6	

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POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

54AC11181, 74AC11181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

D3119, APRIL 1989—REVISED MARCH 1990—TI0184

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 3)

SUM mode; $M = S1 = S2 = 0\text{ V}$, $S0 = S3 = 4.5\text{ V}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC11181		74AC11181		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	C _n	C _{n+4}	1.5	7.1	9.9	1.5	12.6	1.5	10.8	ns
t _{PHL}			1.5	7.5	11.4	1.5	16.8	1.5	14.7	
t _{PLH}	Any \bar{A}	C _{n+4}	1.5	9.6	14.3	1.5	15.6	1.5	14.5	ns
t _{PHL}			1.5	10	17.2	1.5	20.4	1.5	18.5	
t _{PLH}	Any \bar{B}	C _{n+4}	1.5	9.6	14.8	1.5	16.4	1.5	15.2	ns
t _{PHL}			1.5	10.6	17	1.5	20.4	1.5	18.5	
t _{PLH}	C _n	Any F	1.5	9.2	14	1.5	16	1.5	14.9	ns
t _{PHL}			1.5	8.3	13.1	1.5	15	1.5	14.1	
t _{PLH}	Any \bar{A}	\bar{G}	1.5	9.2	13.2	1.5	15.9	1.5	14.6	ns
t _{PHL}			1.5	8.3	14.3	1.5	18.5	1.5	16.3	
t _{PLH}	Any \bar{B}	\bar{G}	1.5	9.1	13	1.5	15.7	1.5	14.4	ns
t _{PHL}			1.5	8.8	13.6	1.5	18.7	1.5	16.7	
t _{PLH}	Any \bar{A}	\bar{P}	1.5	8.4	13.3	1.5	15	1.5	14.1	ns
t _{PHL}			1.5	7.7	10.7	1.5	13.6	1.5	11.8	
t _{PLH}	Any \bar{B}	\bar{P}	1.5	7.9	13	1.5	14.6	1.5	13.8	ns
t _{PHL}			1.5	8.3	10.7	1.5	13	1.5	11.7	
t _{PLH}	\bar{A}_i	F _i	1.5	9.5	14.3	1.5	16.7	1.5	15.5	ns
t _{PHL}			1.5	9.4	14.6	1.5	17.4	1.5	15.9	
t _{PLH}	\bar{B}_i	F _i	1.5	9.2	14	1.5	16.3	1.5	15.2	ns
t _{PHL}			1.5	10	15.3	1.5	17.5	1.5	16.7	
t _{PLH}	Any \bar{A}	Any F	1.5	10.8	14.1	1.5	16.6	1.5	15.4	ns
t _{PHL}			1.5	10.3	15.3	1.5	18.4	1.5	16.7	
t _{PLH}	Any \bar{B}	Any F	1.5	10.4	14.1	1.5	16.7	1.5	15.3	ns
t _{PHL}			1.5	10.7	15.6	1.5	18.7	1.5	17	

mode switching; $S1 = S2 = 0\text{ V}$, $S0 = S3 = 4.5\text{ V}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC11181		74AC11181		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	M	Any F	1.5	7.3	9.2	1.5	10.7	1.5	9.9	ns
t _{PHL}			1.5	8.3	11.2	1.5	13.5	1.5	12.1	
t _{PLH}	M	A = B	1.5	14.3	17.7	1.5	19.1	1.5	18.5	ns
t _{PHL}			1.5	11.7	14.8	1.5	19.4	1.5	17.1	

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**TEXAS
 INSTRUMENTS**

54AC11181, 74AC11181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

TI0184—D3119, APRIL 1989—REVISED MARCH 1990

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 3)**

DIFF mode; M = S0 = S3 = 0 V, S1 = S2 = 4.5 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54AC11181		74AC11181		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	C _n	C _{n+4}	1.5	7.1	9.9	1.5	12.6	1.5	10.8	ns
t _{PHL}			1.5	7.5	11.4	1.5	16.8	1.5	14.7	
t _{PLH}	Any \bar{A}	C _{n+4}	1.5	9.5	14.6	1.5	15.7	1.5	14.8	ns
t _{PHL}			1.5	10.5	17.3	1.5	21.2	1.5	19.1	
t _{PLH}	Any \bar{B}	C _{n+4}	1.5	10.5	15.4	1.5	17.3	1.5	16	ns
t _{PHL}			1.5	11.3	17.4	1.5	21	1.5	19	
t _{PLH}	C _n	Any \bar{F}	1.5	9.2	14	1.5	16	1.5	14.9	ns
t _{PHL}			1.5	8.3	13.1	1.5	15	1.5	14.1	
t _{PLH}	Any \bar{A}	\bar{G}	1.5	9.1	13.4	1.5	16	1.5	14.7	ns
t _{PHL}			1.5	8.4	14.6	1.5	18.1	1.5	16.2	
t _{PLH}	Any \bar{B}	\bar{G}	1.5	9.6	13.8	1.5	16.3	1.5	15	ns
t _{PHL}			1.5	9.5	14.2	1.5	19	1.5	17.3	
t _{PLH}	Any \bar{A}	\bar{P}	1.5	8.7	13.4	1.5	15.1	1.5	14.2	ns
t _{PHL}			1.5	8	10.2	1.5	12.6	1.5	11.2	
t _{PLH}	Any \bar{B}	\bar{P}	1.5	8.6	13.3	1.5	14.9	1.5	14.1	ns
t _{PHL}			1.5	8.8	11.3	1.5	14.2	1.5	12.7	
t _{PLH}	\bar{A}_i	\bar{F}_i	1.5	9.7	14.5	1.5	16.9	1.5	15.7	ns
t _{PHL}			1.5	9.7	14.5	1.5	17.3	1.5	15.8	
t _{PLH}	\bar{B}_i	\bar{F}_i	1.5	9.4	14.4	1.5	16.7	1.5	15.5	ns
t _{PHL}			1.5	10.8	16	1.5	18.8	1.5	17.2	
t _{PLH}	Any \bar{A}	Any \bar{F}	1.5	11	14.3	1.5	16.8	1.5	15.6	ns
t _{PHL}			1.5	10.5	15.5	1.5	18.4	1.5	16.7	
t _{PLH}	Any \bar{B}	Any \bar{F}	1.5	10.9	14.3	1.5	17	1.5	15.7	ns
t _{PHL}			1.5	11.2	15.3	1.5	19.2	1.5	17.5	
t _{PLH}	Any \bar{A}	A · B	1.5	16.5	20.2	1.5	23.6	1.5	22.7	ns
t _{PHL}			1.5	12.8	16.4	1.5	23.2	1.5	21	
t _{PLH}	Any \bar{B}	A · B	1.5	16.3	20	1.5	23	1.5	22.1	ns
t _{PHL}			1.5	13.6	18.4	1.5	24.6	1.5	21.2	

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**TEXAS
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54AC11181, 74AC11181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

D3119, APRIL 1989—REVISED MARCH 1990—TI0184

switching characteristics over recommended operating free-air temperature range,
VCC = 5 V ± 0.5 V (unless otherwise noted) (see Figure 3)

LOGIC and ARITH modes

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TA = 25°C			54AC11181		74AC11181		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
IPLH	Any \bar{A}	Any \bar{F}	M = 4.5 V (LOGIC mode)	1.5	7.6	11.7	1.5	13.8	1.5	12.7	ns
IPHL				1.5	9.8	15	1.5	17.8	1.5	16.1	
IPLH	Bi	Fi	M = 4.5 V (LOGIC mode)	1.5	9.8	14.5	1.5	16.6	1.5	15.5	ns
IPHL				1.5	10.5	15.6	1.5	18.1	1.5	17.2	
IPLH	Any S	Any \bar{F}	M = 0 V, (ARITH mode)	1.5	10.6	13.9	1.5	16.5	1.5	15.2	ns
IPHL				1.5	9.8	12.7	1.5	17.8	1.5	16	
IPLH	Any S	A - B	M = 0 V, (ARITH mode)	1.5	17.7	21.4	1.5	23.7	1.5	22.7	ns
IPHL				1.5	12.3	19	1.5	23.7	1.5	20.9	
IPLH	Any S	Cn 1 4	M = 4.5 V, (LOGIC mode)	1.5	9.9	14.3	1.5	16.6	1.5	15.4	ns
IPHL				1.5	11.6	21	1.5	26.3	1.5	23.3	
IPLH	Any S	\bar{G}	M = 0 V, (ARITH mode)	1.5	10.1	14.4	1.5	17.7	1.5	16	ns
IPHL				1.5	9	15.2	1.5	19.8	1.5	18.4	
IPLH	Any S	\bar{P}	M = 4.5 V, (LOGIC mode)	1.5	10.8	14.8	1.5	18.2	1.5	16.4	ns
IPHL				1.5	9	11.5	1.5	16.4	1.5	14.3	

operating characteristics, VCC = 5 V, TA = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
Cpd Power dissipation capacitance	CL = 50 pF, f = 1 MHz	119	pF

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54AC11181, 74AC11181
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

TI0184—D3119, APRIL 1989—REVISED MARCH 1990

PARAMETER MEASUREMENT INFORMATION

SUM MODE TEST TABLE
FUNCTION INPUTS: M = S1 = S2 = 0 V, S0 = S2 = 4.5 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE FIGURE 3)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
tPLH	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} and \bar{B}	C_n	F_i	In-Phase
tPHL				Remaining \bar{A} and \bar{B}			
tPLH	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A} and \bar{B}	C_n	\bar{F}_i	In-Phase
tPHL				Remaining \bar{A} and \bar{B}			
tPLH	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	In-Phase
tPHL				Remaining \bar{A} and \bar{B} , C_n			
tPLH	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	In-Phase
tPHL				Remaining \bar{A} and \bar{B} , C_n			
tPLH	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	\bar{G}	In-Phase
tPHL				Remaining \bar{B}			
tPLH	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	\bar{G}	In-Phase
tPHL				Remaining \bar{B}			
tPLH	C_n	None	None	All \bar{A}	All \bar{B}	Any \bar{F} or $C_n + 4$	In-Phase
tPHL				All \bar{A}			
tPLH	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	$C_n + 4$	Out-of-Phase
tPHL				Remaining \bar{B}			
tPLH	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	$C_n + 4$	Out-of-Phase
tPHL				Remaining \bar{B}			

MODE SWITCHING TEST TABLE
FUNCTION INPUTS: S1 = S2 = 0 V, S0 = S3 = 4.5 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE FIGURE 3)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
tPLH	M	—	—	Remaining \bar{A} and \bar{B}	$\bar{B}_2, \bar{A}_2, C_n$	Any \bar{F}	In-Phase
tPHL				Remaining \bar{A} and \bar{B}			
tPLH	M	—	—	Remaining \bar{A} and \bar{B}	$\bar{B}_1, \bar{A}_1, C_n$	A - B	In-Phase
tPHL				Remaining \bar{A} and \bar{B}			



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54AC11181, 74AC11181
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

D3119, APRIL 1989—REVISED MARCH 1990—T10184

PARAMETER MEASUREMENT INFORMATION

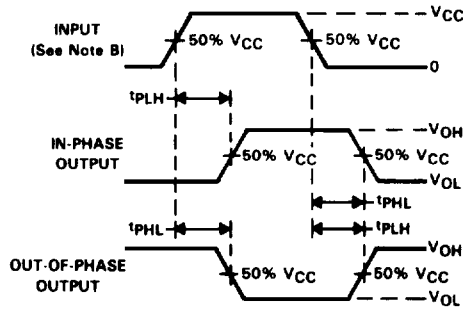
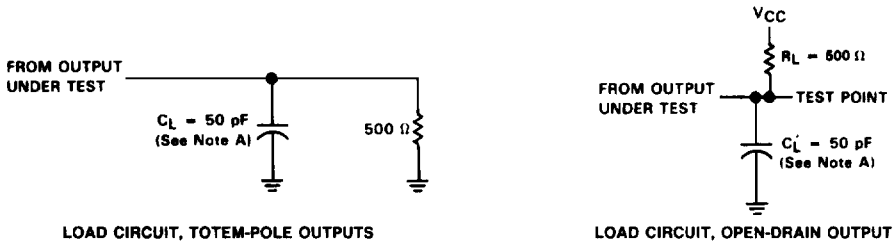
DIFF MODE TEST TABLE
FUNCTION INPUTS: M = S0 = S3 = 0 V, S1 = S2 = 4.5 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE FIGURE 3)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B}, C_n	F_i	In-Phase
t_{PHL}				Remaining \bar{A}	Remaining \bar{B}, C_n		
t_{PLH}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B}, C_n	F_i	Out-of-Phase
t_{PHL}				Remaining \bar{A}	Remaining \bar{B}, C_n		
t_{PLH}	\bar{A}_i	None	\bar{B}_i	None	Remaining \bar{A} and \bar{B}, C_n	F	In-Phase
t_{PHL}				None	Remaining \bar{A} and \bar{B}, C_n		
t_{PLH}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	F	Out-of-Phase
t_{PHL}				None	Remaining \bar{A} and \bar{B}, C_n		
t_{PLH}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	G	In-Phase
t_{PHL}				None	Remaining \bar{A} and \bar{B}, C_n		
t_{PLH}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B}, C_n	G	Out-of-Phase
t_{PHL}				None	Remaining \bar{A} and \bar{B}, C_n		
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B}, C_n	A = B	In-Phase
t_{PHL}				Remaining \bar{A}	Remaining \bar{B}, C_n		
t_{PLH}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B}, C_n	A = B	Out-of-Phase
t_{PHL}				Remaining \bar{A}	Remaining \bar{B}, C_n		
t_{PLH}	C_n	None	None	All \bar{A} and \bar{B}	None	$C_n + 4$ or any F	In-Phase
t_{PHL}				None	None		
t_{PLH}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	$C_n + 4$	Out-of-Phase
t_{PHL}				None	Remaining \bar{A} and \bar{B}, C_n		
t_{PLH}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B}, C_n	$C_n + 4$	In-Phase
t_{PHL}				None	Remaining \bar{A} and \bar{B}, C_n		

LOGIC MODE TEST TABLE
FUNCTION INPUTS: S0 = S3 = 0 V, S1 = S2 = M = 4.5 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE FIGURE 3)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	F_i	Out-of-Phase
t_{PHL}				None	Remaining \bar{A} and \bar{B}, C_n		
t_{PLH}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	F_i	Out-of-Phase
t_{PHL}				None	Remaining \bar{A} and \bar{B}, C_n		

PARAMETER MEASUREMENT INFORMATION



PROPAGATION DELAY TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
 For testing t_{max} and pulse duration: $t_r = 1$ to 3 ns, $t_f = 1$ to 3 ns.
 C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 3. LOAD CIRCUIT AND VOLTAGE WAVEFORMS