HFC0400

Fixed Frequency Flyback Controller with Ultra-low No Load Power Consumption

The Future of Analog IC Technology

DESCRIPTION

HFC0400 is a fixed-frequency current-mode controller with built-in slope compensation. It targets medium-power, off-line, flyback, switch-mode power supplies. At light loads, the controller freezes the peak current and reduces its switching frequency down to 25kHz to offer excellent light-load efficiency.

At very light loads, the controller enters burst mode to achieve very low standby power consumption.

HFC0400 offers frequency jittering to help dissipate energy generated by conducted noise.

HFC0400 also has an X-cap discharge function to discharge the X-cap when the input is unplugged.

HFC0400 features multiple protections that include thermal shutdown (TSD), VCC under-voltage lockout (UVLO), overload protection (OLP), over-voltage protection (OVP), and brown-out protection.

HFC0400 is available in an SOIC8-7A package.

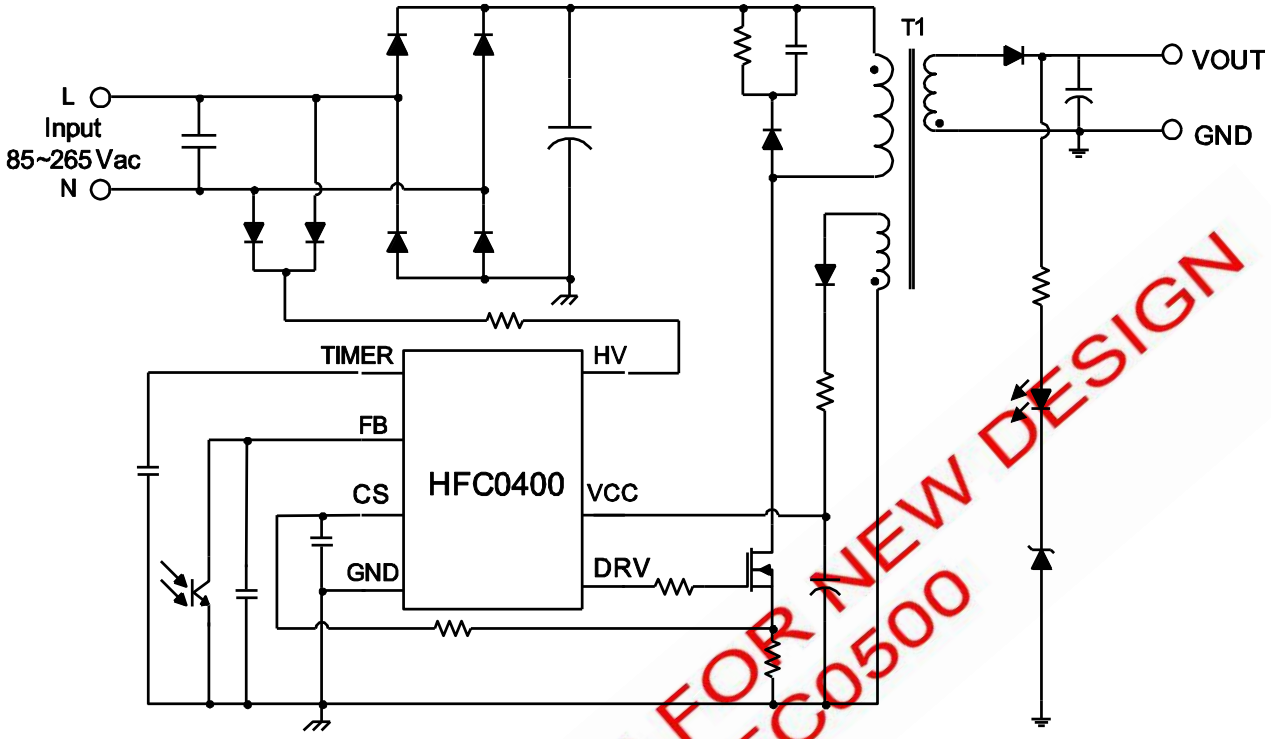
FEATURES

- Fixed-frequency current-mode control with built-in slope compensation
- Frequency foldback down to 25kHz at light loads
- Burst mode for low standby power consumption
- Frequency jitter to reduce EMI signature
- X-cap discharge function
- Internal high-voltage current source
- VCC under-voltage lockout with hysteresis (UVLO)
- Brown-out protection on HV pin
- Overload protection with programmable delay
- Thermal shutdown (auto-restart with hysteresis)
- Latch-off for external over-voltage protection (OVP) and over-temperature protection (OTP) on TIMER pin
- Short-circuit protection
- Programmable soft start

APPLICATIONS

- AC/DC adapters for notebook computers, tablets, and smartphones
- Offline battery chargers
- LCD TV s and monitors

TYPICAL APPLICATION

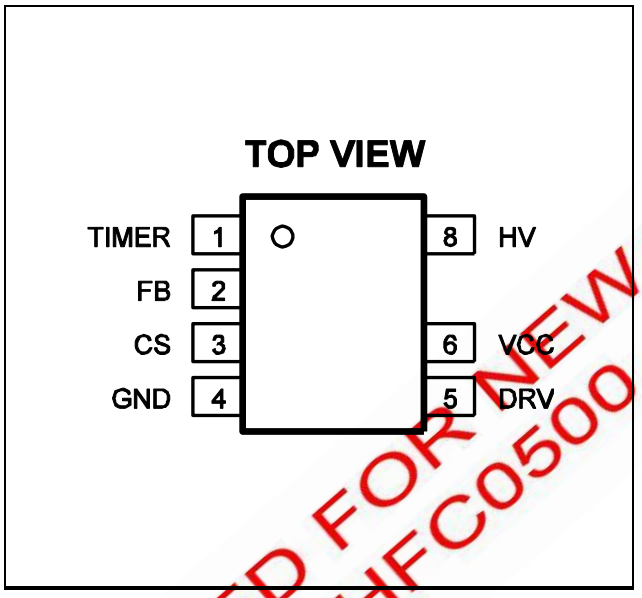


ORDERING INFORMATION

Part Number*	Package	Top Marking
HFC0400GS	SOIC8-7A	HFC0400

* For Tape & Reel, add suffix –Z (e.g. HFC0400GS–Z);

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

HV Break Down Voltage ..... -0.7V to 700V
V_{CC}, DRV to GND..... -0.3V to 30V
FB, TIMER, CS to GND ..... -0.3V to 7V
Continuous Power Dissipation (T_A = +25°C) (2) 1.3W
Junction Temperature..... 150°C
Thermal Shutdown..... 150°C
Thermal Shutdown Hysteresis..... 25°C
Lead Temperature ..... 260°C
Storage Temperature ..... -60°C to +150°C
ESD Capability Human Body Model (All Pins except HV) 4.0kV
ESD capability for Machine Mode..... 200V

Recommended Operation Conditions (3)

Operating Junction Temp (T_J).. -40°C to +125°C
Operating V_{CC} range ..... 8V to 20V

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
SOIC8-7A	96	45	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERICS

For typical value T_J=25°C, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Start-up Current Source (HV)						
Supply Current from HV	I_{HV}	V_{CC}=6V;V_{HV}=400V	1.6	1.85	2.1	mA
Leakage Current from HV	I_{HV}	V_{CC}=10V;V_{HV}=400V		15	25	μA
Break-Down Voltage	V_{BR}		700			V
Supply Voltage Management (VCC)						
VCC Current-Source Turn-Off Level, Rising	VCC_{OFF}		12	14.5	17	V
VCC Threshold for HV Turn-On Detection, Falling	VCC_{SS}		9.5	11.5	13.5	V
VCC Hysteresis for HV Turn-On Detection	VCC_{OFF} – VCC_{SS}		1.5	3		V
VCC Current-Source Turn-On Level, Falling	VCC_{ON}		7.0	8.0	9.0	V
VCC UVLO Hysteresis	VCC_{OFF} - VCC_{ON}		5	6.5		V
VCC Re-charge Level When Protection Occurs	VCC_{PRO}		4.7	5.3	5.9	V
VCC Decreasing Level When Latch-Off Phase Ends	VCC_{LATCH}			2.5		V
Internal IC Consumption	I_{CC}	V_{FB}=2V;C_L=1nF, V_{CC}=12V	1	1.5	2	mA
Internal IC Consumption, Latch Off Phase	$I_{CCLATCH}$	V_{CC}=6V	520	585	650	μA
Voltage above V_{CC} Where the Controller Latches Off (OVP)	V_{OVP}		22	25	27	V
OVP Comparator Blanking Duration	τ_{OVP}			26		μs
Brown-out						
HV Turn-On Threshold	HV_{ON}	V_{HV} rising	95	108	120	V
HV Turn-Off Threshold	HV_{OFF}	V_{HV} falling	90	103	115	V
Brown-Out Hysteresis	ΔHV		4	5.2	6.4	V
Timer Duration for Line Cycle Drop-out	τ_{HV}	C_{TIMER}=47nF	50			ms
Oscillator						
Oscillator Frequency	f_{OSC}		60	65	69.5	kHz
Frequency Jitter Amplitude, in Percentage of f_{OSC}	A_{jitter}			±6.7		%
Frequency Jitter Modulation Period	τ_{jitter}	C_{TIMER}=47nF		3.7		ms
Current Sense						
Current Limit	V_{ILIM}		0.9	0.95	1	V
Short-Circuit Protection Level	V_{SCP}		1.3	1.45	1.55	V
Leading-Edge Blanking for V_{ILIM}	τ_{LEB1}			350		ns
Leading-Edge Blanking for V_{SCP}	τ_{LEB2}			270		ns
Slope of the Compensation Ramp	S_{RAMP}		20	25	30	mV/μs

ELECTRICAL CHARACTERICS *(continued)*

For typical value T_J=25°C, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Feedback (FB)						
Internal Pull-Up Resistor	R_{FB}		12	14	16.5	kΩ
Internal Pull-Up Voltage	V_{DD}			4.3		V
V_{FB} to Internal Current Set-Point Division Ratio	K_{FB}			3.0		--
FB Level (Falling) at which the Controller Enters Burst Mode	V_{BURL}		0.29	0.32	0.35	V
FB Level (Rising) at which the Controller Exits Burst Mode	V_{BURH}		0.42	0.46	0.50	V
Over Load Protection						
FB Level at which the Controller Enters OLP after Blanking Time	V_{OLP}			3.7		V
Time Duration When FB Reaches Protection Point, Before OLP	τ_{OLP}	C_{TIMER}=47nF	50			ms
Frequency Foldback						
Frequency Foldback FB Voltage Threshold, Upper Limit	$V_{FB(FOLD)}$			1.8		V
Minimum Switching Frequency	$f_{OSC(min)}$		21	25	30	kHz
Frequency Foldback FB Voltage Threshold, Lower Limit	$V_{FB(FOLDE)}$			1.0		V
Latch-Off Input (Integration in TIMER)						
The Threshold below which Controller is Latched	$V_{TIMER(LATCH)}$		0.9	1	1.1	V
Blanking Duration on Latch Detection	τ_{LATCH}			12		μs
DRV Voltage						
Driver Voltage High Level	V_{High}	C_L=1nF V_{CC}=8.4V		6.7		V
		C_L=1nF V_{CC}=12V		10.3		V
Driver Voltage-Clamp Level	V_{Clamp}	C_L=1nF, V_{CC}=24V		13.4		V
Driver Voltage, Low Level	V_{Low}	C_L=1nF, V_{CC}=24V		16		mV
Driver Voltage, Rise Time	τ_R	C_L=1nF, V_{CC}=16V		13		ns
Driver Voltage, Fall Time	τ_F	C_L=1nF, V_{CC}=16V		23		ns
Driver Pull-Up Resistance	$R_{Pull-up}$	C_L=1nF, V_{CC}=16V		8		Ω
Driver Pull-Down Resistance	$R_{Pull-down}$	C_L=1nF, V_{CC}=16V		20		Ω

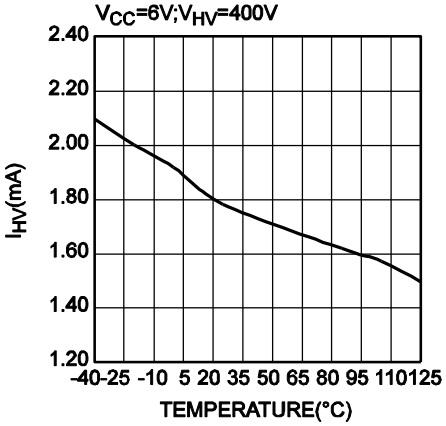
PIN FUNCTIONS

Pin #	Name	Description
1	TIMER	Timer. This pin combines the soft start, frequency jittering, and timer functions for OLP, brown-out protection, and X-cap discharge. Latch the IC by pulling this pin down.
2	FB	Feedback. Use a pull-down optocoupler to control output regulation.
3	CS	Current Sense. Senses the primary current for current-mode operation.
4	GND	IC Ground.
5	DRV	Drive Signal Output.
6	VCC	Power Supply.
8	HV	High-Voltage Current Source. Includes brown-out and X-cap discharge functions.

TYPICAL CHARACTERISTICS

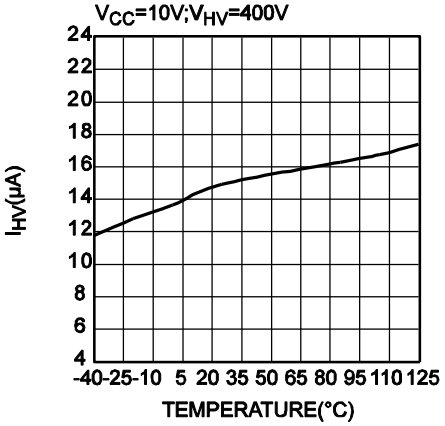
Supply Current from HV vs. Temperature

V_{CC}=6V;V_{HV}=400V



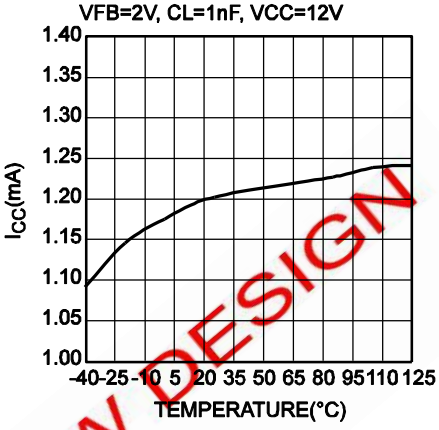
Leakage Current from HV vs. Temperature

V_{CC}=10V;V_{HV}=400V

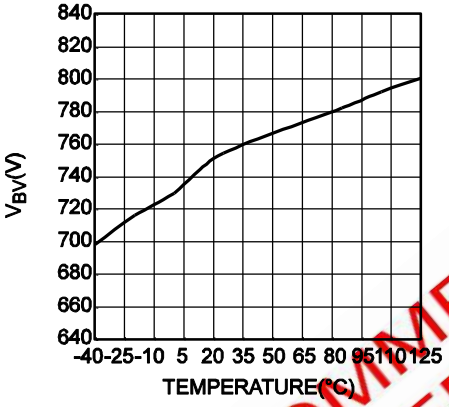


Internal IC Consumption vs. Temperature

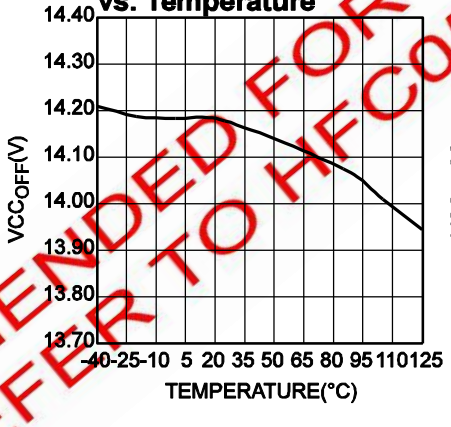
VFB=2V, CL=1nF, VCC=12V



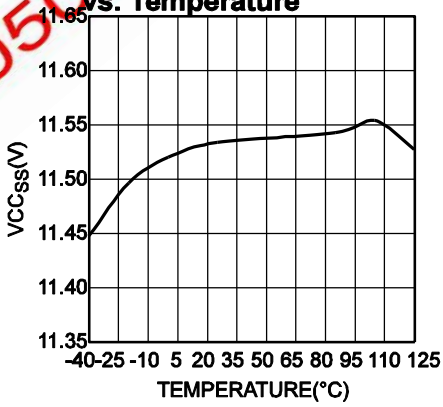
Break-Down Voltage vs. Temperature



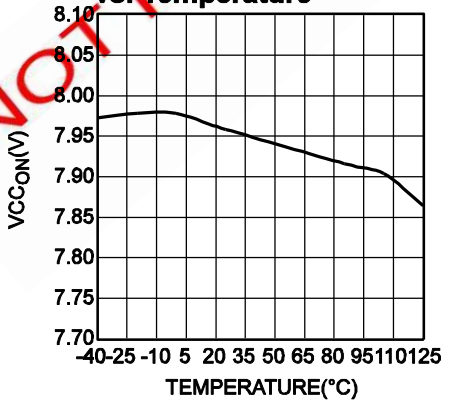
VCC Current-Source Turn-Off Level, Rising vs. Temperature



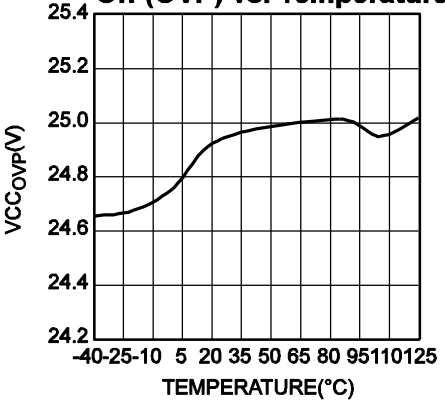
VCC Threshold for HV Turn-On Detection, Falling vs. Temperature



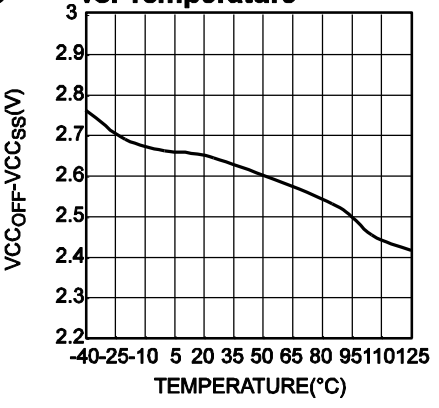
VCC Current-Source Turn-On Level, Falling vs. Temperature



Voltage above VCC Where the Controller Latches Off (OVP) vs. Temperature

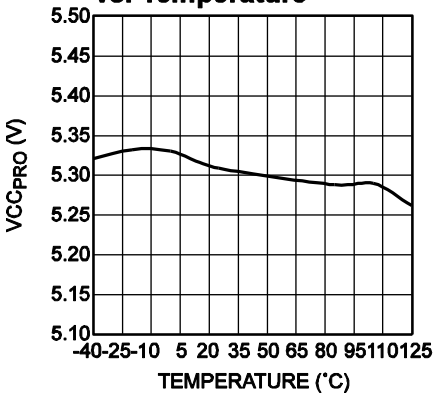


VCC Hysteresis for HV Turn-On Detection vs. Temperature

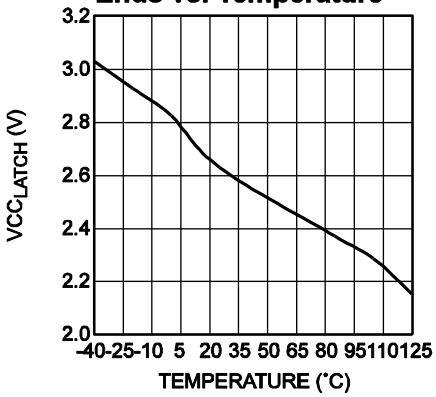


TYPICAL CHARACTERISTICS *(continued)*

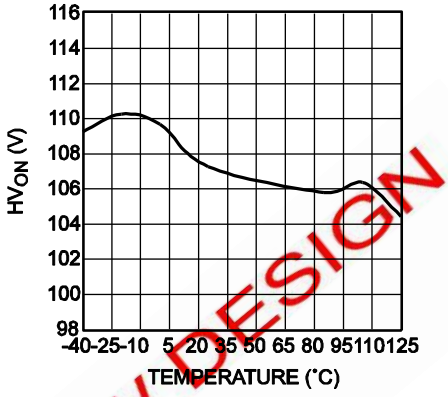
VCC Re-charge Level when Protection Occurs vs. Temperature



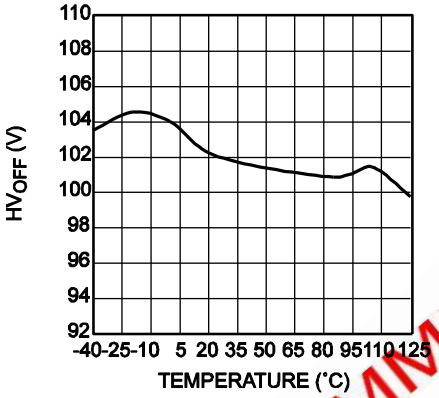
VCC Decreasing Level When Latch-off Phase Ends vs. Temperature



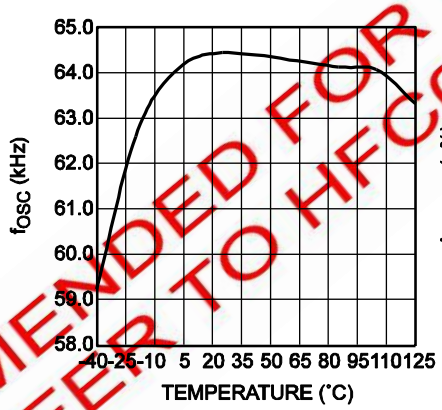
HV Turn-on Threshold vs. Temperature



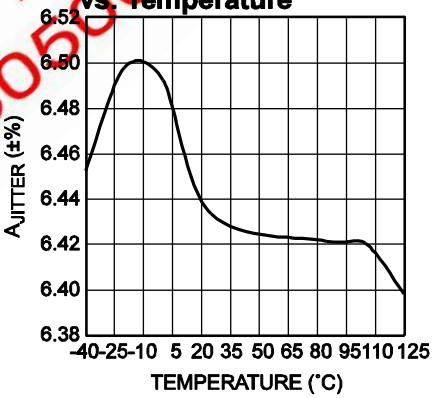
HV Turn-off Threshold vs. Temperature



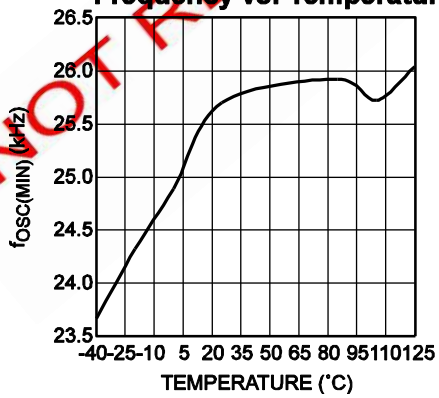
Oscillator Frequency vs. Temperature



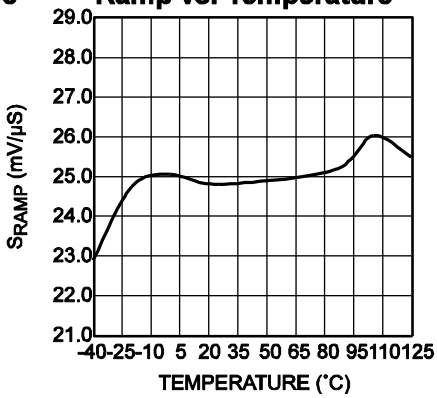
Frequency Jitter Amplitude, in Percentage of f_{OSC} vs. Temperature



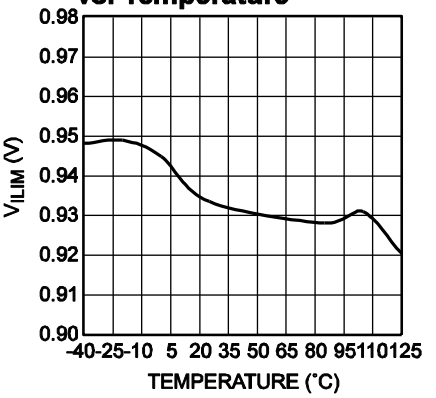
Minimum Switching Frequency vs. Temperature



Slope of the Compensation Ramp vs. Temperature

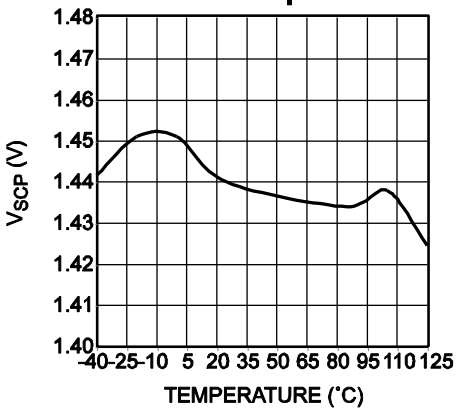


Current Limit vs. Temperature

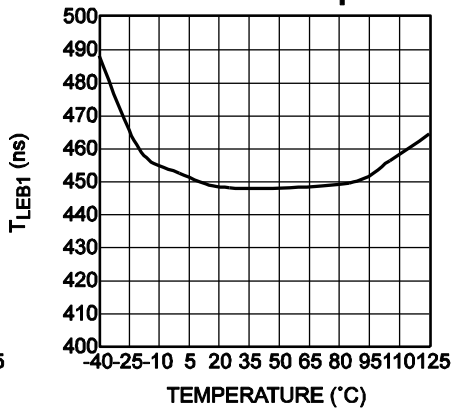


TYPICAL CHARACTERISTICS *(continued)*

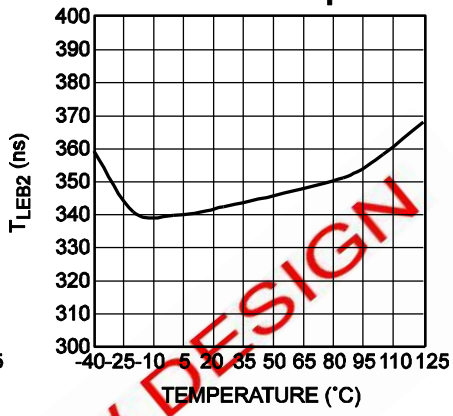
Short-Circuit Protection Level vs. Temperature



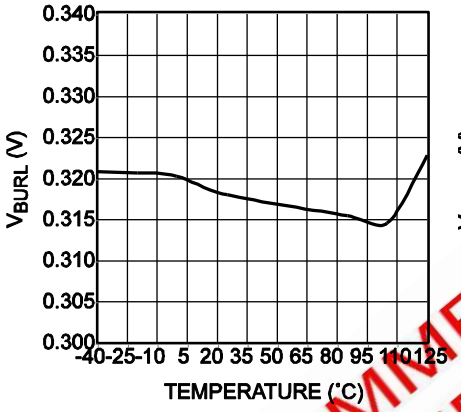
Leading-Edge Blanking for VILIM vs. Temperature



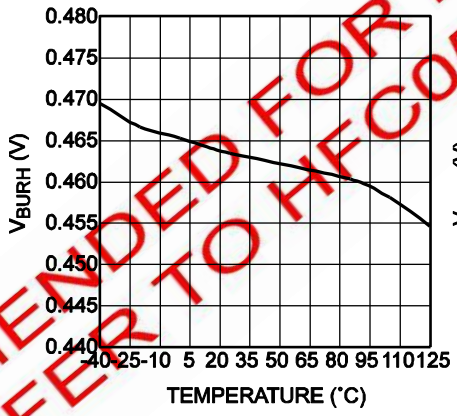
Leading Edge Blanking for VSCP vs. Temperature



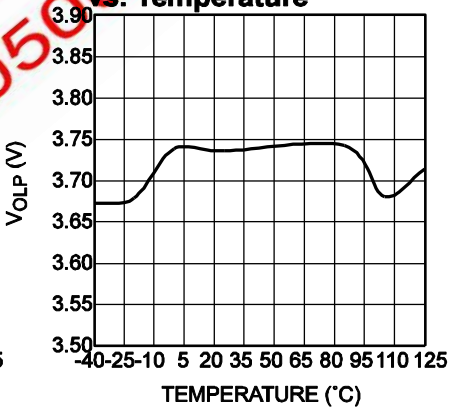
FB Level (Falling) at which the Controller Enters Burst Mode vs. Temperature



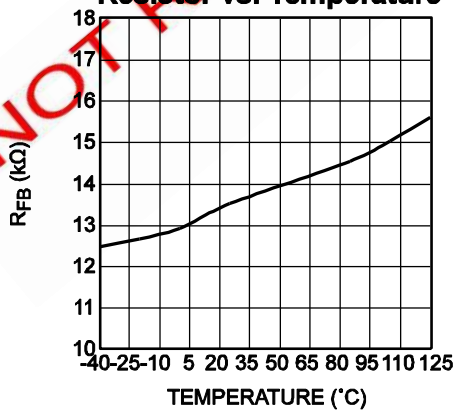
FB Level (Rising) at which the Controller Exits Burst Mode vs. Temperature



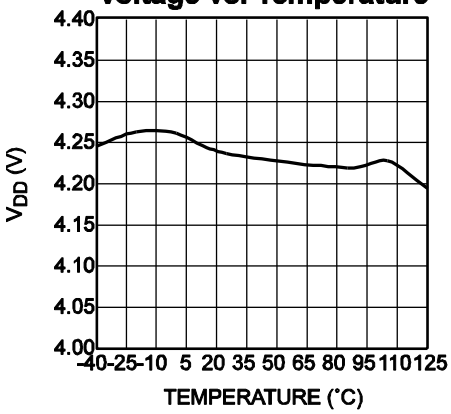
FB Level at which the Controller Enters OLP after Blanking Time vs. Temperature



FB Internal Pull-up Resistor vs. Temperature



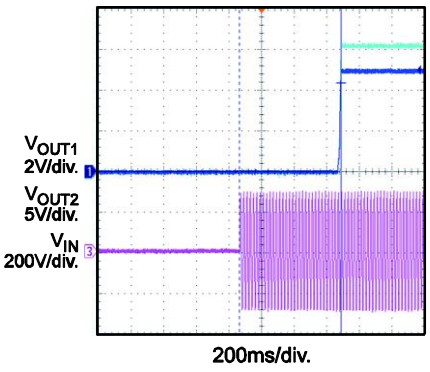
FB Internal Pull-up Voltage vs. Temperature



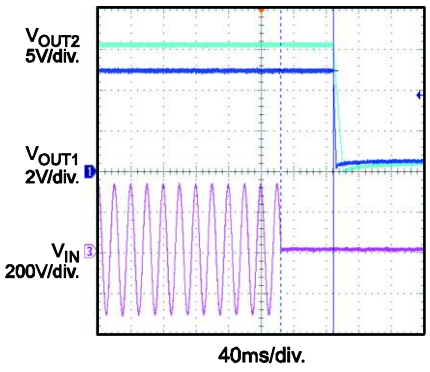
TYPICAL PERFORMANCE CHARACTERISIC

V_{IN}=230VAC, V_{OUT1}=5V, I_{OUT1}=3A, V_{OUT2}=16V, I_{OUT2}=1.5A, T_A=25°C, unless otherwise noted.

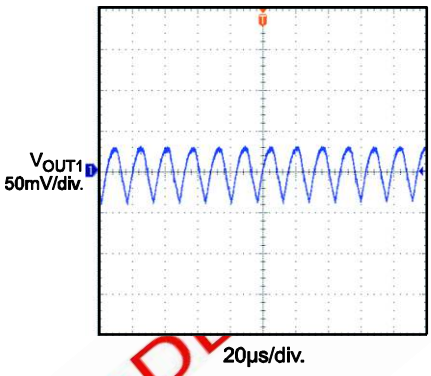
Input Power Start Up



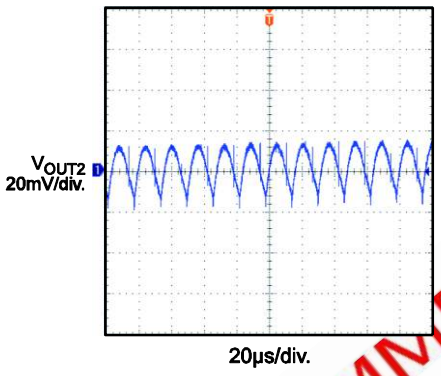
Inut Power Shut Down



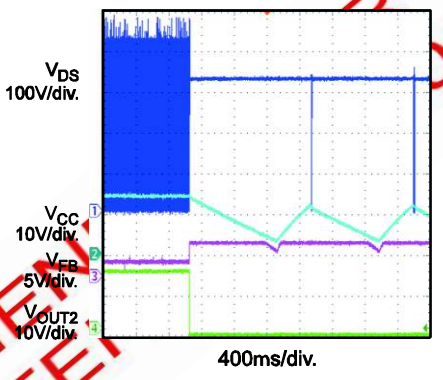
Output1 Ripple



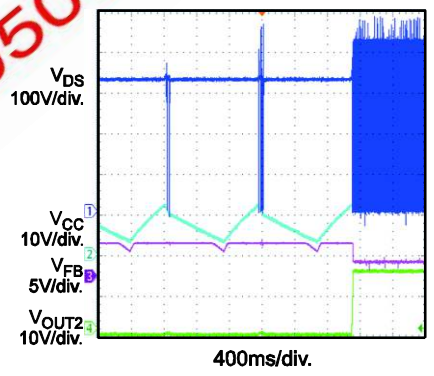
Output2 Ripple



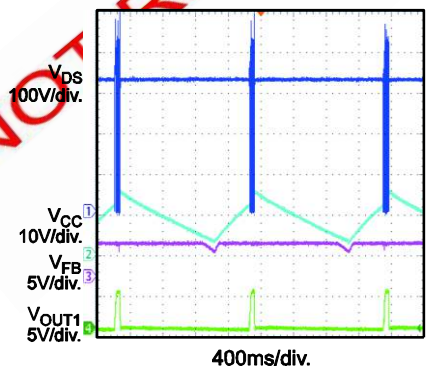
SCP Entry



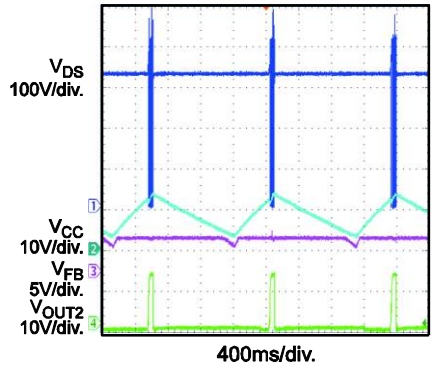
SCP Recovery



OLP, 5V Over Load

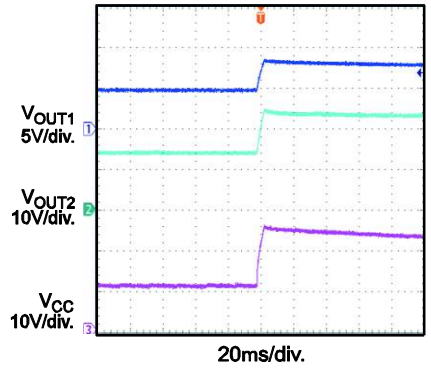


OLP, 16V Over Load



OVP

No Load

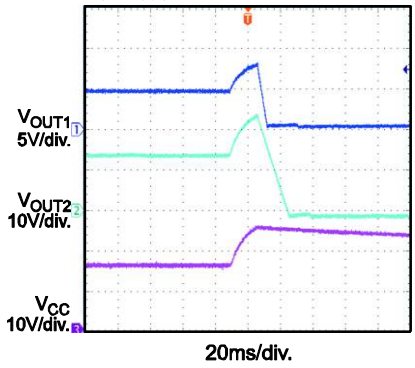


TYPICAL PERFORMANCE CHARACTERISIC *(continued)*

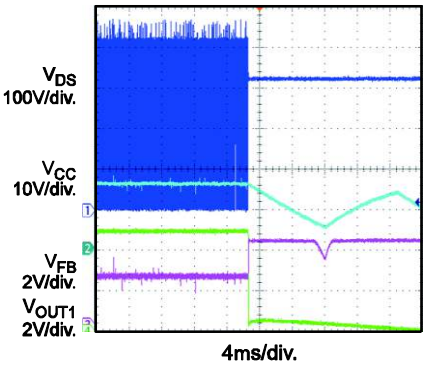
V_{IN}=230VAC, V_{OUT1}=5V, I_{OUT1}=3A, V_{OUT2}=16V, I_{OUT2}=1.5A, T_A=25°C, unless otherwise noted.

OVP

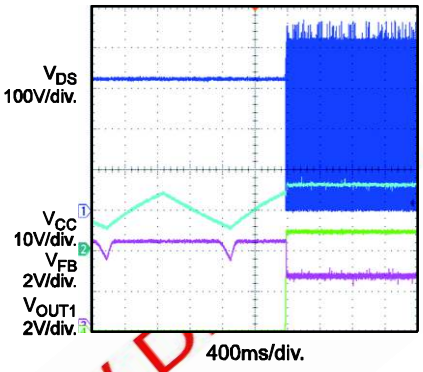
Full Load



OTP Entry

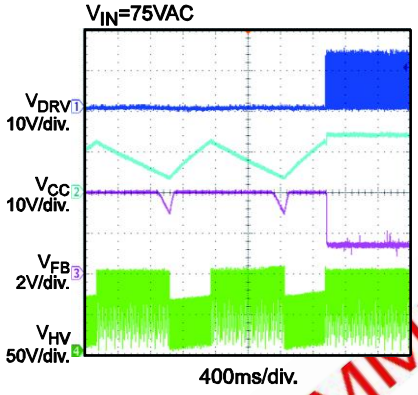


OTP Recovery



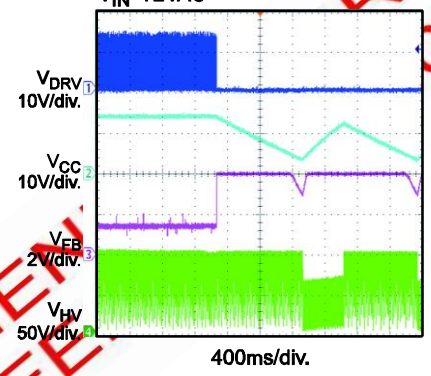
Brown-in

V_{IN}=75VAC



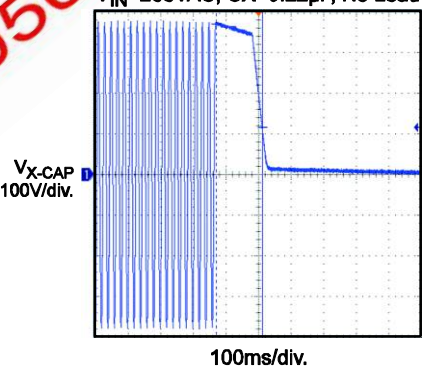
Brown-out

V_{IN}=72VAC



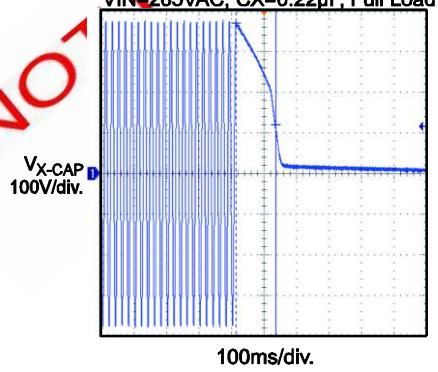
X-cap Discharge

V_{IN}=265VAC, CX=0.22μF, No Load



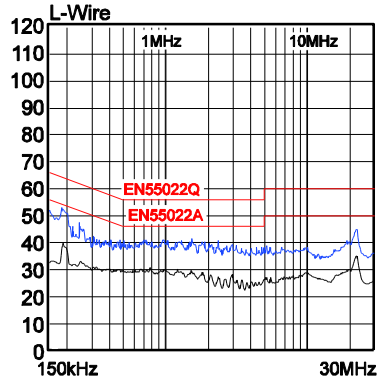
X-cap Discharge,

VIN=265VAC, CX=0.22μF, Full Load



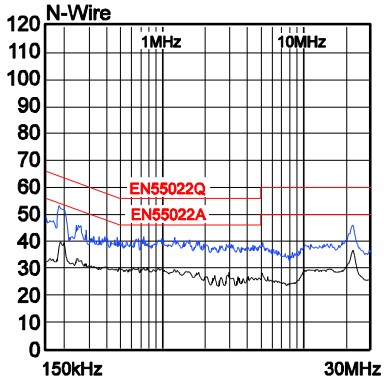
Conducted EMI

L-Wire



Conducted EMI

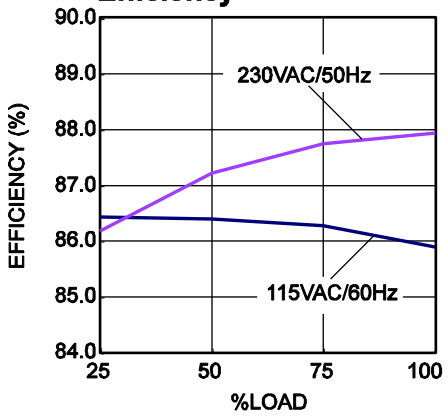
N-Wire



TYPICAL PERFORMANCE CHARACTERISIC *(continued)*

V_{IN}=230VAC, V_{OUT1}=5V, I_{OUT1}=3A, V_{OUT2}=16V, I_{OUT2}=1.5A, T_A=25°C, unless otherwise noted.

Efficiency



No Load Power Consumption

V_{IN} (VAC/Hz)		85/60	115/60	230/50	265/50
P_{IN} (mW)	5V/0A, 16V/0A	26.35	27.59	32.40	35.26
	5V/6mA, 16V/0A	71.92	72.72	80.70	84. 83

OPERATION

HFC0400 incorporates all the necessary features to build a reliable switch-mode power supply. It is a fixed-frequency current-mode controller with built-in slope compensation. At light loads, the controller freezes the peak current and reduces its switching frequency down to 25kHz to minimize switching losses. When the output power falls below a given level, the controller enters burst mode. It also has excellent EMI performance thanks to frequency jittering.

Its high level of integration requires very few external components.

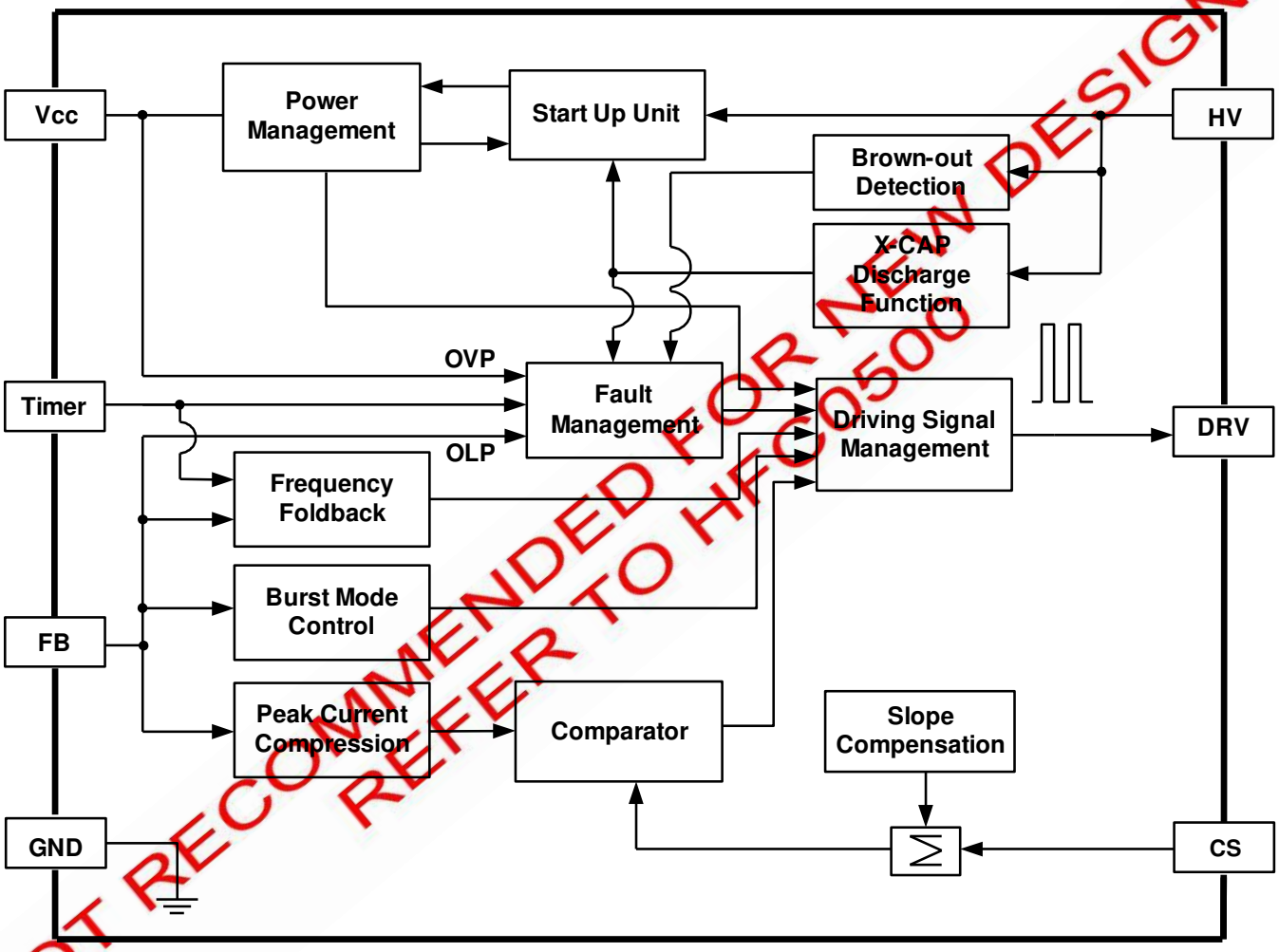


Figure 1: Functional Block Diagram

Fixed-Frequency with Jitter

Frequency jitter reduces EMI by dissipating the energy. Figure 2 shows the circuit of frequency jittering.

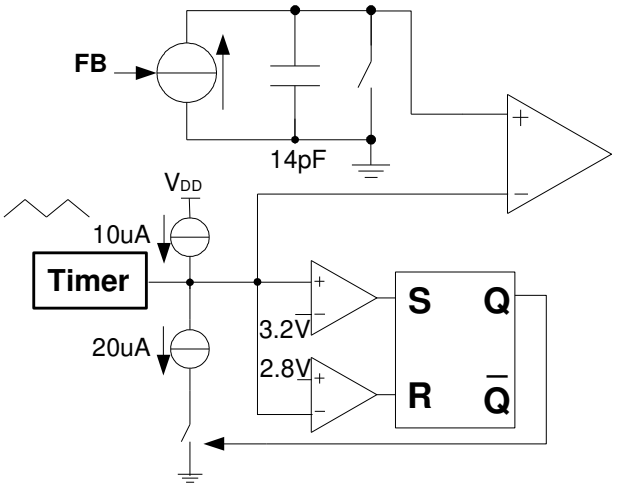


Figure 2: Frequency Jitter Circuit

A controlled current sourced (fixed at 2.72μA when V_{FB}=2V) chargers the internal 14pF capacitor. Comparing the capacitor voltage to the TIMER voltage estimates the switching frequency as per equation (1). V_{TIMER} is a triangular wave that ranges between 2.8V and 3.2V with a charging/discharging current of 10μA. Figure 3 shows shows the frequency jitter, τ_{jitter}, as per equation (2).

$$f_s = \frac{1}{14pF \cdot V_{TIMER} / 2.72\mu A + 0.2\mu s} \quad (1)$$

$$\tau_{jitter} = 2 \cdot \frac{C_{TIMER} \cdot (3.2V - 2.8V)}{10\mu A} \quad (2)$$

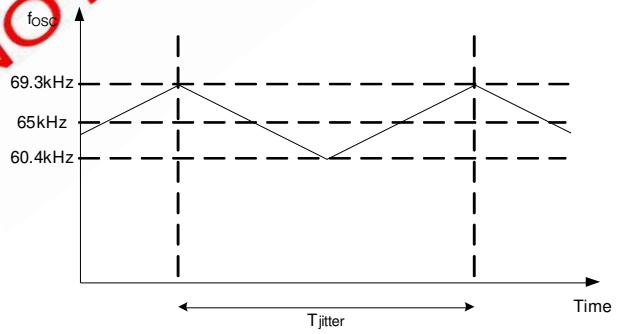


Figure 3: Frequency Jitter

Frequency Foldback

The HFC0400 implements frequency foldback at light load condition to improve overall efficiency.

When the load decreases to a given level (1.33V<V_{FB}<2V), the controller freezes the peak current (as measured as the voltage on the CS pin, 0.67V) and reduces its switching frequency down to 25kHz which helps to reduce the switching loss. If the load continues to decrease, the peak current decreases at a 25kHz fixed frequency to avoid audible noise. Figure 4 shows the frequency vs.V_{FB} and peak current (V_{CS}) vs. V_{FB}.

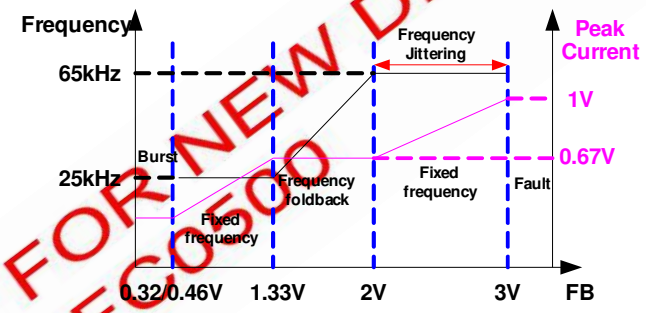


Figure 4: Frequency and Peak Current (V_{CS}) vs V_{FB}

Current-Mode Operation with Slope Compensation

V_{FB} controls the primary-peak current. When the peak current reaches the level determined by V_{FB}, DRV turns off. The controller can also be used in continuous conduction mode (CCM) with a wide input voltage range because its internal synchronous slope compensation (30mV/μs) avoids sub-harmonic oscillations when the duty cycle exceeds 50%.

High Voltage Startup Current Source with Brown-Out Detection

Initially, the internal high-voltage current source drawn from the HV pin supplies the IC. The IC turns off the current source as soon as V_{CC} reaches 14.5V and detects the voltage on HV. Once the HV voltage exceeds HV_{ON} before V_{CC} drops down to 11.5V, the controller starts switching. Otherwise the system treats the condition as a brown-out to to lock the driver

output, causing V_{CC} to drop down to 5.3V and the high-voltage current source turns on to recharge V_{CC}. The auxiliary transformer winding supplies the IC after the controller starts switching. If V_{CC} falls below 8.0V, the switching pulse stops and the current source turns on again. Figure 5 shows the typical V_{CC} under-voltage lockout waveform.

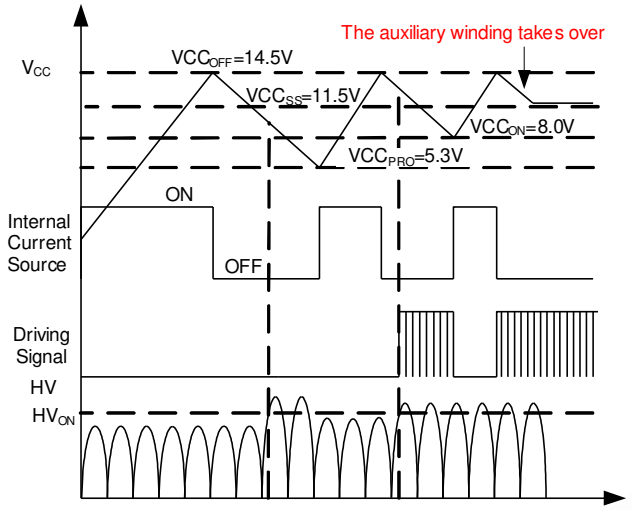


Figure 5: V_{CC} Under-Voltage Lockout

The V_{CC} lower threshold UVLO drops from 8V to 5.3V under fault conditions, such as OLP, SCP, brown-out, OVP, and OTP.

Soft Start

The peak current (controlled by the TIMER voltage) gradually increases from 0.25V to 1V, as does the switching frequency, to reduce the stress on power components and to smoothly establish the output voltage as the TIMER voltage increases from 1V to 1.75V during start-up. Figure 6 shows the typical soft-start waveform. The TIMER capacitor determines the start-up duration as per equation (3).

$$\tau_{Soft-start} = \frac{C_{TIMER} \cdot (1.75V - 1V)}{10/4\mu A} \quad (3)$$

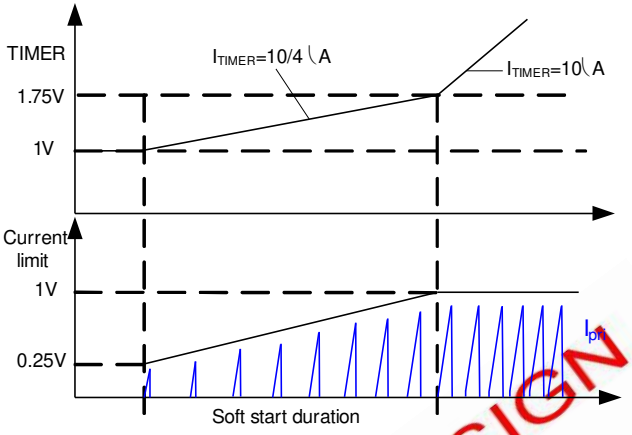


Figure 6: Soft-Start

Burst Mode

The HFC0400 enters burst-mode operation to minimize power dissipation at no load or light load. As the load decreases, V_{FB} decreases. The IC stops the switching cycle when V_{FB} drops below the lower threshold, V_{BRUL}−0.32V. The output voltage starts to drop, which causes V_{FB} to increase again. Once V_{FB} exceeds V_{BRUH}−0.46V, switching resumes. V_{FB} then rises and falls repeatedly. Burst mode alternately enables and disables MOSFET switching, thereby reducing no load or light load switching losses.

Timer-Based Over-Load Protection

In a flyback converter, a fixed switching frequency results in a peak-current-limited maximum output power. When the output demand exceeds the power limit, the output voltage drops below the set value. Then the current flowing through primary and secondary optocoupler falls and V_{FB} is pulled high. The HFC0400 implements a timer-based OLP block as per Figure 7.

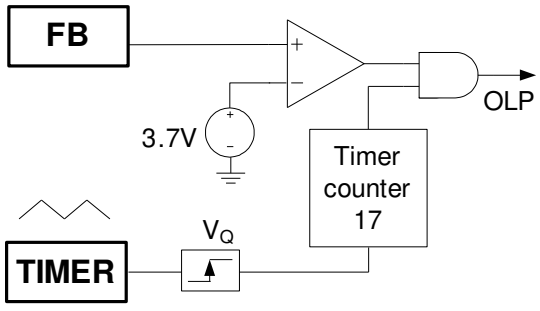


Figure 7: Overload Protection Block

When FB exceeds 3.7V (considered an error), the timer starts to count the V_Q rising edge. Removing the error flag resets the timer. If the timer reaches its completion (a count of 17), OLP triggers. This timer duration avoids triggering OLP during the power supply start-up or a load transition phase. Figure 8 shows OLP.

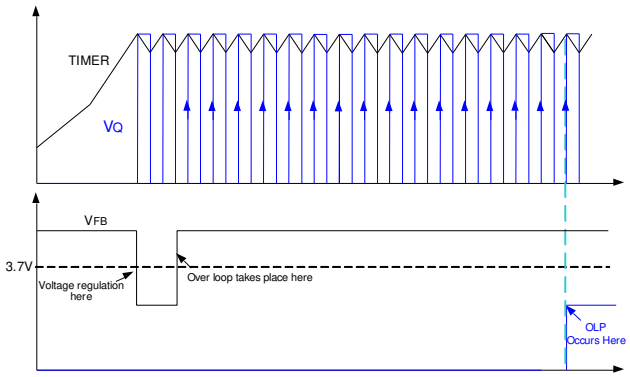


Figure 8: Overload Protection

Timer-Based Brown-Out Protection

The brown-out protection block is similar to the OLP block. When the HV voltage drops below HV_{OFF} (which is an error), the timer starts to count the V_Q rising edges. Once the HV voltage exceeds HV_{OFF}, the timer resets. When the timer has counted to 17, brown-out protection triggers and the switching pulse stops.

Short-Circuit Protection (SCP)

The HFC0400 has short-circuit protection that senses the CS voltage and stops switching if V_{CS} reaches 1.5V after a reduced leading-edge blanking (LEB) time. As soon as the fault disappears, the power supply resumes operation.

Thermal Shutdown (TSD)

To prevent from any lethal thermal damage, HFC0400 shuts down switching when the inner temperature exceeds 150°C. As soon as the inner temperature drops below 125°C, the power supply resumes operation. During TSD, the V_{CC} UVLO lower threshold drops from 8.0V to 5.3V.

V_{CC} Over-Voltage Protection (OVP)

The HFC0400 enters latched fault condition if V_{CC} goes above 25V for 25µs. The controller stays fully latched until V_{CC} drops below 2.5V, e.g. when the user power-cycles the main input.

TIMER Latch-Off for OVP and OTP

Pulling TIMER down below 1.0V for 12µs latches the HFC0400 off for external OVP and OTP etc.

X-Cap Discharge Function

X-caps typically filters the differential-mode EMI noise from a power supply's input. These components pose a potential hazard because they can store unsafe levels of high-voltage energy for long after the AC line is disconnected. Resistors in parallel to the X-cap provide a discharge path to meet safety standards, but constantly dissipate power while the AC is connected, and contribute to no-load and standby input power consumption.

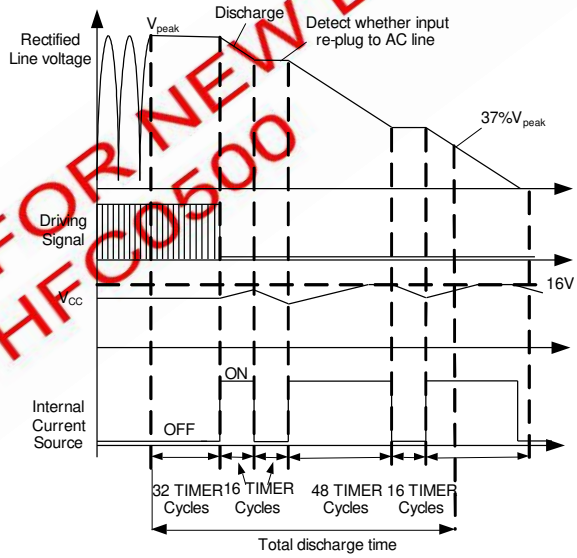


Figure 9: X-Cap Discharger

The HFC0400's HV acts as a smart X-cap discharger. In the presence of an AC voltage, the internal high-voltage current source turns off to block HV current flow and the IC monitors the HV voltage. Upon removing the AC voltage, the IC turns on the high-voltage current source after about 32 TIMER cycles to discharge the X-cap. The first discharge duration is 16 cycles, then the IC turns off the current source for 16 cycles to detect the presence of the AC line. If the AC input remains disconnected, the IC turns on the current source for 48 cycles, then off for 16 cycles repeatedly until the voltage on X-cap drops to V_{CC}. Upon detecting an AC input, the high-voltage current source remains off until V_{CC}

drops to VCC_{PRO} (5.3V) before recharging V_{CC} to restart the system. Figure 9 shows the discharge function waveforms.

This approach provides a discharge path for the X-cap, eliminating discharge resistors and reduce power loss.

Clamped Driver

The DRV voltage is safely clamped at 13.4V when V_{CC} exceeds 16V, allowing the use of any standard MOSFET.

Leading-Edge Blanking

An internal leading-edge blanking (LEB) unit containing two LEB times is employed between the CS pin and the current comparator input to avoid premature switching pulse termination due to the parasitic capacitances. During the blanking time, the current comparator is disabled and can not turn off the external MOSFET. Figure 10 shows the LEB waveform.

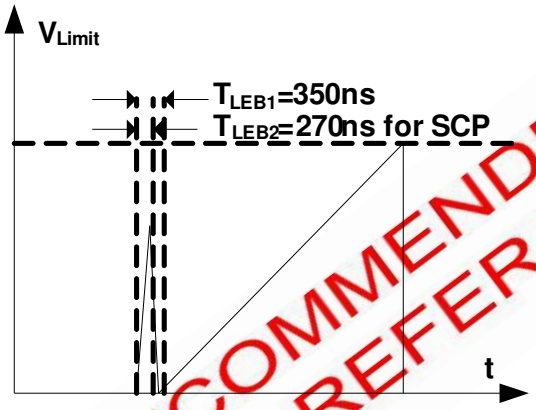


Figure 10: Leading-Edge Blanking

APPLICATION INFORMATION

VCC Capacitor Selection

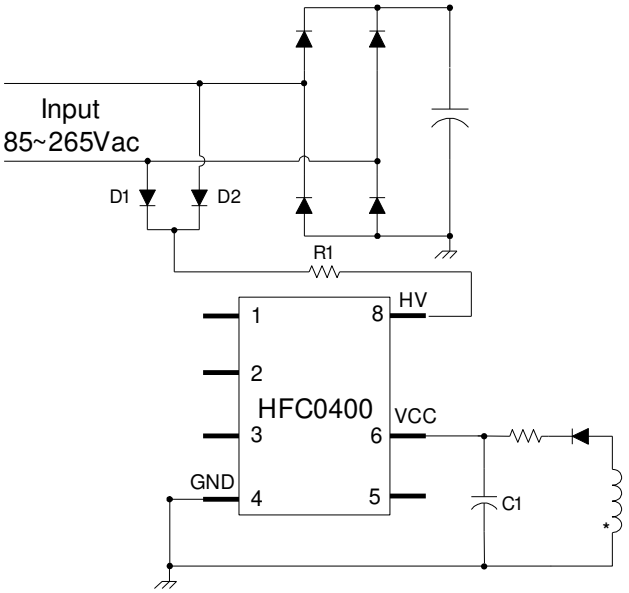


Figure 11: Start-Up Circuit

Figure 11 shows the start-up circuit. The values of R1 and C1 determine the system start-up delay time: a larger R1 or C1 increases the start-up delay. The V_{CC} duration (from $V_{CC,OFF}$ to $V_{CC,SS}$) for brown-out detection should exceed half the input period, equation (4) provides an estimated value for the V_{CC} capacitor, where $I_{CC(noswitch)}$ is the internal consumption (close to $I_{CCLatch}$), and τ_{input} is period of the AC input. For most applications, chose a V_{CC} capacitor value that exceeds 10µF.

$$C_{VCC} > \frac{I_{CC(noswitch)} \cdot 0.5 \cdot \tau_{input}}{VCC_{OFF} - VCC_{SS}} \quad (4)$$

Primary-Side Inductor Design (L_m)

With build-in slope compensation, HFC0400 supports CCM when the duty cycle exceeds 50%. Set a ratio (K_P) of the primary inductor's ripple current amplitude vs. the peak current value to $0<K_P\leq1$, where $K_P=1$ for DCM. Figure 12 shows the relevant waveforms. A larger inductor leads to a smaller K_P leads, which can reduce RMS current but increase transformer size. An optimal K_P value is between 0.6 and 0.8 for the universal input range and 0.8 to 1 for a 230VAC input range.

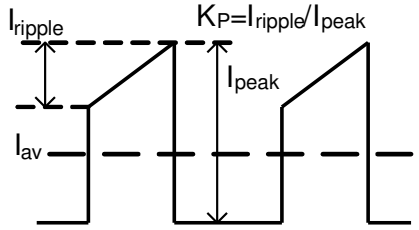


Figure 12: Typical Primary-Current Waveform

The input power (P_{in}) at the minimum input can be estimated as

$$P_{in} = \frac{V_O \cdot I_O}{\eta} \quad (5)$$

Where V_O is the output voltage, I_O is the rated output current, η is the estimated efficiency. Generally, η is between 0.75 and 0.85 depending on the input range and output application.

For CCM at minimum input, the converter duty cycle is:

$$D = \frac{(V_O + V_F) \cdot N}{(V_O + V_F) \cdot N + V_{in(min)}} \quad (6)$$

Where:

V_F is the secondary diode's forward voltage,

N is the transformer turn ratio, and

$V_{in(min)}$ is the minimum voltage on bulk capacitor.

The MOSFET turn-on time is

$$\tau_{on} = D \cdot \tau_s \quad (7)$$

Where τ_s is the frequency jitter's dominant switching period, $\frac{1}{\tau_s} = f_s = 65kHz$.

The average, peak, ripple and valley values of the primary current are described as follows:

$$I_{av} = \frac{P_{in}}{V_{in(min)}} \quad (8)$$

$$I_{peak} = \frac{I_{av}}{(1-\frac{K_P}{2}) \cdot D} \quad (9)$$

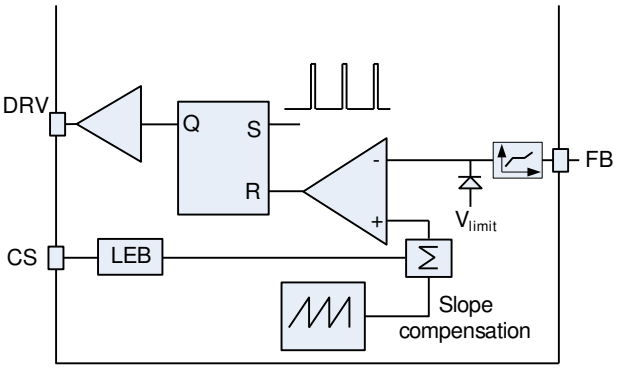
$$I_{ripple} = K_P \cdot I_{peak} \quad (10)$$

$$I_{valley} = (1-K_P) \cdot I_{peak} \quad (11)$$

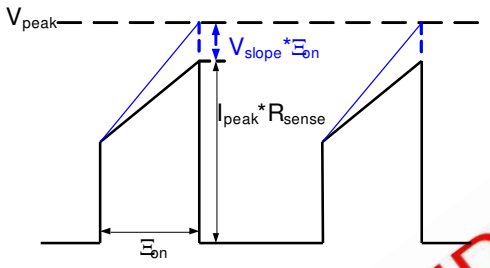
The following equation estimates L_m as

$$L_m = \frac{V_{in(min)} \cdot \tau_{on}}{I_{ripples}} \quad (12)$$

Current-Sense Resistor



a) Peak-Current-Comparator Circuit



b) Typical Waveform

Figure 13: Peak-Current Comparator

Figure 13 shows the peak-current-comparator logic and the subsequent waveform. When the sum of the sensing resistor voltage and the slope compensator reaches V_{peak}, the comparator goes HIGH to reset the RS flip-flop, and the DRV pin is pulled down to turn off the MOSFET. The maximum current limit (V_{limit}, as measured by V_{CS}) is 0.95V. The slope compensator (V_{slope}) is ~25mV/μs. Given the margin, use 0.95×V_{limit} as V_{peak} at full load. The voltage on sensing resistor is then:

$$V_{sense} = 95\% \cdot V_{limit} - V_{slope} \cdot \tau_{on} \quad (13)$$

So the value of the sense resistor is

$$R_{sense} = \frac{V_{sense}}{I_{peak}} \quad (14)$$

Select the current sense resistor with an appropriate power rating based on the power loss:

$$P_{sense} = \left[\left(\frac{I_{peak} + I_{valley}}{2} \right)^2 + \frac{1}{12} \left(I_{peak} - I_{valley} \right)^2 \right] \cdot D \cdot R_{sense} \quad (15)$$

Low-Pass Filter on CS Pin

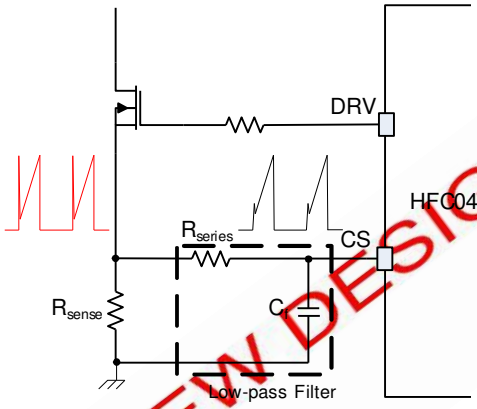


Figure 14: Low-Pass Filter on CS Pin

A small capacitor connected to the CS pin with R_{series} forms a low-pass filter for noise filtering when the MOSFET turns on and off, as shown in Figure 14. The series resistance (R_{series}) should not exceed 1kΩ. The low-pass filter's R×C constant should not exceed 1/3 of the leading-edge blanking period for SCP (LEB2, 270ns), or the filtered sensed voltage won't reach the SCP point (1.5V) to trigger SCP if an output short circuit occurs.

Jitter Period

Frequency jitter is an effective method to reduce EMI by dissipating energy. The nth-order harmonic noise bandwidth is $B_{Tn} = n \cdot (2 \cdot \Delta f + f_{jitter})$, where Δf is the frequency jitter amplitude. If B_{Tn} exceeds the resolution bandwidth (RBW) of the spectrum analyzer (200Hz for noise frequency less than 150 kHz, 9 kHz for noise frequency between 150kHz to 30MHz), the spectrum analyzer receives less noise energy.

The capacitor on the TIMER pin determines the period of the frequency jitter. A 10μA current source charges the capacitor; when the TIMER voltage reaches 3.2V, another 10μA current

source discharges the capacitor to 2.8V. This charging and discharging cycle repeats.

Equation (2) describes the jitter period In theory, a smaller f_{jitter} is more effective at EMI reduction. However, the measurement bandwidth requires that f_{jitter} should be large compared to spectrum analyzer RBW for effective EMI reduction. Also, f_{jitter} should be less than the control-loop-gain crossover frequency to avoid disturbing the output voltage regulation. So for most applications, select f_{jitter} between 200Hz and 400Hz.

X-Cap Discharge Time

Figure 9 shows the X-cap discharger waveforms. The maximum discharge time occurs at a high-line input and under no-load because the energy on X-cap dissipates but won't transfer to the bulk capacitor.

The maximum discharge delay time is

$$\tau_{delay} = 32 \cdot \tau_{jitter} \quad (16)$$

When the high-voltage current source turns on, a constant supply current (I_{HV}, 1.6mA typically) flows into HV. The current-source discharge time for the X-cap to drop to 37% of peak voltage can be estimated by:

$$\tau_{discharge} = \frac{C_X \cdot 63\% \cdot \sqrt{2} \cdot V_{ac(max)}}{I_{HV}} \quad (17)$$

Where C_X is the X-cap capacitance, $V_{ac(max)}$ is the maximum AC-input RMS value.

The first discharging period is $16\times\tau_{jitter}$, with subsequent period equal to $48\times\tau_{jitter}$. The sections times approximately eequals:

$$n = \frac{\tau_{discharge} - 16 \cdot \tau_{jitter}}{48 \cdot \tau_{jitter}} + 1 \quad (18)$$

Rounding n determins the number of detecting sections, as every section is $16\times\tau_{jitter}$, the detecting time is shown as follow:

$$T_{detect} = 16 \cdot \tau_{jitter} \cdot n \quad (19)$$

As a result, the total discharge time is then.

$$\tau_{total} = \tau_{delay} + \tau_{discharge} + \tau_{detect} \quad (20)$$

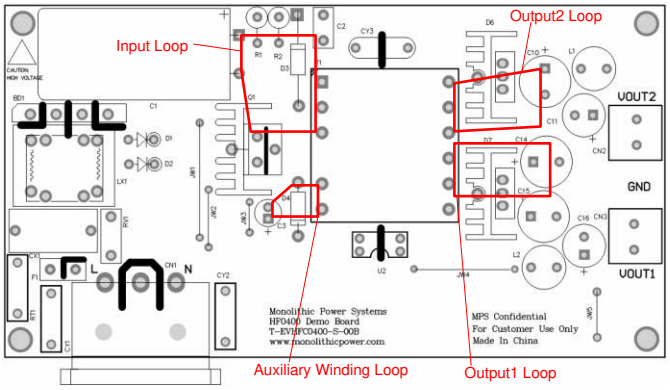
The total discharge time is relative to τ_{jitter}. For example, if C_{TIMER} is 47nF and τ_{jitter}=3.7ms, the X-cap discharge margin is 1s due to X-cap value deviations (around ±10% typically), select an X-cap less than 3.3μF.

Though the X-cap has been discharged, it may still retain a high-voltage on the bulk capacitor. For safety, make sure it is released before the debugging the board.

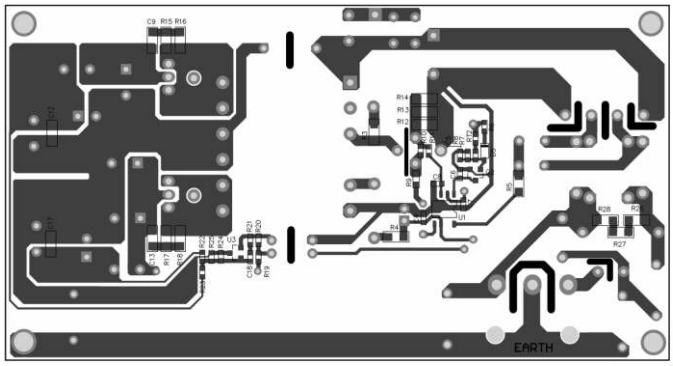
PCB Layout Guide

PCB layout is important to achieve reliable operation, good EMI performance, and good thermal performance. Follow these guidelines to optimize performance.

1) Minimize the power stage switching stage loop area. This includes the input loop (C1 - T1 - Q1 – R12/R13 – C1), the auxiliary winding loop (T1 – D4 – R4 – C3 – T1), and the output loop (T1 – D6 – C10 – T1 and T1 – D7 – C14 – T1).
2) The input loop GND and control circuit should be separate and only connect at C1.
3) Connecting the Q1 heatsink to the primary GND plane improves EMI.
4) Place the control circuit capacitors (such as those for FB, CS and VCC pins) close to IC to decouple noise.



a) Top



b) Bottom

Figure 15: PCB Layout

Typical Application Circuit

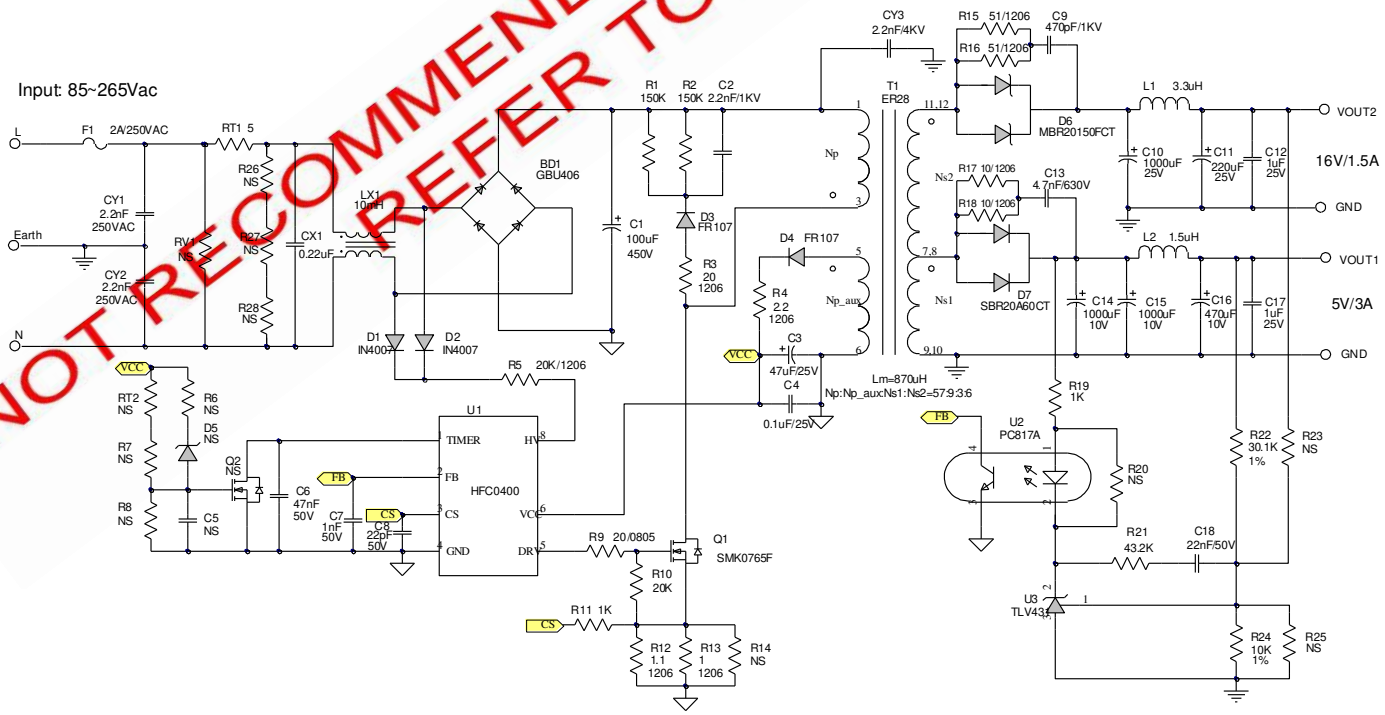


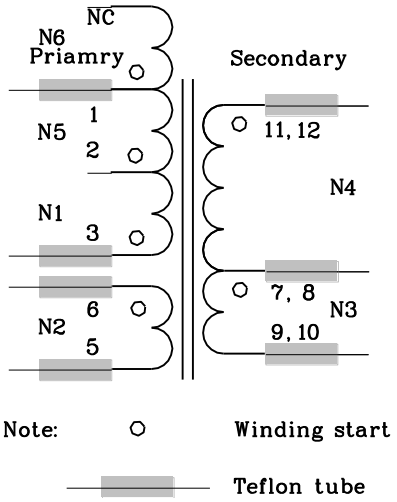
Figure 16: Example of a Typical Application

Design Example

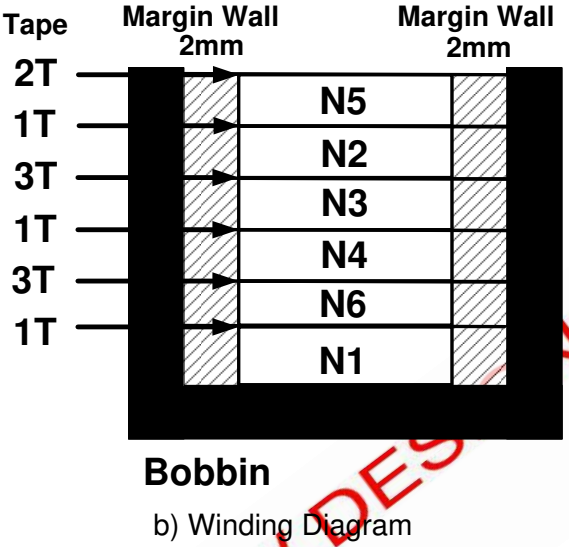
Below is a design example of HFC0400 for dual-output applications.

Table 1—Design Spec.

V_{IN}	85 to 265VAC
V_{OUT1}	5V
I_{OUT1}	3A
V_{OUT2}	16V
I_{OUT2}	1.5A



a) Connection Diagram



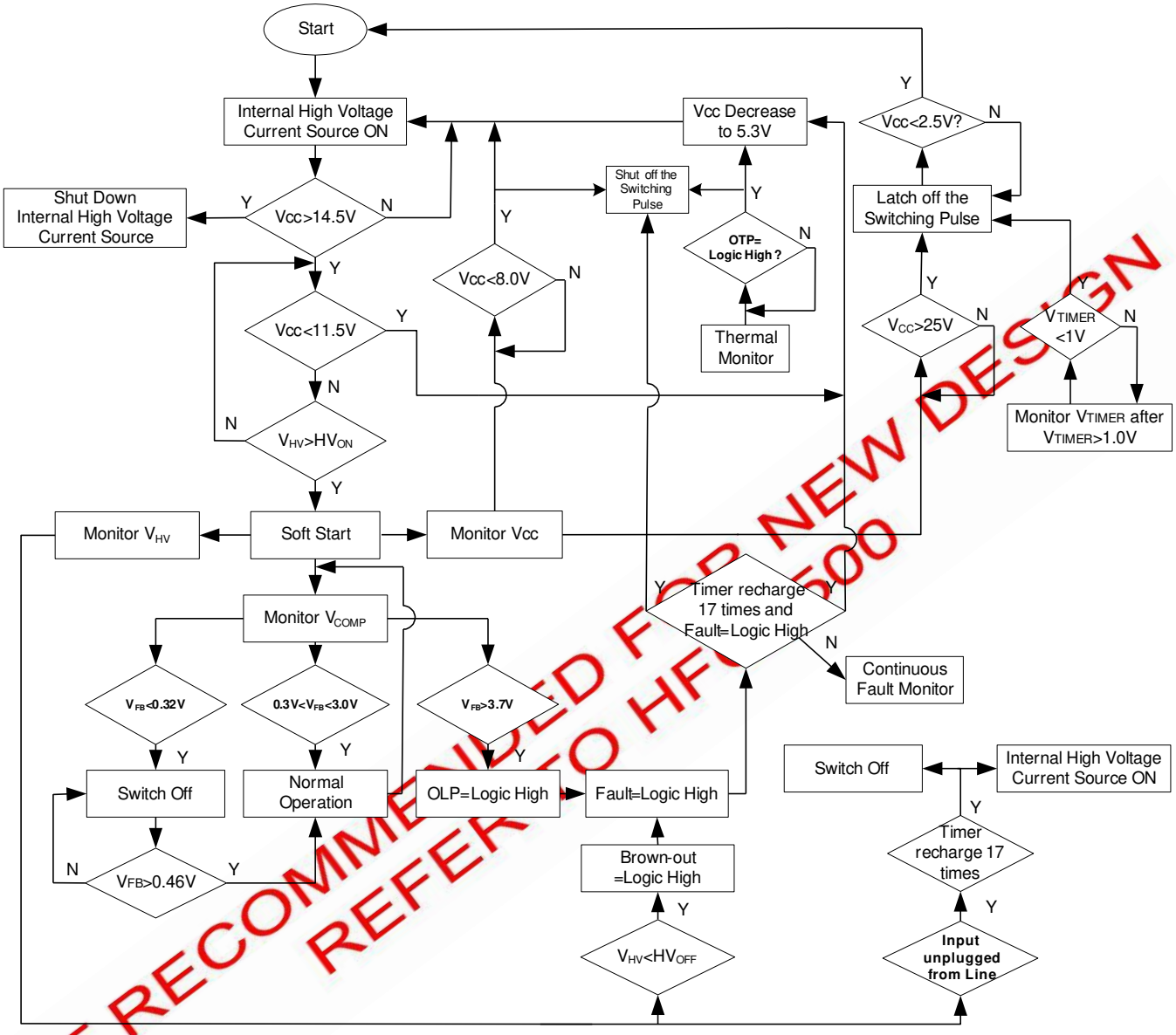
b) Winding Diagram

Figure 17: Transformer Structure

Table 2—Winding Order

Tape (T)	Winding	Margin Wall PRI side	Terminal Start—>End	Margin Wall SEC side	Wire Size (φ)	Turns (T)
1	N1	2mm	3—>2	2mm	0.27mm*2	28
1	N6	2mm	1—>NC	2mm	0.3mm*1	20
3	N4	2mm	7,8—>9,10	2mm	0.33mm*12	3
1	N3	2mm	11,12—>7,8	2mm	0.33mm*5	6
3						
1	N2	2mm	5—>6	2mm	0.27mm*1	9
2	N5	2mm	2—>1	2mm	0.27mm*2	29

FLOW CHART



UVLO, brown-out, OTP & OLP is auto restart, OVP on VCC and Latch-off on TIMER are latch mode

Release from the latch condition , need to unplug from the main input .

Figure 18: Control Flow Chart

EVOLUTION OF THE SIGNALS IN PRESENCE OF FAULTS

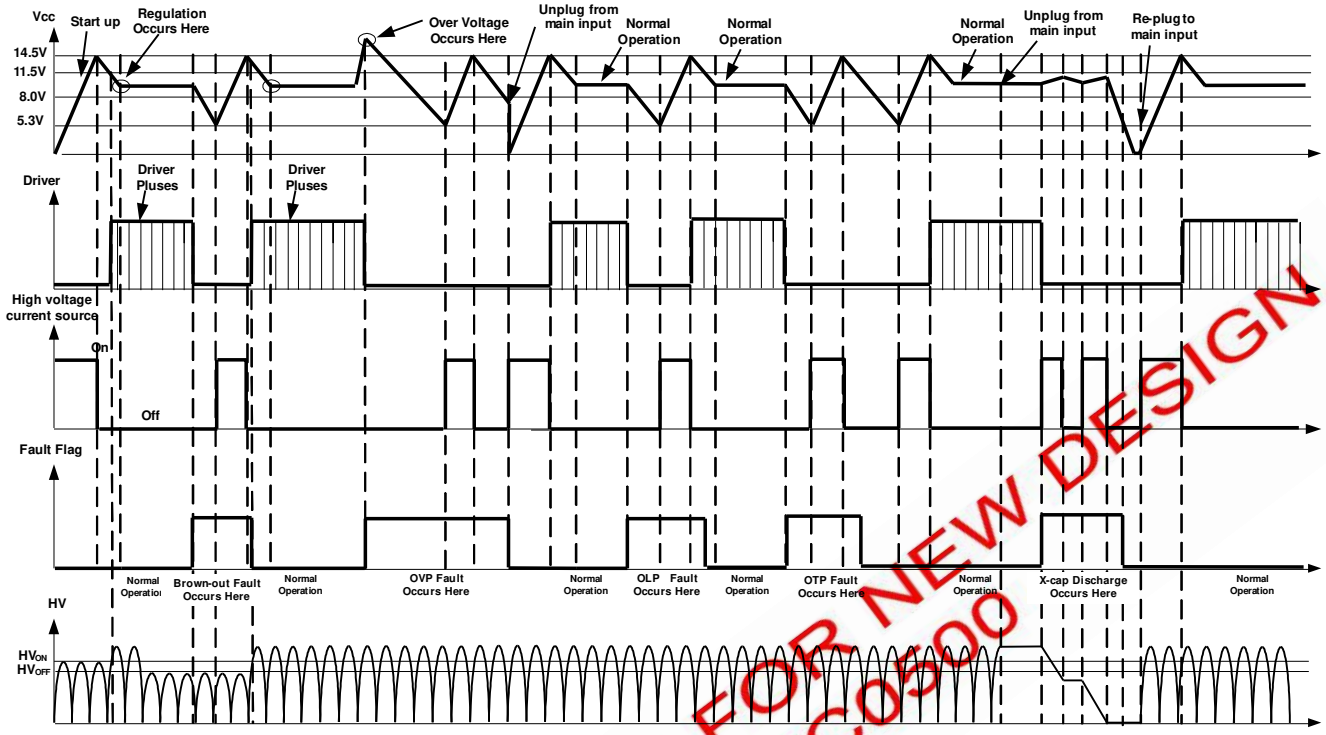
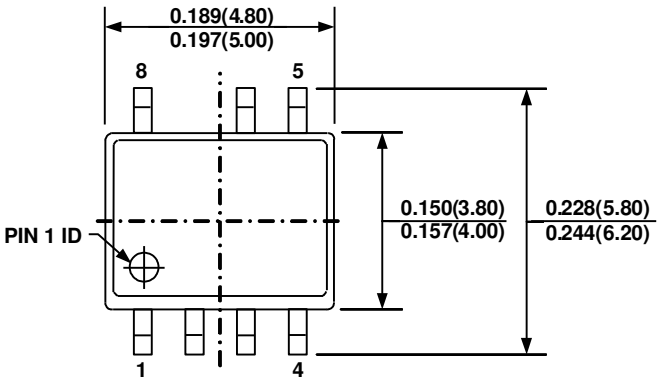


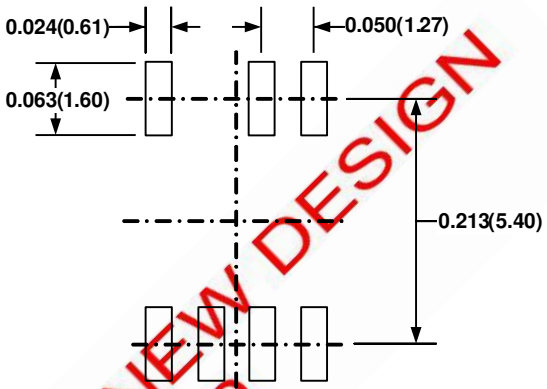
Figure 19: Signal Evolution in the Presence of Faults

PACKAGE INFORMATION

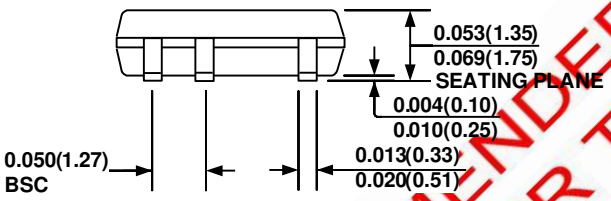
SOIC8-7A



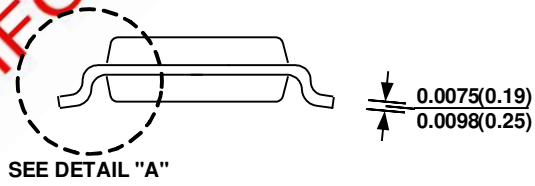
TOP VIEW



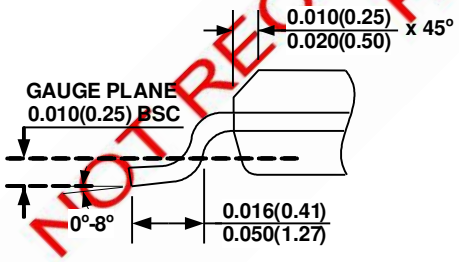
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE