

RoHS

COMPLIANT HALOGEN

FREE

**Vishay Siliconix** 

## N-Channel 30 V (D-S) MOSFET

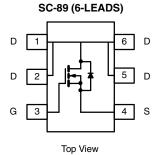
PRODU	CT SUMMARY		
V <sub>DS</sub> (V)	<b>R<sub>DS(on)</sub> (</b> Ω <b>)</b>	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
30	0.099 at V <sub>GS</sub> = 4.5 V	1.2 <sup>a</sup>	3.5
50	0.140 at $V_{GS}$ = 2.5 V	1.0	0.0

#### **FEATURES**

- Halogen-free According to IEC 61249-2-21
  Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

#### APPLICATIONS

Load Switch for Portable Devices



Marking Code

Ordering Information: Si1070X-T1-GE3 (Lead (Pb)-free and Halogen-free)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V <sub>DS</sub>	30	v
Gate-Source Voltage		V <sub>GS</sub>	± 12	v
Continuous Droin Current (T 150 °C)	T <sub>A</sub> = 25 °C		1.2 <sup>b, c</sup>	
Continuous Drain Current $(T_J = 150 \ ^{\circ}C)^a$	T <sub>A</sub> = 70 °C		1 <sup>b, c</sup>	•
Pulsed Drain Current		I <sub>DM</sub>	6	— A
Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	9	
Repetitive Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	4.01	mJ
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	0.2 <sup>b, c</sup>	А
	T <sub>A</sub> = 25 °C	P-	0.236 <sup>b, c</sup>	w
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 70 °C	P <sub>D</sub>	0.151 <sup>b, c</sup>	v
Operating Junction and Storage Temperature Ra	ange	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Manimum hunsting to Americanth d	t ≤ 5 s	R <sub>thJA</sub>	440	530	°C/W
Maximum Junction-to-Ambient <sup>b, d</sup>	Steady State	' 'thJA	540	650	

Notes:

a. Based on  $T_C = 25$  °C.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 5 s.

d. Maximum under steady state conditions is 650  $^{\circ}\text{C/W}.$ 

## Si1070X

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static			•	•	•	•	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_D = 250 \mu A$	30			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA		24.5		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_{\rm D} = 230 \ \mu \text{A}$		- 3.81		mv/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	0.7		1.55	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 12 V$			± 100	nA	
Zara Cata Valtaga Drain Current		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1	nA	
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 85 ^{\circ}\text{C}$			10	μΑ	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS}$ = $\geq$ 5 V, $V_{GS}$ = 4.5 V	6			A	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 1.2 A		0.082	0.099		
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 1.0 A		0.116	0.140	Ω	
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1.2 A		5		S	
Dynamic <sup>b</sup>			•		•	•	
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		385		pF	
Output Capacitance	C <sub>oss</sub>			55			
Reverse Transfer Capacitance	C <sub>rss</sub>			30			
Tatal Oata Obarra	0	$V_{DS} = 15 \text{ V}, V_{GS} = 5 \text{ V}, I_D = 1.2 \text{ A}$		3.8	8.3		
Total Gate Charge	Qg			3.5	4.1		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS}$ = 15 V, $V_{GS}$ = 4.5 V, $I_{D}$ = 4.6 A		1.1		nC	
Gate-Drain Charge	Q <sub>gd</sub>			0.98			
Gate Resistance	Rg	f = 1 MHz		4.7	6.2	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			10	15		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 15 $\Omega$		22	33	ns	
Turn-Off DelayTime	t <sub>d(off)</sub>	$\text{I}_\text{D}\cong$ 1.0 A, $\text{V}_\text{GEN}$ = 4.5 V, $\text{R}_\text{g}$ = 1 $\Omega$		14	21		
Fall Time	t <sub>f</sub>			6	9		
Drain-Source Body Diode Characterist	ics						
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				6	A	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 1.2 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			19.4	29.5	nC	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			18.43	27.5		
Reverse Recovery Fall Time	ta	—— I <sub>F</sub> = 3.8 A, dl/dt = 100 A/μs		16.4		ns	
Reverse Recovery Rise Time	t <sub>b</sub>			3		1	

Notes:

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

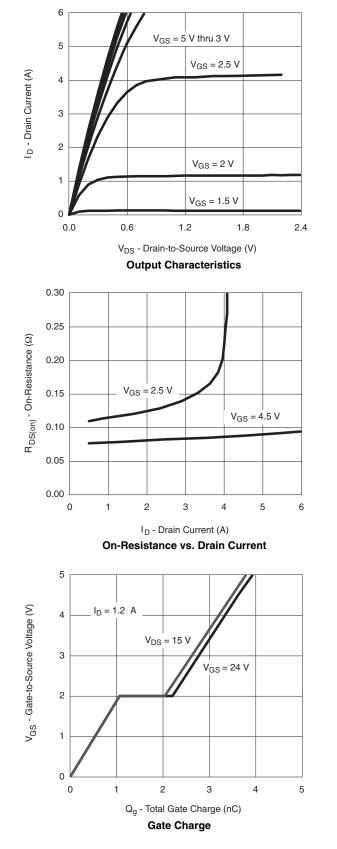
b. Guaranteed by design, not subject to production testing.

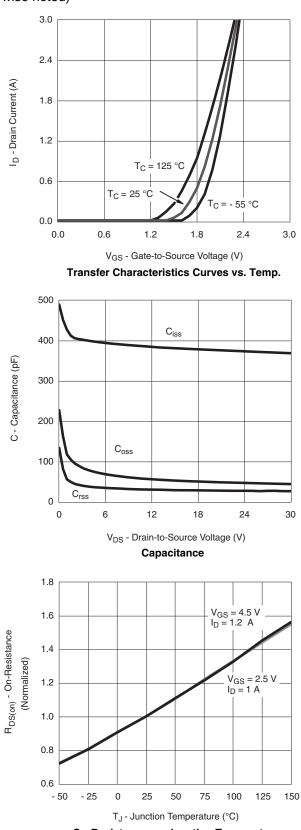
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



### Si1070X Vishay Siliconix

#### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)





**On-Resistance vs. Junction Temperature** 

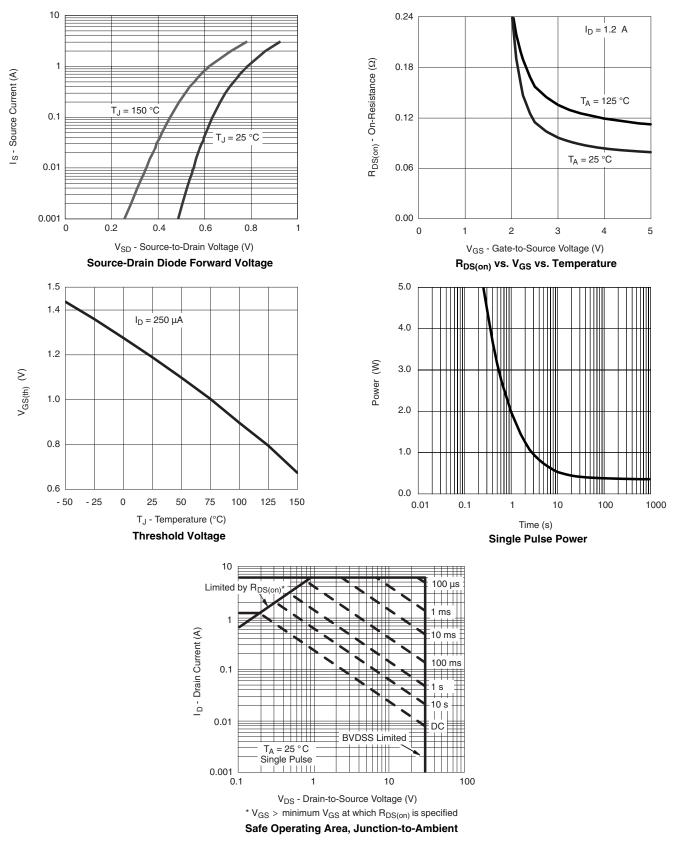
Document Number: 73893 S10-2542-Rev. D, 08-Nov-10

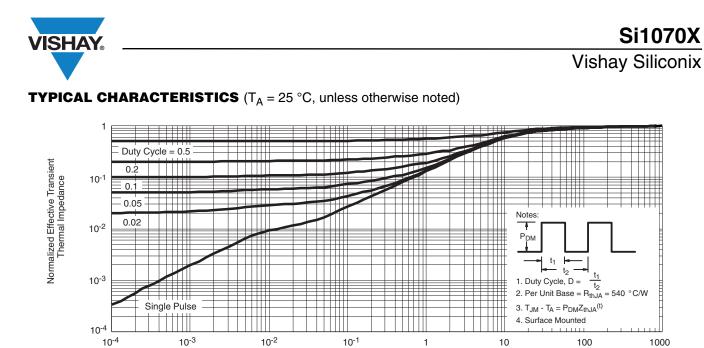
## Si1070X

#### Vishay Siliconix



#### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)





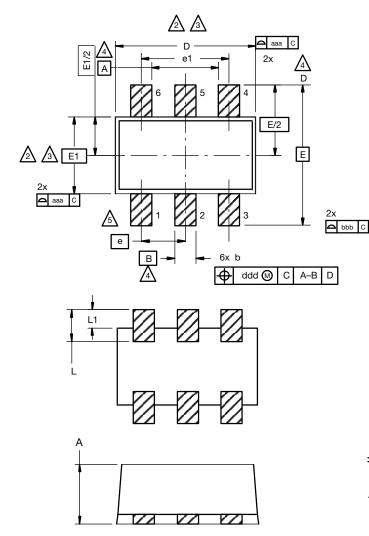
Square Wave Pulse Duration (s) Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?73893">www.vishay.com/ppg?73893</a>.



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#### SC-89 6-Leads (SOT-563F)



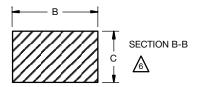
Notes

- 1. Dimensions in millimeters.
- Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.
- Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

A Datums A, B and D to be determined 0.10 mm from the lead tip.

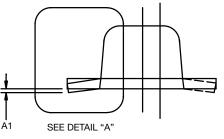
A Terminal numbers are shown for reference only.

These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.









DIM.	MILLIMETERS			
	MIN.	NOM.	MAX.	
А	0.56	0.58	0.60	
A1	0	0.02	0.10	
b	0.15	0.22	0.30	
С	0.10	0.14	0.18	
D	1.50	1.60	1.70	
E	1.50	1.60	1.70	
E1	1.15	1.20	1.25	
е	0.45	0.50	0.55	
e1	0.95	1.00	1.05	
L	0.25	0.35	0.50	
L1	0.10	0.20	0.30	
C14-0439-Rev DWG: 5880	/. C, 11-Aug-14			

Revision: 11-Aug-14

1 For technical questions, contact: <u>analogswitchtechsupport@vishay.com</u> Document Number: 71612

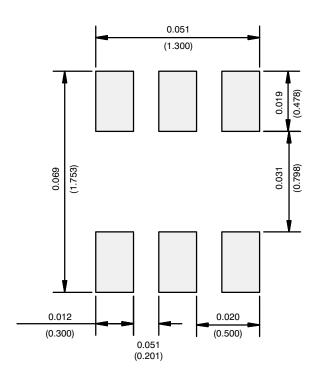
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# Application Note 826

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#### **RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)

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