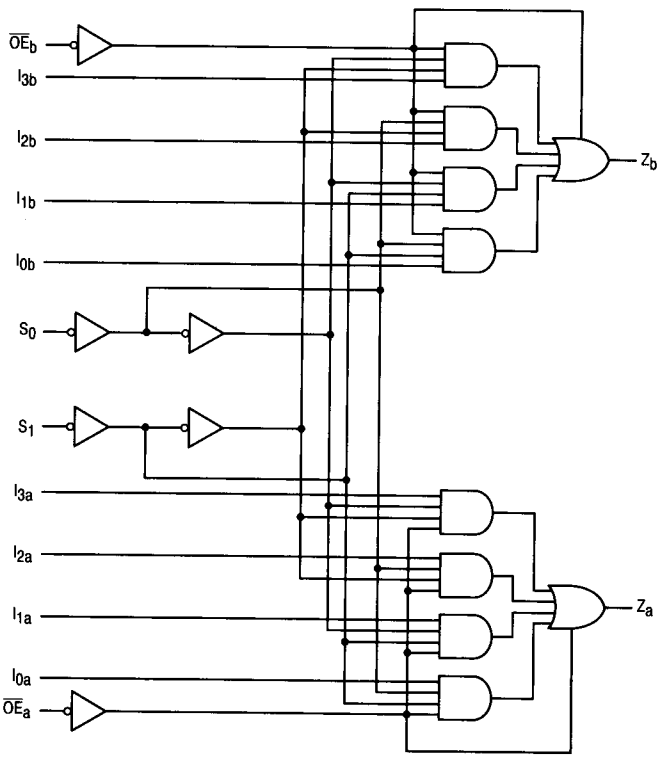
MOTOROLA

Dual 4-Input Data Selector/Multiplexer With 3-State Outputs

ELECTRICALLY TESTED PER:
MIL-M-38510/33908

The 54F253 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high-impedance state with a HIGH on the respective Output Enable $\overline{OE}$ inputs, allowing the outputs to interface directly with bus oriented systems.

LOGIC DIAGRAM



Military 54F253

AVAILABLE AS:

1) JAN: JM38510/33908BXA
2) SMD: N/A
3) 883: 54F253/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
$\overline{OE}_a$	1	1	2	V_{CC}
S_1	2	2	3	V_{CC}
I_{3a}	3	3	4	V_{CC}
I_{2a}	4	4	5	V_{CC}
I_{1a}	5	5	7	V_{CC}
I_{0a}	6	6	8	V_{CC}
Z_a	7	7	9	OPEN
GND	8	8	10	GND
Z_b	9	9	12	OPEN
I_{0b}	10	10	13	V_{CC}
I_{1b}	11	11	14	V_{CC}
I_{2b}	12	12	15	V_{CC}
I_{3b}	13	13	17	V_{CC}
S_0	14	14	18	V_{CC}
$\overline{OE}_b$	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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FUNCTIONAL DESCRIPTION

The F253 contains two identical 4-Input Multiplexers with 3-state Outputs. They select two bits from four sources selected by common Select Inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which when HIGH, force the outputs to a high impedance (high Z) state.

The F253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$Z_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{0b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0).$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

Select Inputs		Inputs (a or b)					Output
S_0	S_1	$\overline{OE}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	(Z)
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance (off)
Address inputs S_0 and S_1 are common to both sections.

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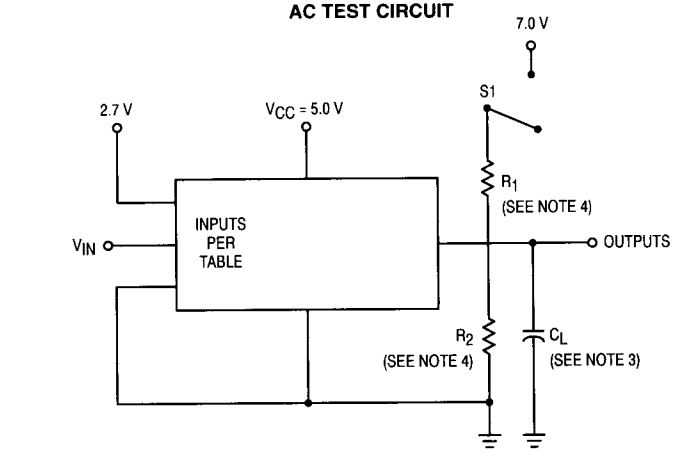
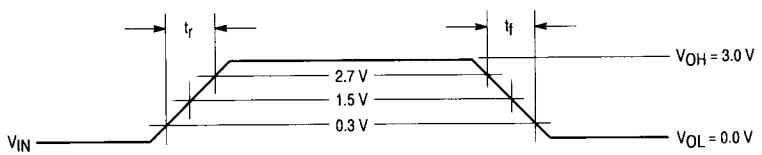
AC TEST CIRCUIT

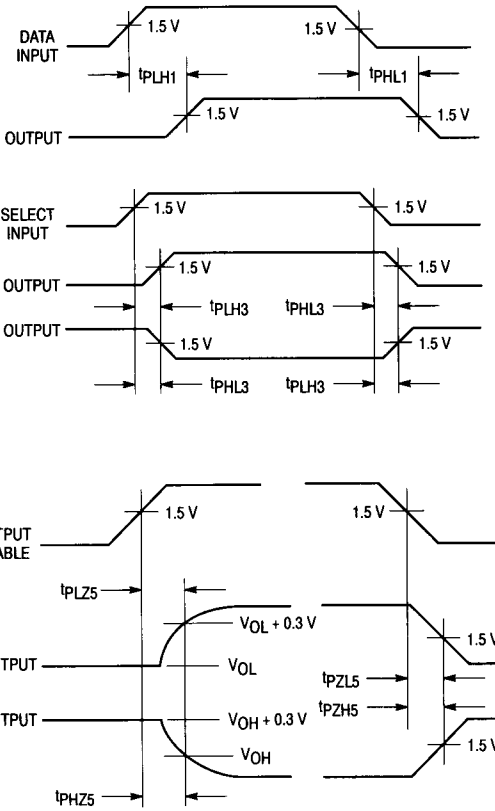




Test Type	S1
t_{PLH}	open
t_{PHL}	open
t_{PHZ}	open
t_{PZH}	open
t_{PLZ}	closed
t_{PZL}	closed

REFERENCE NOTES ON PAGE 4-130

WAVEFORMS



NOTES

1. V_{IN} = input pulse and has the following characteristics: PRR ≤ 1.0 MHz, $t_r = t_f \leq 2.5$ ns, $Z_{OUT} \approx 50\ \Omega$.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. $C_L = 50$ pF ± 10%, including scope probe, wiring and stray capacitance without package in test fixture.
4. $R_1 = R_2 = 499\ \Omega \pm 5.0\%$.
5. Voltage measurements are to be made with respect to network ground terminal.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		− 55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = −3.0 mA, V_{IH} = 2.0 V, S = 0.8 V or 2.0 V, $\overline{OE}$ = 0.8 V or open.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IL} = 0.8 V, S = 0.8 V or 2.0 V, $\overline{OE}$ = 0.8 V or open.
V_{IC}	Input Clamp Diode		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open, S = 4.5 V, 0 V or (2.7 V).
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs are open, S = 4.5 V, 0 V or (7.0 V).
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V, other inputs are open, S = 4.5 V, 0 V or (0.5 V).
I_{OD}	Diode Current	35		35		35		mA	V_{CC} = 4.5 V, V_{IN} = 0 V, S = 0 V, other inputs are open, V_{OUT} = 2.5 V, $\overline{OE}$ = 0 V.
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, all other inputs are open, V_{OUT} = 0 V, S = 0 V, $\overline{OE}$ = 0 V.
I_{OZH}	Output Off Current High		50		50		50	µA	V_{CC} = 5.5 V, V_{IN} = 0 V, all other inputs are open, V_{OUT} = 2.7 V, S = 0 V, $\overline{OE}$ = 2.0 V.
I_{OZL}	Output Off Current Low		−50		−50		−50	µA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, all other inputs are open, V_{OUT} = 0.5 V, S = 4.5 V, $\overline{OE}$ = 2.0 V.
I_{CCH}	Power Supply Current		16		16		16	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V or 0 V (all inputs).
I_{CCL}	Power Supply Current		23		23		23	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs).
I_{CCZ}	Power Supply Current		23		23		23	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs), $\overline{OE}$ = 4.5 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, (**Repeat at**), V_{CC} = 5.5 V, V_{INL} = 0.5 V, and V_{INH} = 2.4 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output I_n to Z_n	2.5	7.0	2.5	8.0	2.5	8.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH1}	Propagation Delay /Data-Output I_n to Z_n	3.0	7.0	2.5	9.0	2.5	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHL3}	Propagation Delay /Data-Output S_n to Z_n	3.0	9.0	2.5	11	2.5	11	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH3}	Propagation Delay /Data-Output S_n to Z_n	4.5	11.5	3.5	15	3.5	15	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PZH5}	Propagation Delay /Data-Output I_n or S_n to Z_n	3.0	8.0	2.5	10	2.5	10	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PZL5}	Propagation Delay /Data-Output I_n or S_n to Z_n	3.0	8.0	2.5	10	2.5	10	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHZ5}	Propagation Delay /Data-Output I_n or S_n to Z_n	2.0	5.0	2.0	6.5	2.0	6.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLZ5}	Propagation Delay /Data-Output I_n or S_n to Z_n	2.0	6.0	2.0	8.0	2.0	8.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.