High Frequency 1-A Synchronous Buck/Boost Converter

DESCRIPTION

The Si9169 provides fully integrated synchronous buck or boost converter solution for the latest one cell Lithium Ion cellular phones. Capable of delivering up to 1 A of output current at + 3.6 V, the Si9169 provides ample power for various baseband circuits as well as for some PAs. It combines the 2 MHz switching controller with fully integrated high-frequency MOSFETs to deliver the smallest and most efficient converter available today. The 2 MHz switching frequency reduces the inductor height to new level of 2 mm and minimizes the output capacitance requirement to less than 10 µF with peak-to-peak output ripple as low as 10 mV. Combined with low-gate charge high-frequency MOSFETs, the Si9169 delivers efficiency up to 95 %. The programmable pulse skipping mode maintains this high efficiency even during the standby and idle modes to increase overall battery life and talktime. In order to extract the last ounce of power from the battery, the Si9169 is designed with 100 % duty cycle control for buck mode. With 100 % duty cycle, the Si9169 operates like a saturated linear regulator to deliver the highest potential output voltage for longer talktime.

Si9169 can be a drop-in replacement of Si9165 provided Pin 1 is not connected. For full 1 A load condition, Pin 1 is required to be connected to low power controller ground.

The Si9169 is available in lead (Pb)-free TSSOP-20 pin package. In order to satisfy the stringent ambient temperature requirements, the Si9169 is rated to handle the industrial temperature range of - 25 °C to 85 °C and - 40 °C to 85 °C.

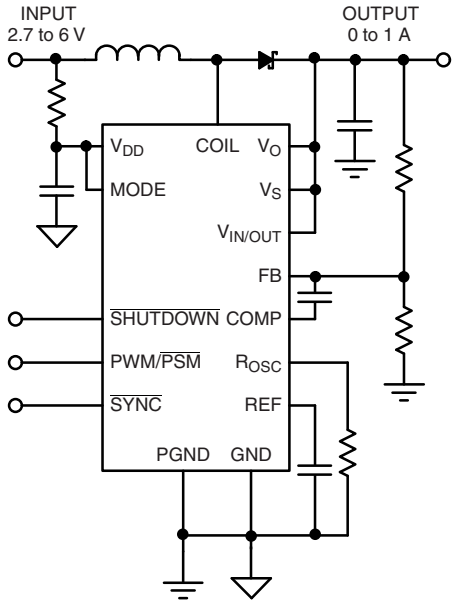
FEATURES

Pb-free

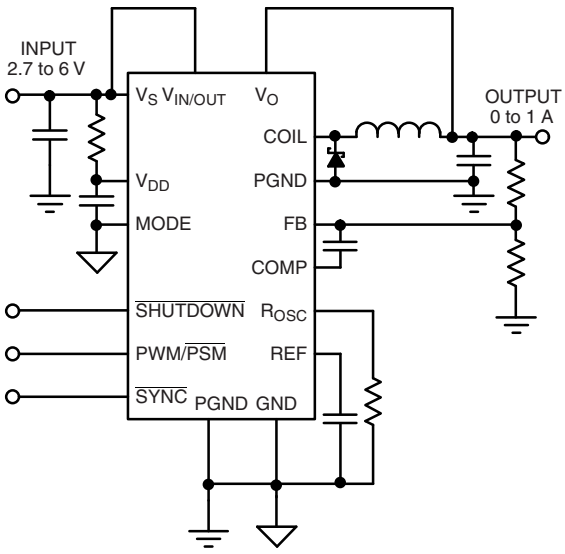
RoHS COMPLIANT

- Voltage Mode Control
- Fully Integrated MOSFET Switches
- 2.7 V to 6 V Input Voltage Range
- Programmable PWM/$\overline{\text{PSM}}$ Control
  - Up to 1 A Output Current at 3.6 V in PWM
  - Up to 2 MHz Adjustable Switching Frequency in PWM
  - Less than 200 µA Quiescent Current in $\overline{\text{PSM}}$
- Integrated UVLO and POR
- Integrated Soft-Start
- Synchronization
- Shutdown Current < 1 µA

FUNCTIONAL BLOCK DIAGRAM



Boost Configuration



Buck Configuration

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Voltages Referenced to GND			
V_{DD}		6.5	V
MODE PWM/$\overline{PSM}$, SYNC, $\overline{SD}$, V_{REF}, R_{OSC}, COMP, FB		- 0.3 V to V_{DD} + 0.3 V	
V_O		- 0.3 V to V_S + 0.3 V	
PGND		± 0.3	
Voltages Referenced to PGND			
V_S, $V_{IN/OUT}$		6.5	V
COIL		- 0.4 V to $V_{IN/OUT}$ + 0.4 V	
Peak Output Current		3 A for 1 ms	
Continuous Output Current		1.4	A
Storage Temperature Range		- 65 to 150	°C
Operating Junction Temperature		150	
Power Dissipation (Package)[a]	20-Pin TSSOP (Q Suffix)[b]	1.0	W
Thermal Impedance (Θ_{JA})	20-Pin TSSOP[c]	90	°C/W

Notes:
a. Device Mounted with all leads soldered or welded to PC board.
b. Derate 11 mW/°C above 60 °C.
c. With Pin 1 connected to GND plane.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Limit	Unit
Voltages Referenced to GND		
V_{DD}	2.7 V to 6 V V	V
MODE, PWM/$\overline{PSM}$, SYNC, $\overline{SD}$	0 V to V_{DD}	
Voltages Referenced to PGND		
V_S, $V_{IN/OUT}$	2.7 V to 6 V	V
F_{OSC}	200 kHz to 2 MHz	
R_{OSC}	25 kΩ to 300 kΩ	kΩ
V_{REF} Capacitor	0.1	µF

SPECIFICATIONS

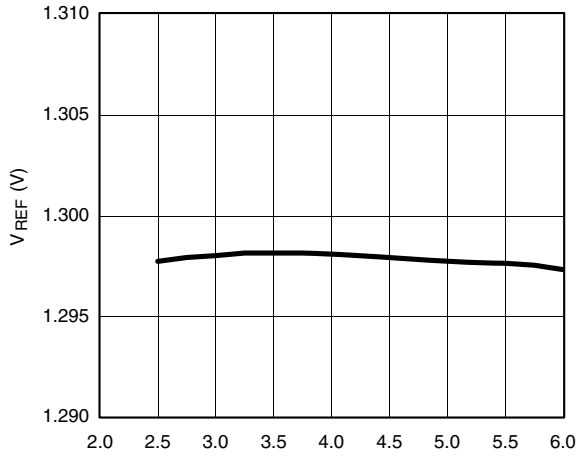
Parameter	Symbol	Test Conditions Unless Otherwise Specified 2.7 V < V_{DD} < 6 V, $V_{IN/OUT}$ = 3.3 V, V_S = 3.3 V	Limits[e] Min[a]	Typ[b]	Max[a]	Unit
Reference						
Output Voltage	V_{REF}	I_{REF} = 0 A	1.265	1.3	1.330	V
		T_A = 25 °C, I_{REF} = 0	1.280	1.3	1.320	
Load Regulation	ΔV_{REF}	V_{DD} = 3.3 V, - 500 µA < I_{REF} < 0		3		mV
Power Supply Rejection	P_{SRR}			60		dB
UVLO						
Under Voltage Lockout (turn-on)	$V_{UVLO/LH}$		2.3	2.4	2.5	V
Hysteresis	V_{HYS}	V_{UVLOLH} - V_{UVLOHL}		0.1		
Soft-Start Time						
SS Time	t_{SS}			6		ms
Mode						
Logic High	V_{IH}		0.7 V_{DD}			V
Logic Low	V_{IL}				0.3 V_{DD}	
Input Current	I_L		- 1.0		1.0	µA

SPECIFICATIONS

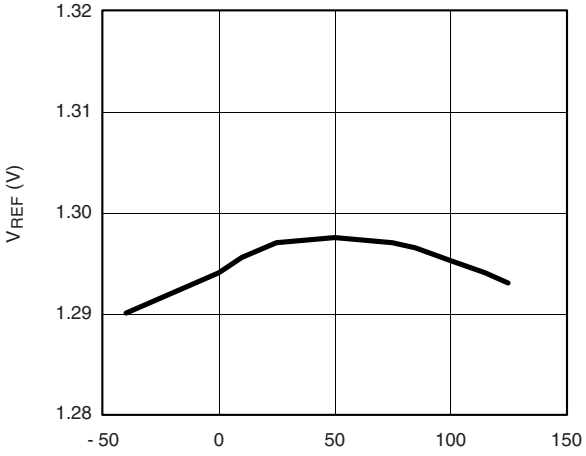
Parameter		Symbol	Test Conditions Unless Otherwise Specified 2.7 V < V_{DD} < 6 V, $V_{IN/OUT}$ = 3.3 V, V_S = 3.3 V		Limits[e] Min[a]	Typ[b]	Max[a]	Unit
$\overline{SD}$, SYNC, PWM/$\overline{PSM}$								
Logic High		V_{IH}			2.4			V
Logic Low		V_{IL}					0.8	
Input Current		I_L			- 1.0		1.0	µA
Oscillator								
Maximum Frequency		F_{MAX}			2			MHz
Accuracy			Nominal 1.60 MHz, R_{OSC} = 30 kΩ		- 20		20	%
Maximum Duty Cycle (Buck, Non LDO Mode)		D_{MAX}	F_{SW} = 2 MHz	Si9169BQ	75	85		
				Si9169DQ	73	85		
Maximum Duty Cycle (Boost)				Si9169BQ	52	65		
				Si9169DQ	50	65		
SYNC Range		F_{SYNC}/F_{OSC}			1.2		1.5	
SYNC Low Pulse Width					50			ns
SYNC High Pulse Width					50			
SYNC t_r, t_f							50	
Error Amplifier								
Input Bias Current		I_{BIAS}	V_{FB} = 1.5 V		- 1		1	µA
Open Loop Voltage Gain		A_{VOL}			50	60		dB
FB Threshold		V_{FB}	T_A = 25 °C		1.270	1.30	1.330	V
					1.255	1.30	1.340	
Unity Gain BW		BW				2		MHz
Output Current		I_{EA}	Source (V_{FB} = 1.05 V), V_{COMP} = 0.75 V			- 3	- 1	mA
			Sink (V_{FB} = 1.55 V), V_{COMP} = 0.75 V		1	3		
Output Current								
Output Current (PWM)	Boost Mode[c]	I_{OUT}	$V_{OUT} \le 4.2$ V		1000			mA
	Buck Mode[d]		1.8 V ≤ V_{OUT} ≤ 5.0 V		1000			
Output Current ($\overline{PSM}$)	Boost Mode[c]		V_{IN} = 3.3 V, V_{OUT} = 3.6 V		150			
	Buck Mode[d]		V_{IN} = 3.6 V, V_{OUT} = 2.7 V		150			
$r_{DS(on)}$ N-Channel		$r_{DS(on)}$	$V_S \ge 3.3$ V			130	300	mΩ
$r_{DS(on)}$ P-Channel						160	330	
Over Temperature Protection								
Trip Point			Rising Temperature			165		°C
Hysteresis						25		
Supply								
Normal Mode		I_{DD}	V_{DD} = 3.3 V, F_{OSC} = 2 MHz			500	750	µA
$\overline{PSM}$ Mode			V_{DD} = 3.3 V			180	250	
$\overline{Shutdown}$ Mode			V_{DD} = 3.3 V, $\overline{SD}$ = 0 V				1	

Notes:
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. $V_{IN} = V_{DD}$, $V_{OUT} = V_{IN/OUT} = V_S = V_O$, L = 1.5 µH, $V_{IN} \le V_{OUT}$
d. $V_{IN} = V_{DD} = V_S = V_{IN/OUT}$, $V_{OUT} = V_O$, L = 1.5 µH, $V_{IN} \ge V_{OUT}$
e. Limits are for both Si9169BQ (- 25 °C to 85 °C) and Si9169DQ (- 40 °C to 85 °C) unless otherwise noted.

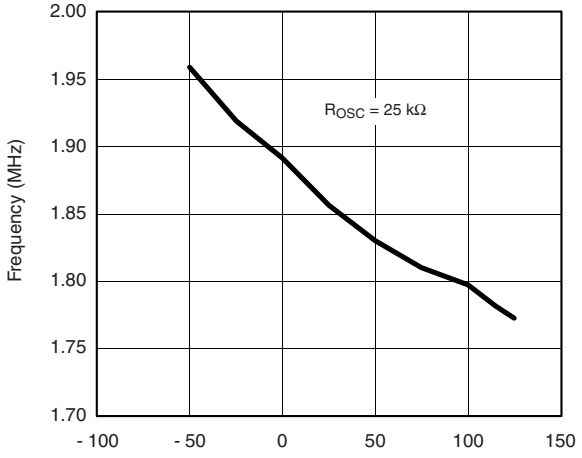
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



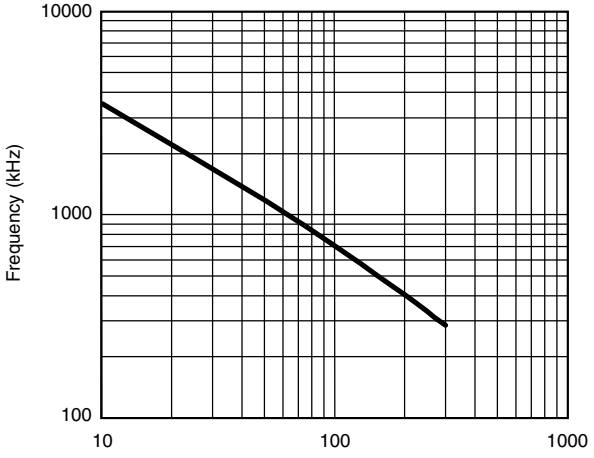
V_{REF} vs. V_{DD}



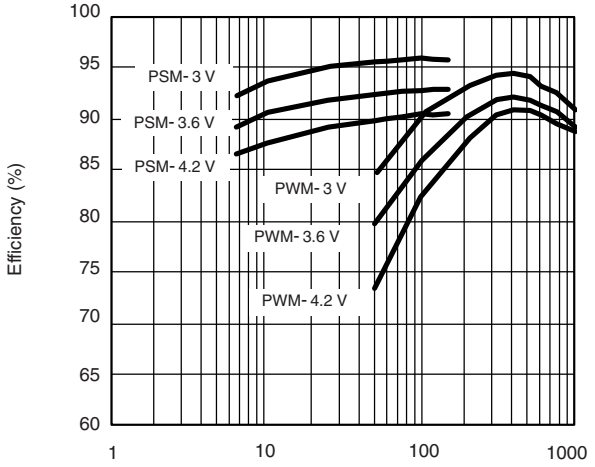
V_{REF} vs. Temperature



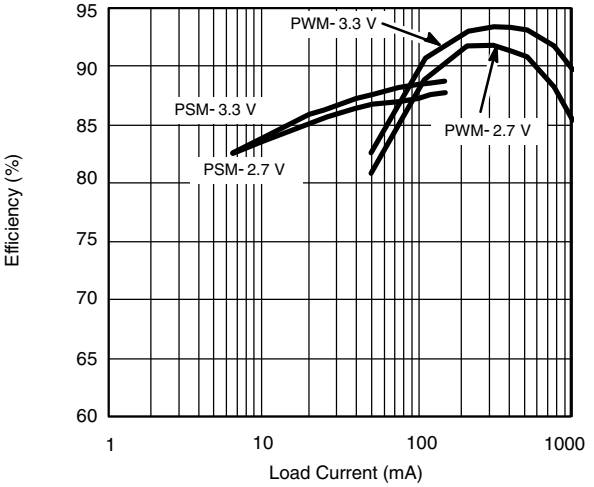
Frequency vs. Temperature



Frequency vs. R_{OSC}

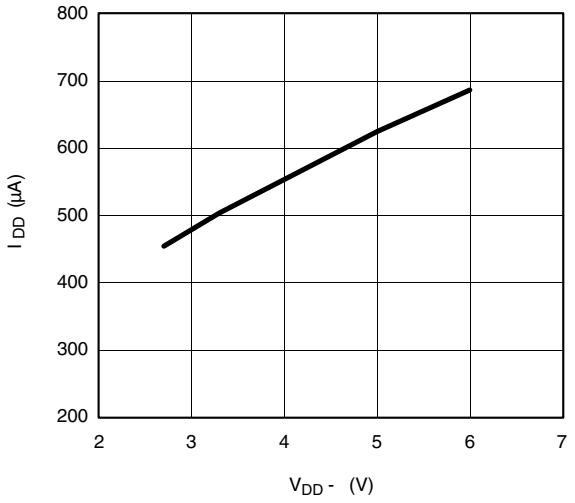


Buck Mode Efficiency, V_O = 2.7 V

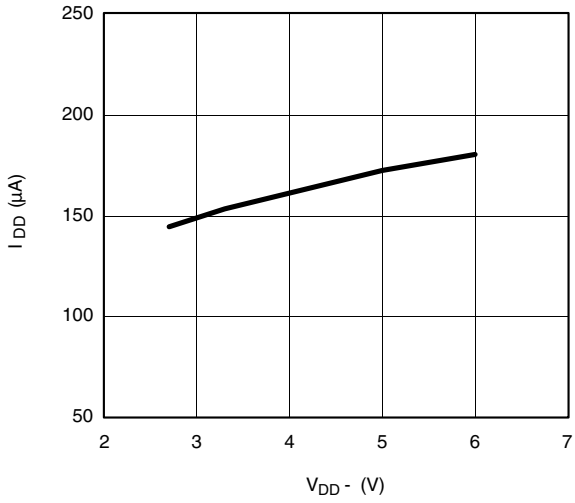


Boost Mode Efficiency, V_O = 3.6 V

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

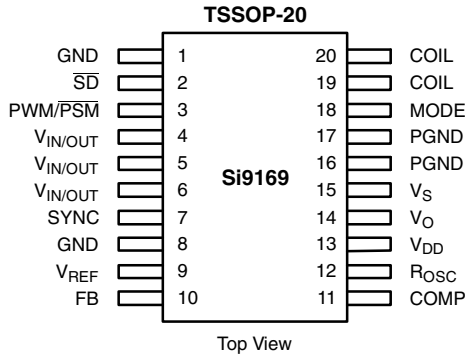


PWM Supply Current



PSM Supply Current

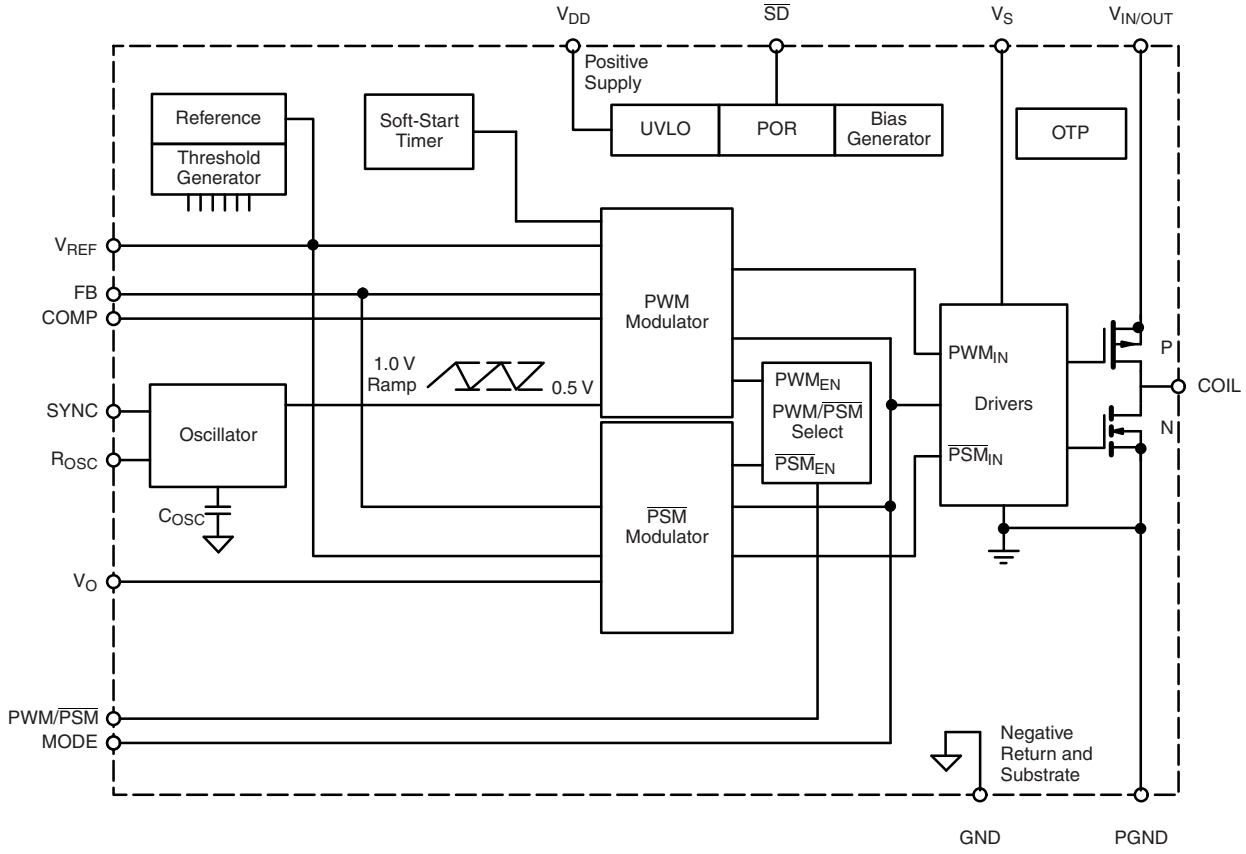
PIN CONFIGURATION AND ORDERING INFORMATION



ORDERING INFORMATION		
Part Number	**Temperature Range**	**Package**
Si9169BQ-T1-E3	- 25 to 85 °C	Tape and Reel
Si9169DQ-T1-E3	- 40 to 85 °C	

PIN DESCRIPTION		
Pin Number	**Name**	**Function**
1	GND	Low power controller ground. Can be left unconnected for load currents below 600 mA.
2	$\overline{SD}$	Shuts down the IC completely and decreases current consumed by the IC to < 1 µA.
3	PWM/$\overline{PSM}$	Logic high = PWM mode, logic low = $\overline{PSM}$ mode. In $\overline{PSM}$ mode, synchronous rectification is disabled.
4, 5, 6	$V_{IN/OUT}$	Input node for buck mode and output node for boost mode.
7	SYNC	Externally controlled synchronization signal. Logic high to low transition forces the clock synchronization. *If not used, the pin must be connected to V_{DD}, or logic high.*
8	GND	Low power controller ground
9	V_{REF}	1.3 V reference. Decoupled with 0.1 µF capacitor.
10	FB	Output voltage feedback connected to the inverting input of an error amplifier.
11	COMP	Error amplifier output for external compensation network.
12	Rosc	External resistor to determine the switching frequency.
13	V_{DD}	Input supply voltage for the analog circuitry. Input voltage range is 2.7 V to 6 V.
14	V_O	Direct output voltage sensing to control peak inductor current in PSM mode.
15	V_S	Supply voltage for the internal MOSFET drive circuit.
16, 17	PGND	Power ground.
18	MODE	Determines the converter topology. Connect to AGND for buck or V_{DD} for boost.
19, 20	COIL	Inductor connection node

FUNCTIONAL BLOCK DIAGRAM



DETAIL OPERATIONAL DESCRIPTION

Start-Up

The UVLO circuit prevents the internal MOSFET switches and oscillator circuit from turning on, if the voltage on V_{DD} pin is less than 2.5 V. With typical UVLO hysteresis of 0.1 V, controller is continuously powered on until the V_{DD} voltage drops below 2.4 V. This hysteresis prevents the converter from oscillating during the start-up phase and unintentionally locking up the system. Once the V_{DD} voltage exceeds the UVLO threshold, and with no other shutdown condition detected, an internal Power-On-Reset timer is activated while most circuitry, except the output driver, are turned on. After the POR timeout of about 1 ms, the internal soft-start capacitor is allowed to charge. When the soft-start capacitor voltage reaches 0.5 V, the PWM circuit is enabled. Thereafter, the constant current charging the soft-start capacitor will force the output voltage to rise gradually without overshooting. *To prevent negative undershoot, the synchronous switch is tri-stated until the duty cycle reaches about 10 %*. In tri-state, the high-side P-Channel MOSFET is turned off by pulling up the gate voltage to V_S potential. The low-side N-Channel MOSFET is turned off by pulling down the gate voltage to PGND potential. Note that the Si9169 will always soft starts in the PWM mode regardless of the voltage level on the PWM/$\overline{PSM}$ pin.

Shutdown

The Si9169 is designed to conserve as much battery life as possible by decreasing current consumption of IC during normal operation as well as the shutdown mode. With logic low level on the $\overline{SD}$ pin, current consumption of the Si9169 is decreased to less than 1 µA by shutting off most of the circuits. The logic high enables the controller and starts up as described in "Start-Up" section above.

DETAIL OPERATIONAL DESCRIPTION (CONT'D)

Over Temperature Protection

The Si9169 is designed with over temperature protection circuit to prevent MOSFET switches from running away. If the temperature reaches 165 °C, internal soft-start capacitor is discharged, shutting down the output stage. Converter remains in the disabled mode until the temperature in the IC decreases below 140 °C.

PWM Mode

With PWM/$\overline{\text{PSM}}$ mode pin in logic high condition, the Si9169 operates in constant frequency (PWM) mode. As the load and line varies, switching frequency remain constant. The switching frequency is programmed by the Rosc value as shown by the Oscillator curve. In the PWM mode, the synchronous drive is always enabled, even when the output current reaches 0 A to assure the converter is operating in continuous current mode. In continuous current mode, transfer function of the converter remain constant, providing fast transient response. If the converter operates in discontinuous current mode, overall loop gain decreases and transient response time can be ten times longer than if the converter remain in continuous current mode. This transient response time advantage can significantly decrease the hold-up capacitors needed on the output of dc-dc converter to meet the transient voltage regulation. Therefore, the PWM/$\overline{\text{PSM}}$ pin is available to dynamically program the controller.

The maximum duty cycle of the Si9169 can reach 100 % in buck mode. This allows the system designers to extract out the maximum stored energy from the battery. Once the controller delivers 100 % duty cycle, converter operates like a saturated linear regulator. At 100 % duty cycle, synchronous rectification is completely turned off. Up to a maximum duty cycle of 80 % at 2 MHz switching frequency, controller maintains perfect output voltage regulation. If the input voltage drops below the level where the converter requires greater than 80 % duty cycle, controller will deliver 100 % duty cycle. This instantaneous jump in duty cycle is due to fixed BBM time, MOSFET delay/rise/fall time, and the internal propagational delays. In order to maintain regulation, controller might fluctuate its duty cycle back and forth from 100 % to something less than maximum duty cycle while the converter is operating in this input voltage range. If the input voltage drops further, controller will remain on 100 %. If the input voltage increases to a point where it requires less than 80 % duty cycle, synchronous rectification is once again activated.

The maximum duty cycle under boost mode is internally limited to 75 % to prevent inductor saturation. If the converter is turned on for 100 % duty cycle, inductor never gets a chance to discharge its energy and eventually saturates.

In boost mode, synchronous rectifier is always turned on for minimum or greater duration as long as the switch has been turned on. The controller will deliver 0 % duty cycle, if the input voltage is greater than the programmed output voltage. Because of signal propagation time and MOSFET delay/rise/fall time, controller will not transition smoothly from minimum controllable duty cycle to 0 % duty cycle. For example, controller may decrease its duty cycle from 5 % to 0 % abruptly, instead of gradual decrease you see from 75 % to 5 %.

Pulse Skipping Mode

The gate charge losses produced from the Miller capacitance of MOSFETs are the dominant power dissipation parameter during light load (i.e. < 10 mA). Therefore, less gate switching will improve overall converter efficiency. This is exactly why the Si9169 is designed with pulse skipping mode. If the PWM/$\overline{\text{PSM}}$ pin is connected to logic low level, converter operates in pulse skipping modulation ($\overline{\text{PSM}}$) mode. During the pulse skipping mode, quiescent current of the controller is decreased to approximately 200 µA, instead of 500 µA during the PWM mode. This is accomplished by turning off most of internal control circuitry and utilizing a simple constant on-time control with feedback comparator. The controller is designed to have a constant on-time and a minimum off-time acting as the feedback comparator blanking time. If the output voltage drops below the desired level, the main switch is first turned on and then off. If the applied on-time is insufficient to provide the desired voltage, the controller will force another on and off sequence, until the desired voltage is accomplished. If the applied on-time forces the output to exceed the desired level, as typically found in the light load condition, the converter stays off. The excess energy is delivered to the output slowly, forcing the converter to skip pulses as needed to maintain regulation. The on-time and off-time are set internally based on inductor used (1.5 µH typical), mode pin selection and maximum load current. Wide duty cycle range can be achieved in both buck and boost configurations. In pulse skipping mode, synchronous rectifier drive is also disabled to further decrease the gate charge loss, which in turn improves overall converter efficiency.

Reference

The reference voltage of the Si9169 is set at 1.3 V. The reference voltage is internally connected to the non-inverting inputs of the error amplifier. The reference is decoupled with 0.1 µF capacitor.

DETAIL OPERATIONAL DESCRIPTION (CONT'D)

Error Amplifier

The error amplifier gain-bandwidth product and slew rate is critical parameters which determines the transient response of converter. The transient response is function of both small and large signal response. The small signal is the converter closed loop bandwidth and phase margin while the large signal is determined by the error amplifier dv/dt and the inductor di/dt slew rate. Besides the inductance value, error amplifier determines the converter response time. In order to minimize the response time, the Si9169 is designed with 2 MHz error amplifier gain-bandwidth product to generate the widest converter bandwidth and 3.5 V/µs slew rate for ultra-fast large signal response.

Oscillator

The oscillator is designed to operate up to 2 MHz minimal. The 2 MHz operating frequency allows the converter to minimize the inductor and capacitor size, improving the power density of the converter. Even with 2 MHz switching frequency, quiescent current is only 500 µA with unique power saving circuit design. The switching frequency is easily programmed by attaching a resistor to R_{OSC} pin. See oscillator frequency versus R_{OSC} curve to select the proper values for desired operating frequency. The tolerance on the operating frequency is ± 20 % with 1 % tolerance resistor.

Synchronization

The synchronization to external clock is easily accomplished by connecting the external clock into the SYNC pin. A logic high to low transition synchronizes the clock. The external clock frequency must be within 1.2 to 1.5 times the internal clock frequency.

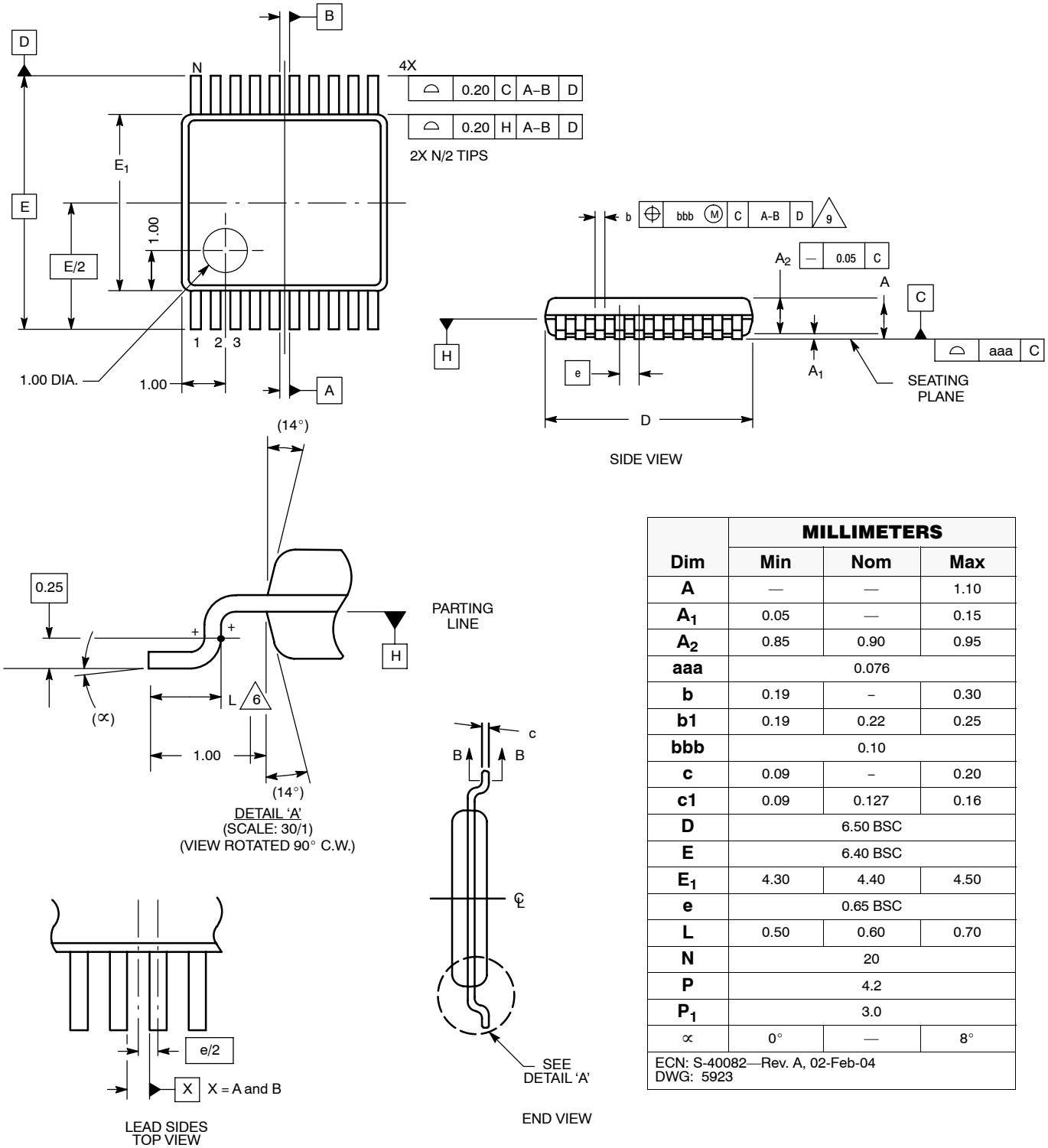
Break-Before-Make Timing

A proper BBM time is essential in order to prevent shoot-through current and maintain high efficiency. The break-before-make time is set internally at 20 ns at V_S = 3.6 V. The high and low-side MOSFET drain voltages are monitored and when the drain voltage reaches the 1.75 V below or above its initial starting voltage, 20 ns BBM time is set before the other switch turns on. The maximum controllable duty cycle is limited by the BBM time. Since the BBM time is fixed, maximum controllable duty cycle will vary depending on the switching frequency.

Output MOSFET Stage

The high- and low-side switches are integrated to provide optimum performance and to minimize the overall converter size. Both, high and low-side switches are designed to handle up to 1 A of continuous current. The MOSFET switches were designed to minimize the gate charge loss as well as the conduction loss. For the high frequency operation, switching losses can exceed conduction loss, if the switches are designed incorrectly. Under full load, efficiency of 90 % is accomplished with 3.6 V battery voltage in both buck and boost modes (+ 2.7 V output voltage for buck mode and + 5 V output voltage for boost mode).

TSSOP: 20-LEAD (POWER IC ONLY)



Dim	MILLIMETERS		
	Min	Nom	Max
A	—	—	1.10
A_1	0.05	—	0.15
A_2	0.85	0.90	0.95
aaa		0.076	
b	0.19	–	0.30
b1	0.19	0.22	0.25
bbb		0.10	
c	0.09	–	0.20
c1	0.09	0.127	0.16
D		6.50 BSC	
E		6.40 BSC	
E_1	4.30	4.40	4.50
e		0.65 BSC	
L	0.50	0.60	0.70
N		20	
P		4.2	
P_1		3.0	
∝	0°	—	8°

ECN: S-40082—Rev. A, 02-Feb-04
DWG: 5923

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