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ON Semiconductor®

June 2017

FAN54110 USB-Compatible Single-Cell Li-Ion Linear Charger with DBP

Features

Fully Integrated, High-Efficiency Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs

Charge Voltage Accuracy: $\pm 0.5\%$ at 25°C
 $\pm 1\%$ from -30 to 85°C

+0/-10% Charge Current Regulation Accuracy

28 V Absolute Maximum Input Voltage

1 A Maximum Charge Current

Support for Dead Battery Provision (DBP) of USB Battery Charging Specification 1.2

Programmable through I²C Interface with Fast Mode (400 kHz) Compatibility

- Input Current
- Fast-Charge / Termination Current
- Charger Voltage

Safety Timer with Reset Control

Weak Input Sources Accommodated by Reducing Charging Current to Maintain Minimum V_{BUS} Voltage

Low Reverse Leakage to Prevent Battery Drain to V_{BUS}

Applications

Smart Phones

Tablets

Portable Media Players

Li Ion Powered Devices

Description

The FAN54110 is a USB-compatible single-cell, linear Li-Ion charger with support for Dead Battery Provision (DBP).

The device employs Over-Voltage Protection (OVP) circuitry to protect the device, load, and battery. The maximum charge current is rated at 1 A and can be programmed from 100 mA to 1 A through the I²C interface, optimizing charging for various battery sizes.

Dynamic Input Voltage Control ensures weak power sources can be used to power the FAN54110 without collapsing to an unusable input voltage for charging.

Open-drain status pins, STAT and POK_B, provide a status of charging and input power. The STAT pin also notifies the system processor when an I²C interrupt occurs so the processor can take action based on the interrupt.

The FAN54110 conforms to the constraints of the Dead Battery Provision within the BC1.2 specification, including a 30-minute timer that cannot exceed 45 minutes.

The FAN54110 is designed to be stable with space-saving ceramic capacitors. The FAN54110 is available in a 15-bump, 0.4 mm pitch, WLCSP package.

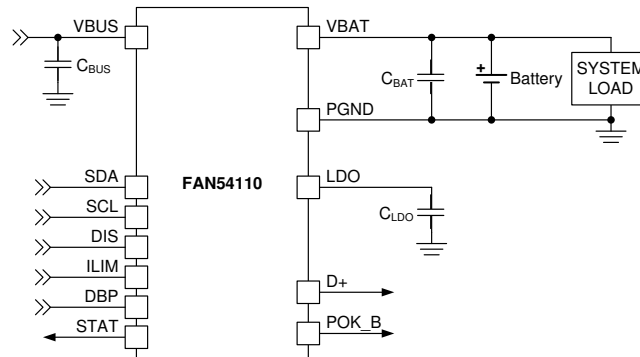


Figure 1. Typical Application

Ordering Information

| Part Number | PN Reg00h[4:3] | Temperature Range | Package | Packing Method |
|-------------|----------------|-------------------|---|----------------|
| FAN54110UCX | 00 | -40°C to 85°C | 15-Bump, Wafer-Level Chip-Scale (WLCSP), 0.4 mm Pitch | Tape and Reel |

Recommended External Components

| Component | Description | Vendor | Parameter | Min. | Typ.(1) | Unit |
|----------------------|------------------------------------|---|-----------|------|---------|---------|
| C _{BUS} | 1.0 μ F, 10%, 25 V, X5R, 0603 | Murata GRM188R61E105K TDK C1608X5R1E105M | C | 0.5 | 1.0 | μ F |
| C _{BAT} (2) | 4.7 μ F, 10%, 6.3 V, X5R, 0603 | Murata GRM188R60J475K TDK C1608X5R0J475K | C | 2.0 | 4.7 | μ F |
| C _{LDO} | 1.0 μ F, 10%, 6.3 V, X5R, 0402 | Murata GRM155R60J105M | C | 0.4 | 1.0 | μ F |

Notes:

- Does not reflect effects of bias, tolerance, and temperature.
- C_{BAT} is placed as close to the charger IC as possible. A minimum requirement of 30 μ F distributed system capacitance (C_{sys}) is parallel with C_{BAT}, but can be located further from the IC.

Block Diagram

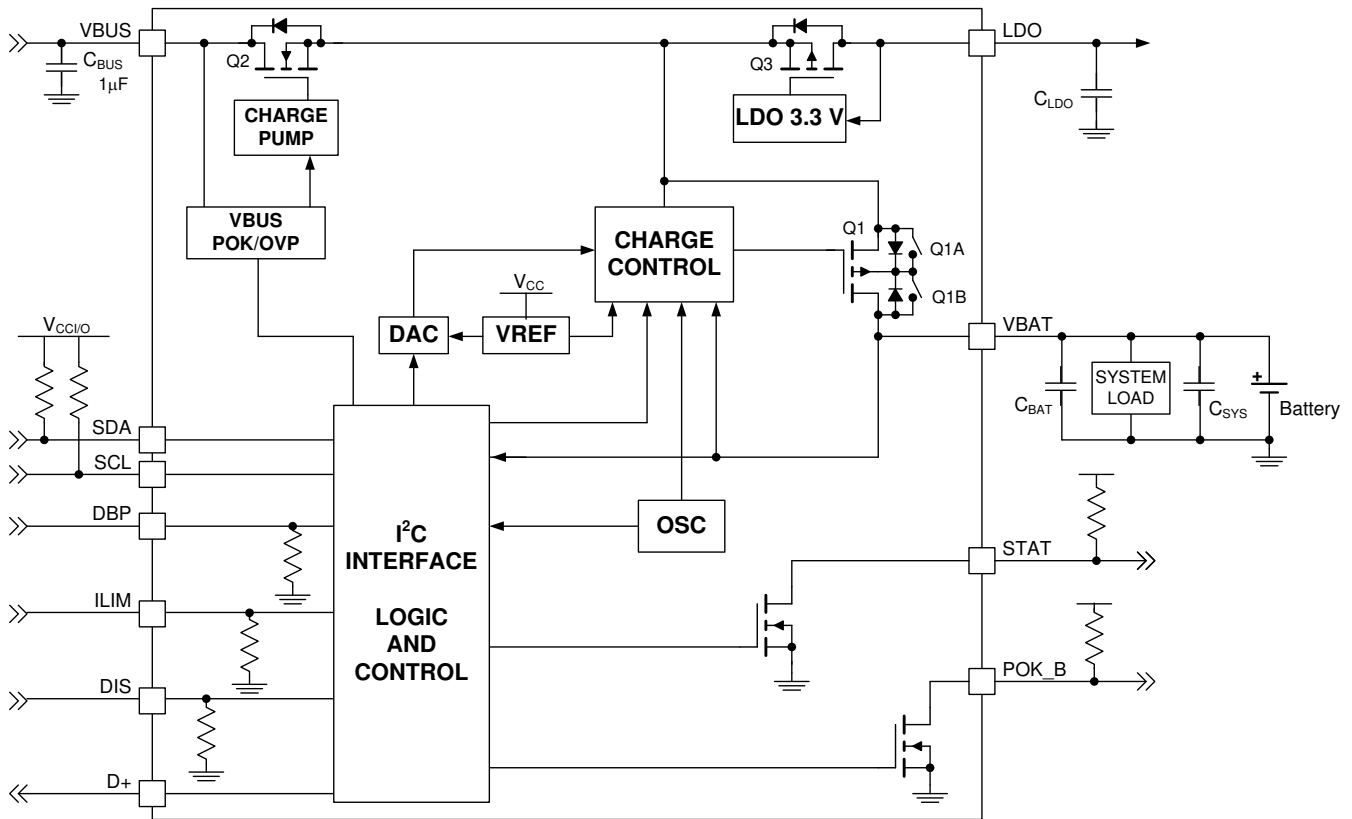
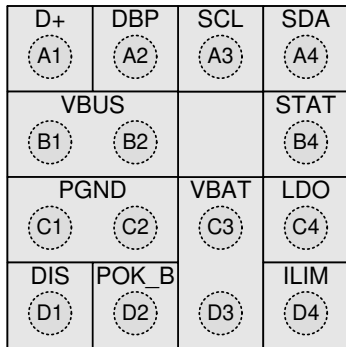
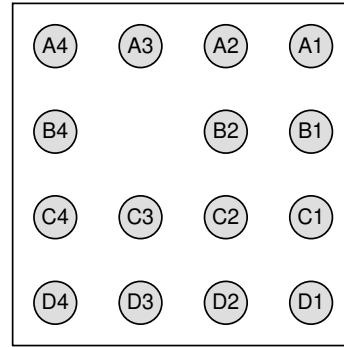


Figure 2. IC and System Block Diagram



Top View



Bottom View

Pin Definitions

| Pin # | Name | Description |
|--------|-------|---|
| A1 | D+ | Connect to the USB connector D+ pin Charger IC sources 0.6 V in CHARGE state when DBP is LOW. Otherwise, this pin is 3-state. |
| A2 | DBP | Dead Battery Provision Disable Pull HIGH to disable charger D+ output. Internal pull-down resistor. |
| A3 | SCL | I²C Interface Serial Clock |
| A4 | SDA | I²C Interface Serial Data |
| B1, B2 | VBUS | Charger Input Voltage Bypass with a 1 μ F capacitor directly to PGND. |
| B4 | STAT | Status / Interrupt Open-drain output indicating charge status. The IC pulls this pin LOW when charge is in process. High impedance when charging is done or charger is disabled. Also used as system interrupt. 128 μ s pulse and then high impedance indicates to the system a fault has occurred. |
| C1, C2 | PGND | Power Ground Power return for gate drive and power transistors. |
| C4 | LDO | 3.3 V LDO 3.3 V regulator output. |
| D1 | DIS | Active-High Disable When pulled HIGH, the charger is disabled. Internal pull-down resistor. |
| D2 | POK_B | VBUS Power-OK Monitor Open-drain output that is pulled LOW when V _{BUS} is greater than the V _{BUS} validation threshold and lower than V _{BUS} OVP. High impedance when outside this range. |
| C3, D3 | VBAT | Battery Voltage Connect to the positive (+) terminal of the battery pack. Bypass locally with a 4.7 μ F capacitor to PGND. |
| D4 | ILIM | Input Current Limit This pin sets the input current limit for t _{30MIN} charging. Internal pull-down resistor. |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Min. | Max. | Unit |
|------------------|--|---|------|------|------|
| V _{BUS} | Voltage on VBUS | Continuous | -1.2 | 28.0 | V |
| V _{BAT} | Voltage on VBAT | | -0.3 | 6.5 | V |
| V _O | Voltage on Other Pins | | -0.3 | (3) | V |
| ESD | Electrostatic Discharge Protection Level | Human Body Model per ANSI/ESDA/JEDEC JS-001-2012 (All Pins) | 2000 | | V |
| | | Charged Device Model per JESD22-C101 (All Pins) | 1500 | | |
| | | IEC 61000-4-2 System (VBUS and D+ Pins) | 8000 | | |
| LU | Latch Up | JESD78 – Class 1, 25°C | ±100 | | mA |
| T _J | Junction Temperature | | -40 | +150 | °C |
| T _{STG} | Storage Temperature | | -65 | +150 | °C |
| T _L | Lead Soldering Temperature, 10 Seconds | | | +260 | °C |

Note:

3. Lesser of 6.5 V or V_{BAT} + 0.3 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|-----------------|----------------------|------|------|------|
| V _{IN} | Supply Voltage | 4 | 6 | V |
| T _A | Ambient Temperature | -30 | +85 | °C |
| T _J | Junction Temperature | -30 | +125 | °C |

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature T_{J(max)} at a given ambient temperature T_A. *For measured data, see the Evaluation Board Measured θ_{JA} table.*

| Symbol | Parameter | Typical | Unit |
|---------------|--|---------|------|
| θ_{JA} | Junction-to-Ambient Thermal Resistance | 60 | °C/W |
| θ_{JB} | Junction-to-PCB Thermal Resistance | 20 | °C/W |

Electrical Specifications

Unless otherwise specified: circuit of Figure 2, recommended operating temperature range for T_J and T_A , $V_{BUS}=5.0\text{ V}$, $DIS=0$ (Charger Mode operation), SCL , $SDA=0$ or 1.8 V ; typical values are for $T_J=25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|--|---|--|------|-------|------------------|
| Power Supplies | | | | | | |
| $V_{IN(MIN)1}$ | V_{BUS} Input Voltage Rising | To Initiate and Pass V_{BUS} Validation | 4.18 | 4.40 | 4.65 | V |
| $V_{IN(MIN)2}$ | Minimum V_{BUS} during Charge | V_{BUS} Regulation Loop is Off | 2.95 | 3.10 | 3.35 | V |
| t_{VBUS_VALID} | V_{BUS} Validation Time | | | 32 | | ms |
| V_{BUS_REF} | V_{BUS} Regulation Loop Threshold | Relative to V_{BUS_REF} Setting | -5 | | +5 | % |
| I_{VBUS} | V_{BUS} Current | $DIS=1$ | | 890 | 1,000 | μA |
| I_{DIS} | V_{BUS} Discharge Current | V_{BUS} Removal or Validation | 40 | 63 | 90 | mA |
| I_{BAT} | Battery Discharge Current during SLEEP State | $V_{BAT}=4.2\text{ V}$, $V_{BUS}=\text{Open}$, $SDA=SCL=1.8\text{ V}$, No I^2C Traffic, $-30^\circ\text{C} < T_J < 85^\circ\text{C}$ | | 5 | 10 | μA |
| | | $V_{BAT}=4.2\text{ V}$, $V_{BUS}=\text{Open}$, $SDA=SCL=0\text{ V}$, $-30^\circ\text{C} < T_J < 85^\circ\text{C}$ | | 3 | 8 | |
| I_{BUS_LKG} | V_{BAT} to V_{BUS} Leakage Current | $V_{BAT}=4.2\text{ V}$, $V_{BUS}=0\text{ V}$, $-30^\circ\text{C} < T_J < 85^\circ\text{C}$ | | <1 | 2 | μA |
| Charger Voltage Regulation | | | | | | |
| V_{OREG} | Charge Voltage Range | | 3.38 | | 4.44 | V |
| | Charge Voltage Accuracy | $V_{OREG}=4.2\text{ V}$ | $T_J=25^\circ\text{C}$ | -0.5 | +0.5 | % |
| | | | $-30^\circ\text{C} < T_J < 85^\circ\text{C}$ | -1 | +1 | |
| | | $3.38\text{ V} < V_{OREG} < 4.44\text{ V}$ | $T_J=25^\circ\text{C}$ | -1 | +1 | |
| | | $-30^\circ\text{C} < T_J < 85^\circ\text{C}$ | -1.5 | -1.5 | | |
| | V_{BAT} Overshoot Pulsed Load ⁽⁴⁾ | See V_{BAT} Overshoot Test | | 2 | 10 | mV |
| Fast Charging Current Regulation | | | | | | |
| I_{OCHRG} | Output Charge Current Range | | 100 | | 1,000 | mA |
| | Charge Current Accuracy (measured at V_{BUS} , includes $I_{CHRG} + I_{REG}$) | $I_{OCHRG} \geq 350\text{ mA}$ | -10 | -5 | 0 | % |
| | | $I_{OCHRG} < 350\text{ mA}$ | -15 | -7 | 0 | |
| Logic Levels: DIS, SDA, SCL, ILIM, DBP | | | | | | |
| V_{IH} | High-Level Input Voltage | | 1.05 | | | V |
| V_{IL} | Low-Level Input Voltage | | | | 0.4 | V |
| I_{IN} | Input Bias Current | Input Tied to GND or Greater of V_{BAT} or Valid V_{BUS} | | 0.01 | 1.00 | μA |
| R_{PD} | ILIM, DBP, DIS Pull-Down Resistance | | 0.6 | 0.9 | 1.4 | $\text{M}\Omega$ |

V_{BAT} Overshoot Test

In the figure below, $I_{OCHARGE}=1\text{ A}$ (1111), $V_{OREG}=4.2\text{ V}$. I_{LOAD} $t_r=t_f=1\ \mu\text{s}$. Charge current prior to load transient = $\frac{20\text{mV}}{200\text{m}\Omega} = 100\text{mA}$

Overshoot is measured as the peak voltage above V_{BAT} level prior to the load transient application. C_{SYS} represents the distributed system capacitance across the V_{BAT} terminals and is assumed to be a minimum of $30\ \mu\text{F}$.

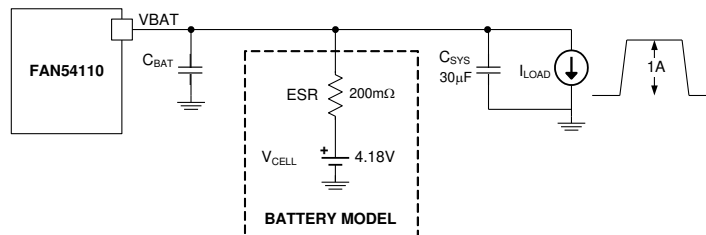


Figure 3. V_{BAT} Overshoot Test Condition

Electrical Specifications

Unless otherwise specified: circuit of Figure 2, recommended operating temperature range for T_J and T_A , $V_{BUS}=5.0\text{ V}$, $DIS=0$ (Charger Mode operation), SCL , $SDA=0$ or 1.8 V ; typical values are for $T_J=25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--|---|---|------|----------|------|------------------|
| Charge Termination Detection | | | | | | |
| I_{TERM} | Termination Current Range | $V_{BAT} > V_{OREG} - V_{RCH}$, $V_{BUS} > V_{BUS_REF}$ | 20 | | 170 | mA |
| | Termination Current Accuracy | $I_{TERM} > 80\text{ mA}$ | -10 | | +10 | % |
| | | $I_{TERM} \leq 80\text{ mA}$ | -20 | | +20 | |
| Battery Recharge Threshold | | | | | | |
| V_{RCH} | Recharge Threshold | V_{BAT} Falling by V_{RCH} below V_{OREG} Threshold | | 100 | | mV |
| 3.3 V Linear Regulator | | | | | | |
| V_{REG} | 3.3 V Regulator Output | I_{REG} from 0 to 40 mA | 3.10 | 3.30 | 3.50 | V |
| DBP Output | | | | | | |
| V_{DBP_SRC} | Voltage on D+ pin | $DBP=0$, I_{LOAD} on D+ from 0 to 250 μA | 0.51 | 0.60 | 0.69 | V |
| I_{DBP_OFF} | Leakage Current | $DBP=1$, V_{D+} from 0 to 3.6 V | -1 | | +1 | μA |
| STAT / POK_B Output | | | | | | |
| V_{OL} | STAT / POK_B Output Low | $I=10\text{ mA}$ | | | 0.4 | V |
| I_{OH} | STAT / POK_B Leakage Current | $V=5\text{ V}$ | | | 1 | μA |
| Battery Detection | | | | | | |
| I_{DETECT} | Battery Detection Current before Charge Done (Sink Current) | Begins after Termination Detected | | -1 | | mA |
| t_{DETECT} | Battery Detection Time | | | 262 | | ms |
| Power Switches (see Error! Reference source not found.) | | | | | | |
| $Q1\ R_{DS(ON)}$ | Q1 On Resistance | | | 175 | 260 | $\text{m}\Omega$ |
| $Q2\ R_{DS(ON)}$ | Q2 On Resistance | | | 110 | 170 | $\text{m}\Omega$ |
| Protection and Timers | | | | | | |
| V_{BUSOVP} | V_{BUS} OVP Accuracy | V_{BUS} Rising | -7 | | +7 | % |
| | Hysteresis | V_{BUS} Falling | | 100 | | mV |
| V_{SHORT} | Battery Short-Circuit Threshold | V_{BAT} Rising | 2.10 | 2.27 | 2.40 | V |
| | Hysteresis | V_{BAT} Falling | | 120 | | mV |
| I_{SHORT} | Linear Charging Current | $V_{BAT} < V_{SHORT}$ | 85 | 93 | 100 | mA |
| $I_{LIM(PTM)}$ | Production Test Mode Current Limit | | 2.2 | | | A |
| $T_{SHUTDWN}$ | Thermal Shutdown Threshold ⁽⁴⁾ | T_J Rising | 130 | 145 | 160 | $^\circ\text{C}$ |
| | Re-Enable Threshold ⁽⁴⁾ | T_J Falling | | T_{CF} | | |
| T_{CF} | Thermal Regulation Accuracy ⁽⁴⁾ | Relative to T_{CF} Setting | -10 | | +10 | $^\circ\text{C}$ |
| t_{32S} | 32-Second Timer | | 20.5 | 24.3 | 28.0 | s |
| t_{30MIN} | 30-Minute Timer | | 30 | 38 | 45 | min |
| t_{OSC} | 125 kHz Oscillator Tolerance | Timing in all Sequencing Diagrams | -15 | | 15 | % |

Note:

4. Guaranteed by design; not tested in production.

I²C Timing Specifications

Guaranteed by design.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---------------------------------------|--|--|----------------------|------|------|------|
| f _{SCL} | SCL Clock Frequency | Standard Mode | | | 100 | kHz |
| | | Fast Mode | | | 400 | |
| | | High-Speed Mode, C _B ≤ 100 pF | | | 3400 | |
| | | High-Speed Mode, C _B ≤ 400 pF | | | 1700 | |
| t _{BUF} | Bus-Free Time between STOP and START Conditions | Standard Mode | | 4.7 | | μs |
| | | Fast Mode | | 1.3 | | |
| t _{HD,STA} | START or Repeated START Hold Time | Standard Mode | | 4 | | μs |
| | | Fast Mode | | 600 | | ns |
| | | High-Speed Mode | | 160 | | ns |
| t _{LOW} | SCL LOW Period | Standard Mode | | 4.7 | | μs |
| | | Fast Mode | | 1.3 | | |
| | | High-Speed Mode, C _B ≤ 100 pF | | 160 | | ns |
| | | High-Speed Mode, C _B ≤ 400 pF | | 320 | | |
| t _{HIGH} | SCL HIGH Period | Standard Mode | | 4 | | μs |
| | | Fast Mode | | 600 | | |
| | | High-Speed Mode, C _B ≤ 100 pF | | 60 | | ns |
| | | High-Speed Mode, C _B ≤ 400 pF | | 120 | | |
| t _{SU,STA} | Repeated START Setup Time | Standard Mode | | 4.7 | | μs |
| | | Fast Mode | | 600 | | ns |
| | | High-Speed Mode | | 160 | | |
| t _{SU,DAT} | Data Setup Time | Standard Mode | | 250 | | ns |
| | | Fast Mode | | 100 | | |
| | | High-Speed Mode | | 10 | | |
| t _{HD,DAT} | Data Hold Time | Standard Mode | 0 | | 3.45 | μs |
| | | Fast Mode | 0 | | 900 | ns |
| | | High-Speed Mode, C _B ≤ 100 pF | 0 | | 70 | |
| | | High-Speed Mode, C _B ≤ 400 pF | 0 | | 150 | |
| t _{RCL} | SCL Rise Time | Standard Mode | 20+0.1C _B | | 1000 | ns |
| | | Fast Mode | 20+0.1C _B | | 300 | |
| | | High-Speed Mode, C _B ≤ 100 pF | | 10 | 80 | |
| | | High-Speed Mode, C _B ≤ 400 pF | | 20 | 160 | |
| t _{FCL} | SCL Fall Time | Standard Mode | 20+0.1C _B | | 300 | ns |
| | | Fast Mode | 20+0.1C _B | | 300 | |
| | | High-Speed Mode, C _B ≤ 100 pF | | 10 | 40 | |
| | | High-Speed Mode, C _B ≤ 400 pF | | 20 | 80 | |
| t _{RDA} t _{RCL1} | SDA Rise Time Rise Time of SCL after a Repeated START Condition and after ACK Bit | Standard Mode | 20+0.1C _B | | 1000 | ns |
| | | Fast Mode | 20+0.1C _B | | 300 | |
| | | High-Speed Mode, C _B ≤ 100 pF | | 10 | 80 | |
| | | High-Speed Mode, C _B ≤ 400 pF | | 20 | 160 | |

Continued on the following page...

I²C Timing Specifications

Guaranteed by design.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---------------------|------------------------------|--|----------------------|------|------|------|
| t _{FDA} | SDA Fall Time | Standard Mode | 20+0.1C _B | | 300 | ns |
| | | Fast Mode | 20+0.1C _B | | 300 | |
| | | High-Speed Mode, C _B ≤ 100 pF | | 10 | 80 | |
| | | High-Speed Mode, C _B ≤ 400 pF | | 20 | 160 | |
| t _{SU:STO} | Stop Condition Setup Time | Standard Mode | | 4 | | μs |
| | | Fast Mode | | 600 | | ns |
| | | High-Speed Mode | | 160 | | |
| C _B | Capacitive Load for SDA, SCL | | | | 400 | pF |

Timing Diagram

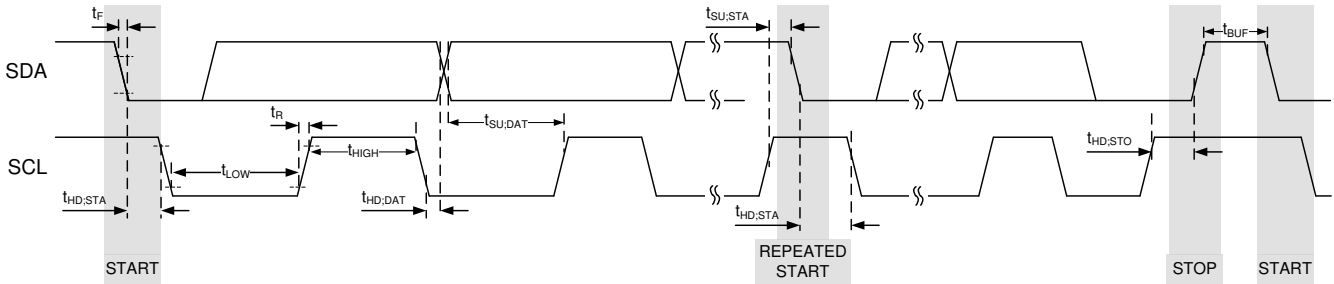


Figure 4. I²C Interface Timing for Fast and Slow Modes

Typical Characteristics

Unless otherwise specified; circuit of Figure 2, $V_{OREG}=4.2\text{ V}$, $V_{BUS}=5.0\text{ V}$, and $T_A=25^\circ\text{C}$.

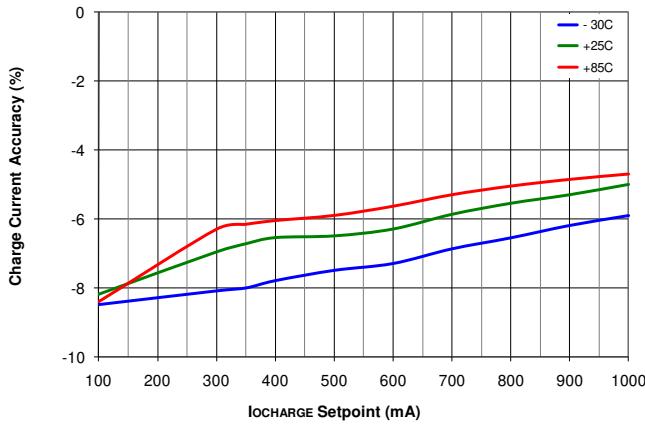


Figure 5. I_{OCHRG} Accuracy Over-Temperature, 3.7 V_{BAT}

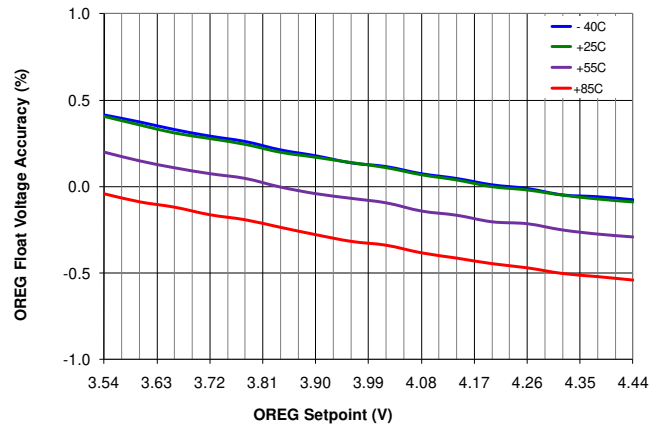


Figure 6. OREG Accuracy Over-Temperature, $I_{BAT}=100\text{ mA}$

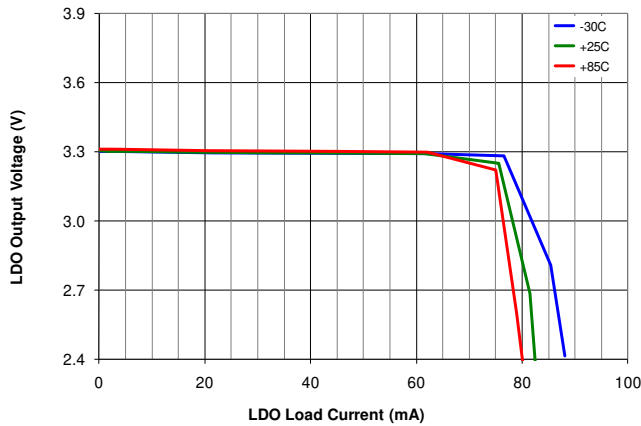


Figure 7. LDO Load Regulation, $V_{OREG}=V_{BAT}=4.2\text{ V}$

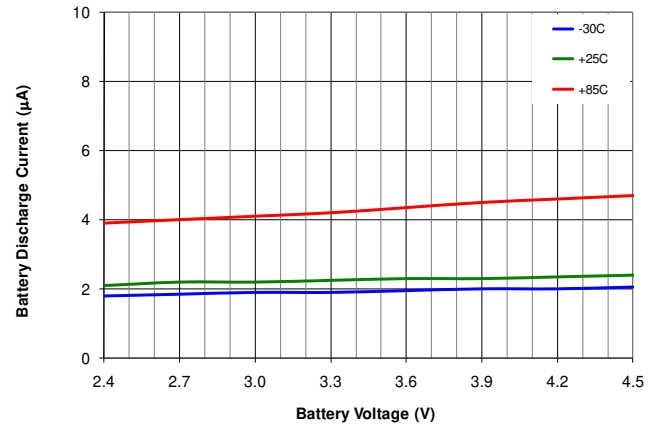


Figure 8. HZ / Sleep Mode Battery Discharge Current, V_{BUS} Open, $DIS=SDA=SCL=0\text{ V}$

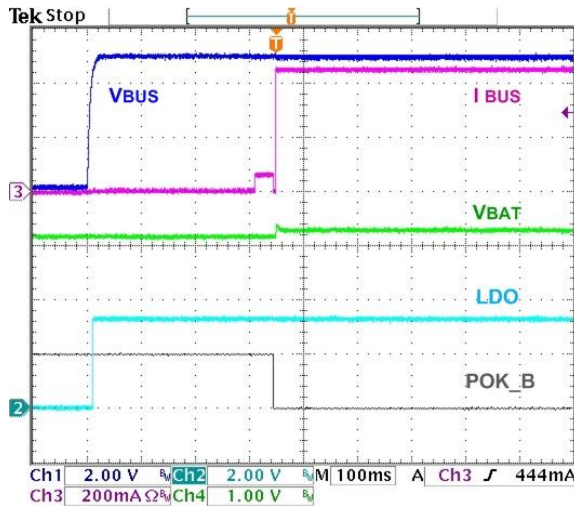


Figure 9. Charger Startup at V_{BUS} Plug-In, 500 mA I_{OCHRG} , 3.2 V_{BAT} , $1\text{ k}\Omega$ LDO Load, $ILIM=IBP=1.8\text{ V}$

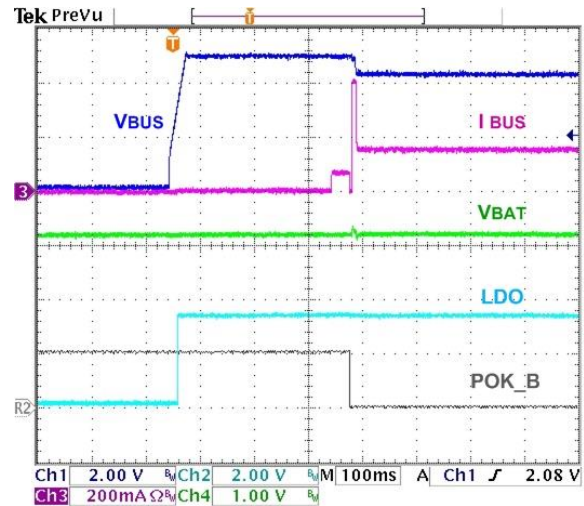


Figure 10. Charger Startup at V_{BUS} Plug-In Using 150 mA Current Limited Source, 3.2 V_{BAT} , 500 mA I_{OCHRG} , $1\text{ k}\Omega$ LDO Load, $ILIM=IBP=1.8\text{ V}$

Typical Characteristics

Unless otherwise specified; circuit of Figure 2, $V_{OREG}=4.2\text{ V}$, $V_{BUS}=5.0\text{ V}$, and $T_A=25^\circ\text{C}$.

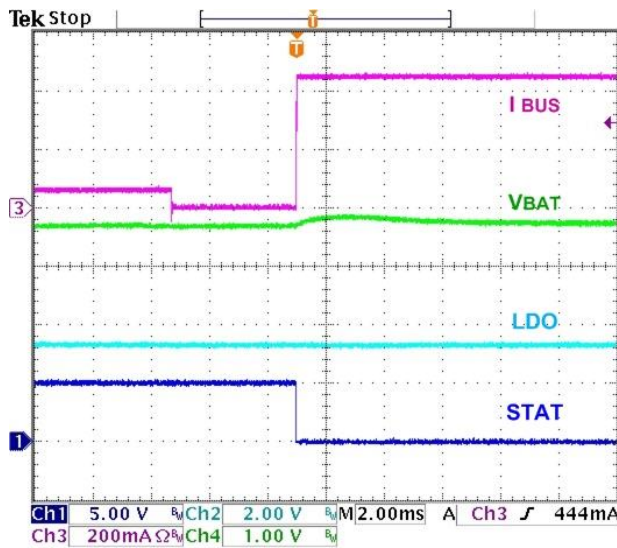


Figure 11. Charger Startup Using HZ Bit Reset, 3.7 V_{BAT} , 500 mA I_{OCHRG} , 1 k Ω LDO Load, $I_{LIM}=DBP=1.8\text{ V}$

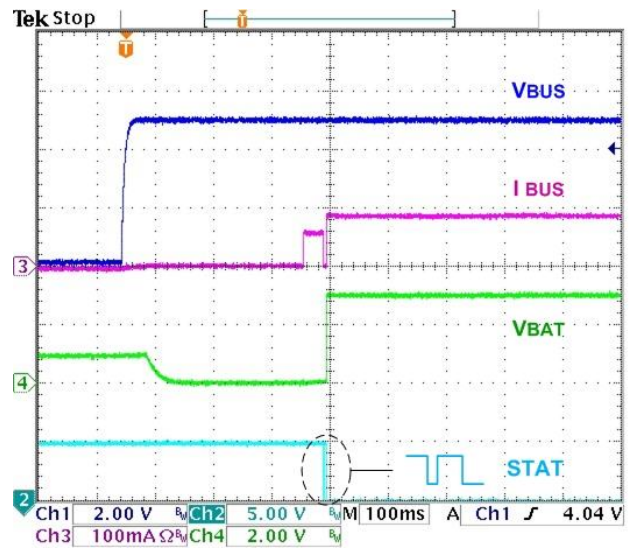


Figure 12. Charger Startup at V_{BUS} Plug-In with Dead Battery (Protection Switch Open), 1 k Ω LDO Load, $I_{LIM}=DBP=0\text{ V}$

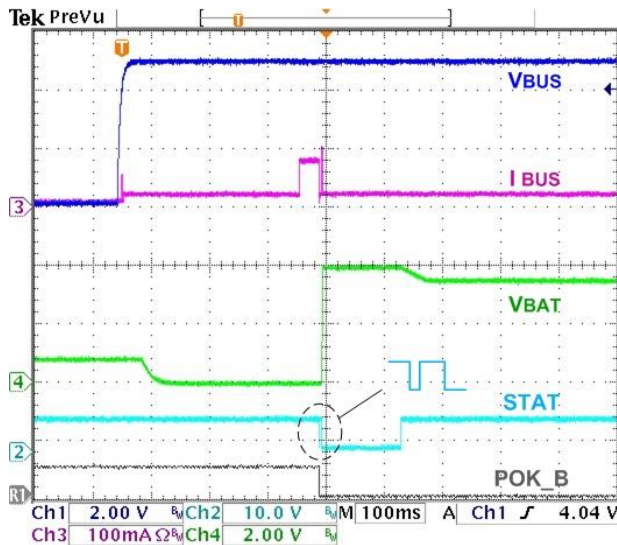


Figure 13. Charger Startup at V_{BUS} Plug-In with No Battery, 300 Ω LDO Load, $I_{LIM}=DBP=0\text{ V}$

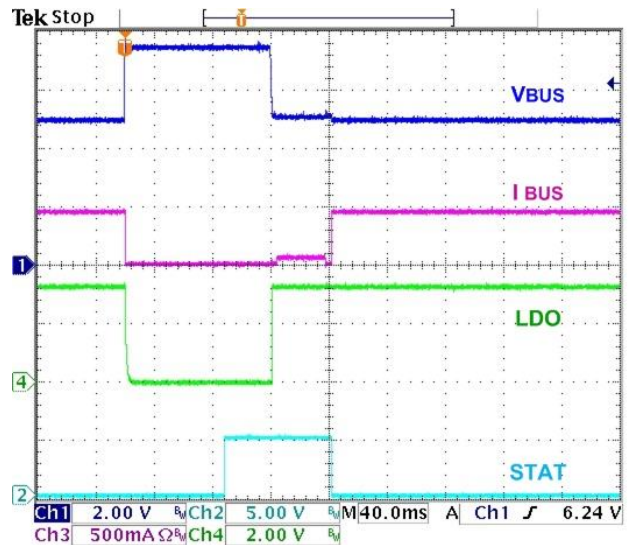


Figure 14. V_{BUS} OVP Response while Charging, 3.7 V_{BAT} , 500 mA I_{OCHRG} , 1 k Ω LDO Load, $I_{LIM}=DBP=1.8\text{ V}$

Typical Characteristics

Unless otherwise specified; circuit of Figure 2, $V_{OREG}=4.2\text{ V}$, $V_{BUS}=5.0\text{ V}$, and $T_A=25^\circ\text{C}$.

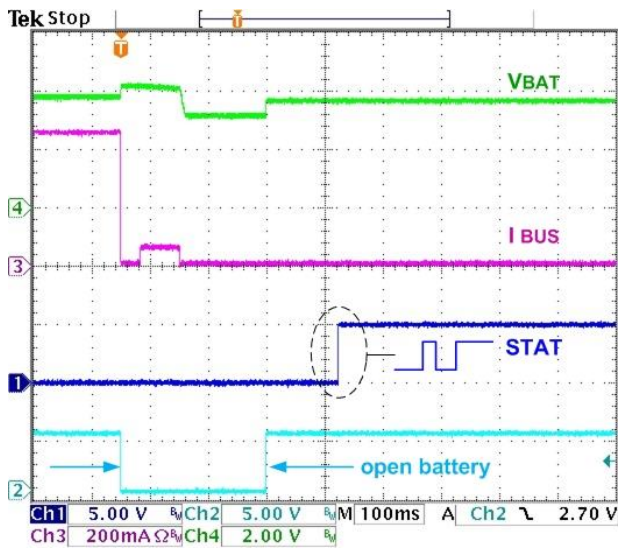


Figure 15. Battery Removal/Insertion while Charging, 3.7 V_{BAT}, 500 mA I_{CHRG}, I_{LIM}=DBP=1.8 V, I_{TERM_DIS}=0

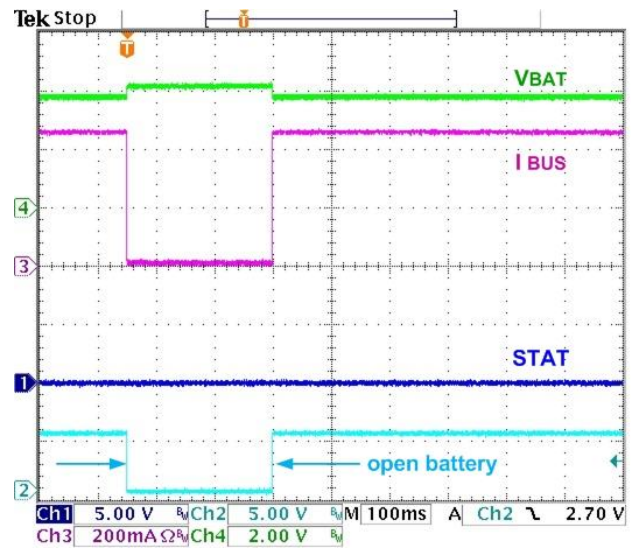


Figure 16. Battery Removal/Insertion while Charging, 3.7 V_{BAT}, 500 mA I_{CHRG}, I_{LIM}=DBP=1.8 V, I_{TERM_DIS}=1

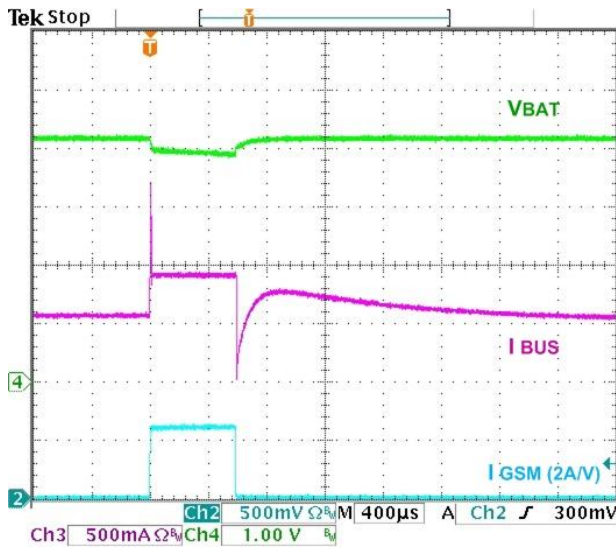


Figure 17. 1.2 A Load Pulse, $t_r=t_f=5\ \mu\text{s}$, 4.19 V_{BAT}, 1.0 A I_{CHRG}

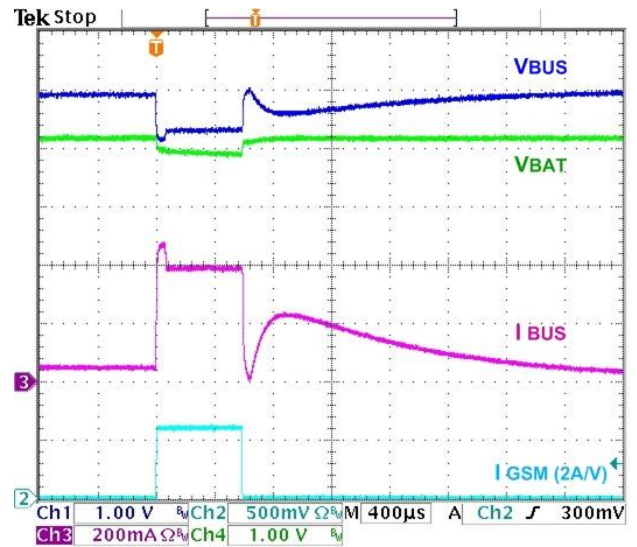


Figure 18. 1.2 A Load Pulse, $t_r=t_f=5\ \mu\text{s}$, 500 mA Current Limited Source, 4.2 V_{BAT}, 1.0 A I_{CHRG}, 4.32 V_{BUS_REF}

Basic Operation

The FAN54110 is a USB-compatible single-cell Li-Ion charger with support for Dead Battery Provision (DBP) and a maximum charge current rated at 1 A.

The FAN54110 conforms to all the requirements for the DBP within the BC1. 2 specifications, including a 30-minute timer that cannot exceed 45 minutes.

The FAN54110 is designed to be stable with space-saving ceramic capacitors and is available in a 15-bump, 0.4 mm pitch, WLCSP.

Charger Circuit Details

VBUS Insertion

When the IC detects that V_{BUS} has risen above $V_{IN(MIN)1}$, adapter validation and battery voltage detection will occur before charging begins. To pass validation, V_{BUS} must remain above $V_{IN(MIN)1}$ and below $V_{BUSOVVP}$ for t_{VBUS_VALID} before the IC initiates charging. Refer to Figure 20 and Figure 21 for details.

If V_{BUS} is validated, the POK_B pin pulls LOW and an interrupt is issued to indicate to the system that VBUS is connected. This point is considered to be VBUS_POR.

If VBUS fails validation, the POK_B pin remains HIGH and an interrupt is issued. Re-validation is attempted every two seconds.

Setting the HZ_MODE bit or DIS pin prevents validation from occurring after VBUS rises above $V_{IN(MIN)1}$, but, VBUS validation will be performed prior to entering Charge State from any state where the charger is off.

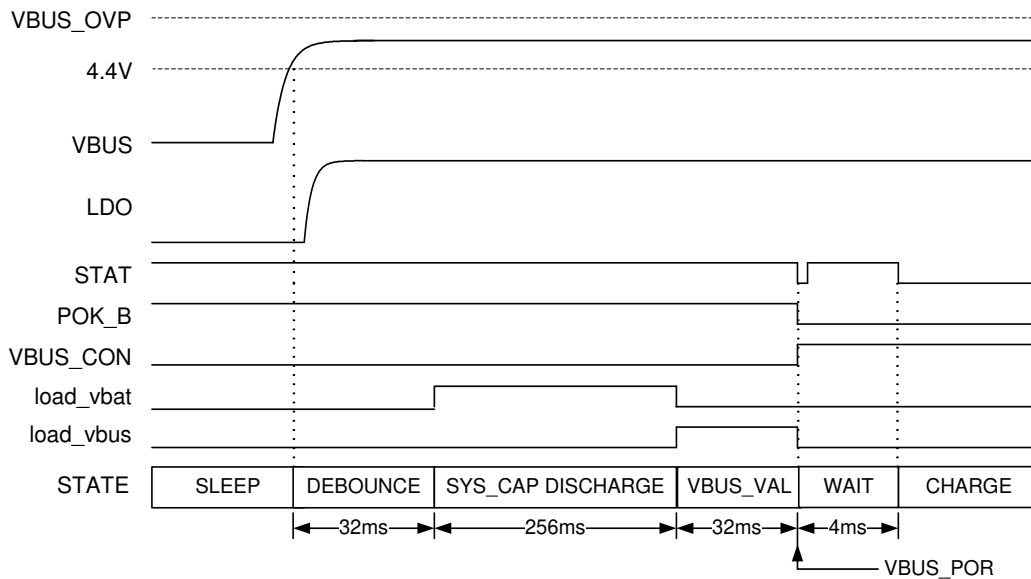


Figure 19. VBUS Plug-In Timing: DIS=0, HZ_MODE=0, DBP=1

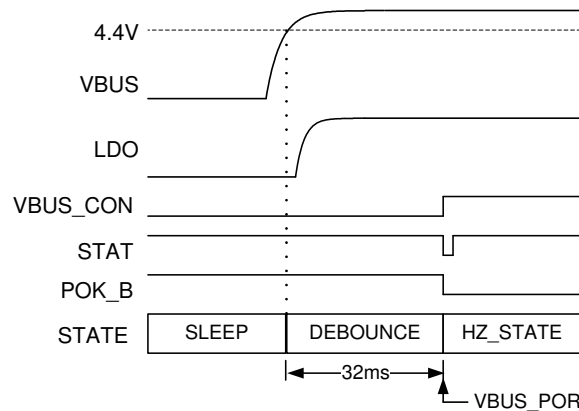


Figure 20. VBUS Plug-In Timing: DIS=1 or (DBP=1 and HZ_MODE=1)

VBUS POR and DBP Charging

If the DBP pin is HIGH at VBUS_POR, the IC operates in accordance with its I²C register settings and starts the t_{32s} timer when charging begins. This is the normal operating mode for the FAN54110.

If the DBP pin is LOW at VBUS_POR or the DBP pin transitions from HIGH to LOW when VBUS is valid, the FAN54110:

- Resets its registers to default values
- Charges with its charge current limit set by the state of the ILIM pin:
 - ILIM= LOW, I_{CHRG}=100 mA
 - ILIM= HIGH, I_{CHRG}=350 mA
- Starts the t_{30MIN} timer
- Sources 0.6 V to the D+ pin

BC1.2 and USB 2.0 allow a portable device (defined as a device with a battery) with a dead battery to take a maximum of 100 mA from the USB VBUS line for a maximum of 45 minutes as long as the portable device forces the D+ line to 0.6 V typical.

Once DBP transitions from LOW to HIGH, D+ is three-stated and charge parameters may be programmed by the host. Charge current remains controlled by the state of the ILIM pin and the t_{30MIN} timer continues running until the first I²C write occurs; at which time, charge current is controlled by the I_{CHRG} (Reg03h[7:4]) bits and the timer changes to t_{32s}.

The ILIM and DBP pins are internally pulled down and there is typically nothing to force them HIGH at this point due to the processor / system not yet being awake. When the t_{30MIN} timer expires, the FAN54110 removes the 0.6 V from D+ and stops charging. The D+ pin is three-stated when DBP is HIGH.

Battery Absent at VBUS Insertion

Before charging begins, if V_{BAT} is below V_{SHORT}, the FAN54110 will determine whether the battery is absent or present.

To accomplish this, the IC temporarily raises V_{OREG} to 4.0 V after V_{BAT} has risen above V_{SHORT}. If V_{BAT} remains below 3.7 V for more than 128 ms, the battery is present. If V_{BAT} is above 3.7 V after 128 ms, the battery is assumed absent.

If battery absence is detected, all registers are reset to their default values, the NOBAT bit is set, and an interrupt is generated. Also, it is assumed the DBP pin is LOW since the system was without a power source prior to plug in. The FAN54110 will provide power to the system with STAT HIGH in DBP Mode until otherwise instructed through I²C commands. This allows the host processor an opportunity to detect charger type and negotiate with the USB host for higher current.

The IC continues to provide current, provided that:

- a timer (t_{30MIN} or t_{32s}) is running
- HZ_MODE (Reg=01h[6])=0 and DIS=LOW.

The current drawn from VBUS is determined by either the state of ILIM pin or the I_{CHRG} programming.

Charging Stages

Figure 21 shows the different charging stages when a battery is present and discharged below 2.25 V.

PRE-CHARGE is when the battery voltage is below V_{SHORT} and a current of I_{SHORT} is used to charge the battery above V_{SHORT}. This stage is typically used to recover a deeply discharge battery with its protection switch open.

CURRENT REGULATION increases charging current considerably above I_{SHORT} to a programmable I_{CHRG} (Reg 03h[7:4]) level.

VOLTAGE REGULATION occurs during charging when V_{BAT} reaches V_{OREG} (Reg4[5:0]). The current charging the battery is reduced, limited by the battery's ESR and its internal cell voltage.

- If I_{TERM_DIS} (Reg03h[0])=0, charging current decreases to I_{TERM} (Reg03h[3:0]), where Charge Termination occurs.
- If I_{TERM_DIS}=1 (default configuration), charging will continue past I_{TERM} until current decreases to 0A, where the part will remain in Charge Mode with the t_{32s} timer running.

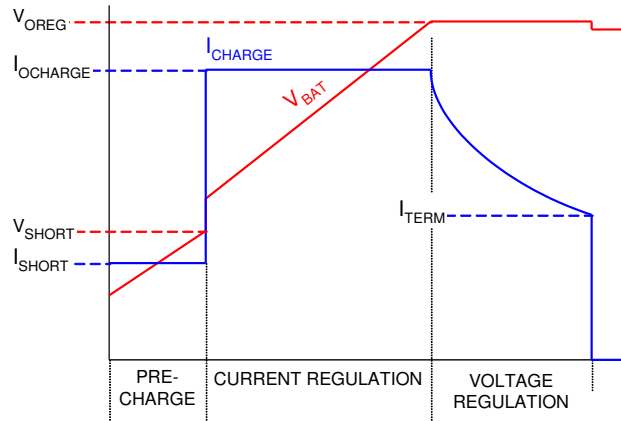


Figure 21. Typical Charge Profile

Charge Termination

During Voltage Regulation, charging continues until the I_{BAT} ≤ I_{TERM}. If I_{TERM_DIS}=0, charging stops and the t_{32s} timer continues counting. The STAT pin remains LOW until the IC determines whether the I_{BAT} < I_{TERM} condition was caused by VBUS removal, Battery Removal, or by the battery being fully charged (Charge Termination).

During Charge Termination, the t_{32s} timer will continue running, but, if it expires will not reset all registers until Recharge. Setting the TMR_RST bit (Reg8[7]) during Charge Termination will reset the t_{32s} timer. Refer to the Timers section for more details.

Recharge from Charge Termination

During Charge Termination, if V_{BAT} falls by V_{RCH} below V_{OREG}, charging starts again.

A recharge condition de-bounce time of 60 ms is used to prevent transient battery load currents (such as GSM current pulses) from triggering auto-recharge unnecessarily.

Battery Removal during Charging

When $ITERM_DIS=0$ and the charge current drops below the I_{TERM} setting, a load current (I_{DETECT}) is placed on V_{BAT} in order to determine if the battery was removed during charging. If the battery is determined to be present, the load is removed, and Charge Done State is entered. If the battery is determined to be absent, the IC enters a fault state, which waits with the charger disabled for two seconds, then re-starts the charger validation process.

- If the battery is determined to be present, the load is removed, and Charge Termination occurs.
- If the battery is determined to be absent, charging is disabled, all registers except $ITERM_DIS$ are reset to default values, the $NOBAT$ interrupt bit is set, and the $STAT$ pin rises. After 2s, the charger will restart validation and if the battery is re-inserted, the IC will return to Charge State.

In response to V_{BAT} collapsing, though, the system electronics have likely lowered the DBP pin which will reset all registers. As a result, the $ITERM_DIS$ bit will be reset to 1, which will set the unloaded V_{BAT} pin to output 3.54V (the default V_{OREG} setting) and place the IC in Charge State with the $NOBAT$ bit remaining set until the next V_{BUS_POR} validation.

VBUS Removal and SLEEP

When V_{BUS} falls below either $V_{IN(MIN)2}$ or V_{BAT} , the IC ceases charging, the POK_B pin sets HIGH, and an interrupt occurs to indicate to the system that V_{BUS} has been removed. The IC then enters the Sleep State.

LDO

The FAN54110 provides a regulated 3.3 V LDO output when a valid V_{BUS} condition exists to power the USB PHY. Regulation occurs within 5 ms of valid V_{BUS} being applied.

LDO load current is derived from V_{BUS} and is subject to the $I_{OCHARGE}$ setting / limit. Available battery charging current is reduced by the LDO load current.

Charger/Battery/System Protections

Timers

There are two timers on the FAN54110; t_{32S} and the t_{30MIN} .

The t_{32S} timer is for normal operation where the DBP pin is HIGH. When charging begins after a V_{BUS_POR} with the DBP pin HIGH, the t_{32S} timer is started. If the t_{32S} timer is allowed to expire, charging ceases and the part will enter the IDLE State where all registers are reset. A write to any register can return the IC to charging. To avoid a t_{32S} timer fault, the host must reset the timer by periodically setting the TMR_RST (Reg08h[7]) bit before it expires.

The t_{30MIN} timer is for unattended charging. If $V_{BAT}<V_{SHORT}$ the device is assumed to be dead and the DBP pin is, therefore, LOW. When charging begins after a V_{BUS_POR} with $V_{BAT}<V_{SHORT}$ and the DBP pin LOW, the t_{30MIN} timer is started. If the t_{30MIN} timer is allowed to expire, charging

ceases and the part will enter the IDLE State where all registers are reset. Only a new V_{BUS_POR} will return the IC to charging.

During unattended charging, if the DBP pin transitions from LOW to HIGH (due to the host waking up and controlling the charger):

- 1- If $V_{BAT}<V_{SHORT}$, the t_{30MIN} timer will continue running.
- 2- If $V_{BAT}>V_{SHORT}$, the t_{30MIN} timer will continue running until the first I²C write. Then the t_{30MIN} will stop and the t_{32S} timer is started.

VBUS Over-Voltage

The FAN54110 contains programmable Over-Voltage Protection (OVP) on V_{BUS} , ranging from 6.5 V to 8.0 V, as specified in the V_{BUSOV} (Reg01h[2:1]) bits with a default setting of 7 V. If OVP is detected, the FAN54110 terminates charging functionality if charging is active when OVP is detected. The FAN54110 interrupts the host when the OVP event occurs and sets the OVP_FLAG bit.

Dynamic Input Voltage Control (DIVC)

V_{BUS} is typically 5 V +5% / -10%, depending on the charging current. If the FAN54110 is programmed to a higher current than the charger can support, a regulation control actively regulates the charging current to maintain at least 4.32V (typical) on V_{BUS} . This level is controlled via the V_{BUS_REF} (Reg02h[3:2]) bits. The FAN54110 reduces the charging current to ensure V_{BUS} is maintained above the V_{BUS_REF} setting. The DIVC regulation loop is enabled by default and disabled with the V_{BUS_REG} (Reg01h[5]) bit.

If DIVC is disabled, the charging cycle stops when V_{BUS} falls below the V_{BUS} valid falling threshold (V_{INMIN2}) or below V_{BAT} . Charging remains stopped until V_{BUS} rises above the rising V_{BUS} valid threshold (V_{INMIN1}) and stays above this threshold.

Thermal Regulation and Shutdown

The thermal regulation loop is enabled if the junction temperature reaches the threshold defined by the T_{CF} (Reg02h[5:4]) bits. When T_{CF} is reached, the FAN54110 reduces the charging current to 90 mA until the junction temperature falls below T_{CF} . Charge current is then incremented in 1 ms steps until the I_{OCHRG} level is reached. This algorithm allows for the fastest recovery from a thermal regulation event while averaging a current that keeps the temperature below T_{CF} .

The FAN54110 terminates charging completely if the junction temperature exceeds $T_{SHUTDOWN}$ (145°C).

In both cases, the temperature event is indicated via the $TREG_FLAG$ and TSD_FLAG bits in the $FAULT_INTERRUPT$ (Reg05h) register. Recovery from either event is indicated via the OT_RECOV bit in the same register.

Additional θ_{JA} data points, measured using the FAN54110 evaluation board, are given in the table below (measured with $T_A=25^\circ\text{C}$). Note that as power dissipation increases, the effective θ_{JA} decreases due to the larger difference between the die temperature and ambient.

Table 1. Evaluation Board Measured θ_{JA}

| Power (W) | θ_{JA} |
|-----------|---------------|
| 0.504 | 54°C/W |
| 0.844 | 50°C/W |
| 1.506 | 46°C/W |

Production Test Mode

Production Test Mode (PTM) provides power for the system from the USB port. This eliminates the burden of having an attached battery during production line testing.

PTM is enabled when the PTM_EN bit is HIGH and when the battery is absent (NOBAT (Reg05h[0])=1). In PTM, Q1 (see Figure 2) is turned on, but it is current limited to about 2.5 A. V_{BAT} is initially regulated to the default V_{OREG} setting of 3.54 V in PTM. However, V_{BAT} can be programmed to output any V_{OREG} from 3.38 V to 4.44 V, as specified in the VOREG (Reg04h[5:0]) bits.

Care should be taken to limit the RMS current in PTM Mode. Thermal regulation (T_{CF}) and thermal shutdown are enabled in PTM.

Charging Status and Interrupt Reporting

The STAT and POK_B pins are used to indicate to the host the presence or absence of a valid charging source, charging status, as well as fault status.

The FAULT_INTERRUPT (Reg05h[7:0]) and STATUS_INTERRUPT (Reg07h[7:5]) bits have associated MASK bits and there is a general INTERRUPT (Reg01h[0]) bit. This bit is set when any interrupt occurs, even if the occurring fault is masked. While this bit is set to 1, all subsequent STAT pulses are prevented. Reading this register clears the bit.

The FAULT_INTERRUPT and STATUS_INTERRUPT registers and the INTERRUPT (Reg01h[0]) bit should be read and cleared on every STAT pin rising edge and POK_B pin falling edge to ensure that all faults, masked or otherwise, as well as adapter presence changes are immediately available to the host.

POK_B Pin

The POK_B pin is used to indicate the presence or absence of a valid charging source to the host processor.

Table 2. POK_B Pin State

| POK_B | Charging Source |
|-------|---|
| HIGH | absent or not valid |
| LOW | V _{INMIN(1)} <V _{BUS} <V _{BUSOV} P |

STAT Pin

The STAT pin is used to indicate charging status, as well as to signal the host processor of a change in the status of the IC or system.

The static state of the STAT pin is determined by whether the IC is charging a battery:

Table 3. STAT Pin Static State

| CHARGER | NOBAT (Reg05h[0]) | STAT Pin |
|---------|-------------------|----------|
| ON | 0 | LOW |
| OFF | X | HIGH |
| X | 1 | HIGH |

The STAT pin emits a 128 μ s LOW pulse whenever an unmasked interrupt event occurs and the INTERRUPT (Reg01h[0]) bit is reset to “0”.

Any interrupt pulse that occurs while STAT is statically LOW is preceded by 128 μ s of STAT HIGH, as shown below.

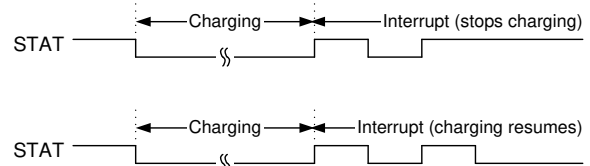


Figure 22. STAT Interrupt Pulse Behavior

Masking the STAT Pin Interrupt

The FAULT_INTERRUPT and STATUS_INTERRUPT register bits have associated MASK bits located in Reg06h[7:0] and Reg07h[3:1] that will mask STAT pin pulses.

When a mask bit is set and an event occurs:

- The associated FAULT_INTERRUPT or STATUS_INTERRUPT bit is set
- The INTERRUPT bit is set
- The STAT pin will not pulse

INTERRUPT (Reg01h[0]) Bit

When bits in the FAULT_INTERRUPT and STATUS_INTERRUPT register are set, the INTERRUPT (Reg01h[0]) bit is set before the falling edge of STAT.

If additional interrupt conditions occur before the host clears the INTERRUPT bit by reading Reg01h, the STAT pin does not pulse.

I²C Interface

The serial interface is compatible with Standard Mode and Fast Mode I²C bus specifications. The SCL line is an input and the SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

Slave Address

Table 4. I²C Slave Address Byte

| | | | | | | | |
|---|---|---|---|---|---|---|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | R/W |

In hex notation, the slave address assumes a 0 LSB. The hex slave address for the FAN54110 is D6.

Bus Timing

As shown below, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions at or shortly after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

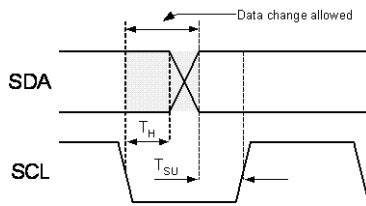


Figure 23. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown below.

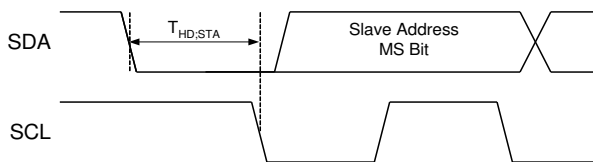


Figure 24. Start Bit

A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 25.

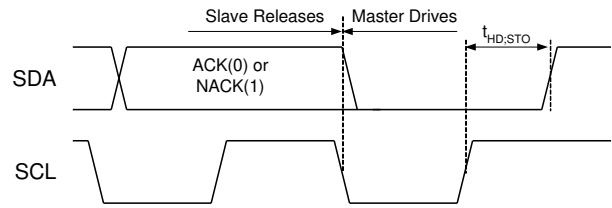


Figure 25. Stop Bit

During a read from the FAN54110, the master issues a Repeated Start after sending the register address and before resending the slave address. The Repeated Start is a 1-to-0 transition on SDA while SCL is HIGH, as shown below.

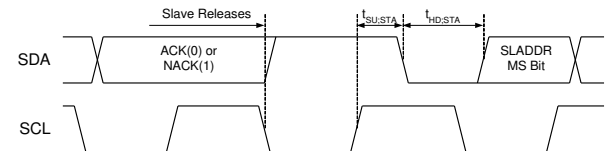


Figure 26. Repeated Start Timing

Read and Write Transactions

The figures below outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as **Master Drives Bus** and **Slave Drives Bus**. All addresses and data are MSB first.

Table 5. Bit Definitions for Write and Read Transactions

| Symbol | Definition |
|-----------|---|
| S | START, <i>see</i> Figure 24. |
| A | ACK. The slave drives SDA to 0 to acknowledge the preceding packet. |
| \bar{A} | NACK. The slave sends a 1 to NACK the preceding packet. |
| R | Repeated START, <i>see</i> Figure 26 |
| P | STOP, <i>see</i> Figure 25 |



Figure 27. Write Transaction



Figure 28. Read Transaction

Register Descriptions

Table 6. Register Bit Definitions

Default values are in bold text with VBUS removed and VBAT=3.8V.

| Bit | Name | Type | Description |
|----------------|--------|---------------------------------|--|
| IC_INFO | | Register Address: 00h | |
| | | Default= 100X XXXX (XXh) | |
| 7:5 | VENDOR | R | 100 : Identifies ON Semiconductor as the supplier |
| 4:3 | PN | R | Part number bits, <i>see the Ordering Info on page 2</i> |
| 2:0 | REV | R | IC Revision. Revision is 1.X, where X is the decimal of these 3 bits |

| CHARGE_CTRL1 | | Register Address: 01h | | Default=0011 0010 (32h) | |
|---------------------|-----------|------------------------------|---|--------------------------------|--------------------------|
| 7 | RESET | W | Setting this bit to 1 resets all registers to default values and deactivates t_{32S} , causing the part to go to into IDLE State until the next I ² C write reactivates t_{32S} . This bit returns 0 when read. | | |
| 6 | HZ_MODE | R/W | 0 : Charging is enabled. 1: Charging is disabled. | | |
| 5 | VBUS_REG | R/W | 0 : VBUS regulation loop disabled. 1 : VBUS regulation loop enabled. | | |
| 4 | VBUS_LOOP | R | 0 : VBUS regulation loop is enabled and is active ($V_{BUS}=V_{BUS_REF}$). 1 : VBUS > VBUS_REF or VBUS regulation loop is disabled. | | |
| 3 | Reserved | R | This bit returns 0 when read. | | |
| 2:1 | VBUSOVP | R/W | When VBUS is at or above this threshold, a VBUS OVP fault is enunciated and the charger is disabled until the fault clears. Table 7. VBUSOVP Threshold | | |
| | | | | [2:1] | VBUSOVP Threshold |
| | | | | 00 | 6.5 |
| | | | | 01 | 7.0 |
| | | | | 10 | 7.5 |
| | | | | 11 | 8.0 |
| 0 | INTERRUPT | RC | A 1 indicates that a fault has occurred. <i>See the Charging Status and Interrupt Reporting section for details.</i> While this bit is set to 1, all subsequent STAT pulses are prevented. Reading this register clears the bit. | | |

| CHARGE_CTRL2 | | Register Address: 02h | | Default=0010 0111 (27h) | | | | | | | | | | | | | | | |
|--------------|-----------------|-----------------------|---|-------------------------|-----|-----|----------------------|---|----|------|----------|-----------|-------------|----------|-----------|------------|---|----|------|
| 7 | PTM_EN | R/W | 0: Normal operation 1: Production Test Mode is enabled if NOBAT (Reg5[0])=1. See the <i>Production Test Mode section for details.</i> | | | | | | | | | | | | | | | | |
| 6 | Reserved | R | This bit returns 0 when read. | | | | | | | | | | | | | | | | |
| 5:4 | T _{CF} | R/W | Temperature threshold at which the current is reduced to allow the device to cool. See the <i>Thermal Regulation and Shutdown section for details.</i> Table 8. Temperature Threshold Settings <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>DEC</th> <th>BIN</th> <th>T_{CF}</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>00</td> <td>70</td> </tr> <tr> <td>1</td> <td>01</td> <td>85</td> </tr> <tr> <td>2</td> <td>10</td> <td>100</td> </tr> <tr> <td>3</td> <td>11</td> <td>120</td> </tr> </tbody> </table> | | DEC | BIN | T _{CF} | 0 | 00 | 70 | 1 | 01 | 85 | 2 | 10 | 100 | 3 | 11 | 120 |
| DEC | BIN | T _{CF} | | | | | | | | | | | | | | | | | |
| 0 | 00 | 70 | | | | | | | | | | | | | | | | | |
| 1 | 01 | 85 | | | | | | | | | | | | | | | | | |
| 2 | 10 | 100 | | | | | | | | | | | | | | | | | |
| 3 | 11 | 120 | | | | | | | | | | | | | | | | | |
| 3:2 | VBUS_REF | R/W | Sets the V _{BUS_REF} threshold. Table 9. V_{BUS_REF} Threshold <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>DEC</th> <th>BIN</th> <th>V_{BUS_REF}</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>00</td> <td>4.22</td> </tr> <tr> <td>1</td> <td>01</td> <td>4.32</td> </tr> <tr> <td>2</td> <td>10</td> <td>4.37</td> </tr> <tr> <td>3</td> <td>11</td> <td>4.46</td> </tr> </tbody> </table> | | DEC | BIN | V _{BUS_REF} | 0 | 00 | 4.22 | 1 | 01 | 4.32 | 2 | 10 | 4.37 | 3 | 11 | 4.46 |
| DEC | BIN | V _{BUS_REF} | | | | | | | | | | | | | | | | | |
| 0 | 00 | 4.22 | | | | | | | | | | | | | | | | | |
| 1 | 01 | 4.32 | | | | | | | | | | | | | | | | | |
| 2 | 10 | 4.37 | | | | | | | | | | | | | | | | | |
| 3 | 11 | 4.46 | | | | | | | | | | | | | | | | | |
| 1 | VRCH_DIS | R/W | 0: Charging re-starts if V _{BAT} < V _{OREG} -V _{RCH} . 1: Charging does not re-start automatically if V_{BAT} drops. | | | | | | | | | | | | | | | | |
| 0 | ITERM_DIS | R/W | 0: Charging terminates at the programmed I _{TERM} level. 1: Charging does not terminate at the programmed I_{TERM} level. | | | | | | | | | | | | | | | | |

| IBAT | Register Address: 03h | Default=0010 0110 (26h) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|-----------------------|--------------------------|-----|-----|--------------------------|---|------|-----|---|------|-----|----------|-------------|------------|---|------|-----|---|------|-----|---|------|-----|----------|-------------|-----------|---|------|-----|---|------|-----|---|------|-----|----|------|-----|----|------|-----|----|------|-----|----|------|-----|----|------|-----|----|------|------|
| 7:4 | I _{CHARGE} | R/W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <p>Charge current, I_{CHRG}, is the maximum current drawn from VBUS during charging. Current consumed by the 3.3 V LDO, therefore, reduces the current available to charge the battery.</p> <p>Table 10. I_{CHARGE} Settings</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>DEC</th> <th>BIN</th> <th>I_{CHARGE} (mA)</th> </tr> </thead> <tbody> <tr><td>0</td><td>0000</td><td>100</td></tr> <tr><td>1</td><td>0001</td><td>300</td></tr> <tr><td>2</td><td>0010</td><td>350</td></tr> <tr><td>3</td><td>0011</td><td>400</td></tr> <tr><td>4</td><td>0100</td><td>450</td></tr> <tr><td>5</td><td>0101</td><td>500</td></tr> <tr><td>6</td><td>0110</td><td>550</td></tr> <tr><td>7</td><td>0111</td><td>600</td></tr> <tr><td>8</td><td>1000</td><td>650</td></tr> <tr><td>9</td><td>1001</td><td>700</td></tr> <tr><td>10</td><td>1010</td><td>750</td></tr> <tr><td>11</td><td>1011</td><td>800</td></tr> <tr><td>12</td><td>1100</td><td>850</td></tr> <tr><td>13</td><td>1101</td><td>900</td></tr> <tr><td>14</td><td>1110</td><td>950</td></tr> <tr><td>15</td><td>1111</td><td>1000</td></tr> </tbody> </table> | | | DEC | BIN | I _{CHARGE} (mA) | 0 | 0000 | 100 | 1 | 0001 | 300 | 2 | 0010 | 350 | 3 | 0011 | 400 | 4 | 0100 | 450 | 5 | 0101 | 500 | 6 | 0110 | 550 | 7 | 0111 | 600 | 8 | 1000 | 650 | 9 | 1001 | 700 | 10 | 1010 | 750 | 11 | 1011 | 800 | 12 | 1100 | 850 | 13 | 1101 | 900 | 14 | 1110 | 950 | 15 | 1111 | 1000 |
| DEC | BIN | I _{CHARGE} (mA) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0000 | 100 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0001 | 300 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | 0010 | 350 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | 0011 | 400 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | 0100 | 450 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | 0101 | 500 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | 0110 | 550 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | 0111 | 600 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | 1000 | 650 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | 1001 | 700 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 | 1010 | 750 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11 | 1011 | 800 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 12 | 1100 | 850 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 13 | 1101 | 900 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 14 | 1110 | 950 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 15 | 1111 | 1000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3:0 | I _{TERM} | R/W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <p>Table 11. I_{TERM} Settings</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>DEC</th> <th>BIN</th> <th>I_{TERM} (mA)</th> </tr> </thead> <tbody> <tr><td>0</td><td>0000</td><td>20</td></tr> <tr><td>1</td><td>0001</td><td>30</td></tr> <tr><td>2</td><td>0010</td><td>40</td></tr> <tr><td>3</td><td>0011</td><td>50</td></tr> <tr><td>4</td><td>0100</td><td>60</td></tr> <tr><td>5</td><td>0101</td><td>70</td></tr> <tr><td>6</td><td>0110</td><td>80</td></tr> <tr><td>7</td><td>0111</td><td>90</td></tr> <tr><td>8</td><td>1000</td><td>100</td></tr> <tr><td>9</td><td>1001</td><td>110</td></tr> <tr><td>10</td><td>1010</td><td>120</td></tr> <tr><td>11</td><td>1011</td><td>130</td></tr> <tr><td>12</td><td>1100</td><td>140</td></tr> <tr><td>13</td><td>1101</td><td>150</td></tr> <tr><td>14</td><td>1110</td><td>160</td></tr> <tr><td>15</td><td>1111</td><td>170</td></tr> </tbody> </table> | | | DEC | BIN | I _{TERM} (mA) | 0 | 0000 | 20 | 1 | 0001 | 30 | 2 | 0010 | 40 | 3 | 0011 | 50 | 4 | 0100 | 60 | 5 | 0101 | 70 | 6 | 0110 | 80 | 7 | 0111 | 90 | 8 | 1000 | 100 | 9 | 1001 | 110 | 10 | 1010 | 120 | 11 | 1011 | 130 | 12 | 1100 | 140 | 13 | 1101 | 150 | 14 | 1110 | 160 | 15 | 1111 | 170 |
| DEC | BIN | I _{TERM} (mA) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0000 | 20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0001 | 30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | 0010 | 40 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | 0011 | 50 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | 0100 | 60 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | 0101 | 70 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | 0110 | 80 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | 0111 | 90 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | 1000 | 100 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | 1001 | 110 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 | 1010 | 120 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11 | 1011 | 130 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 12 | 1100 | 140 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 13 | 1101 | 150 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 14 | 1110 | 160 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 15 | 1111 | 170 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| OREG | | Register Address: 04h | | Default=0000 1000 (08h) | | | | | | |
|------|----------|-----------------------|--------------------------------|-------------------------|------------|-------------------------|------------|------------|------------|-------------------------|
| 7:6 | Reserved | R | These bits return 0 when read. | | | | | | | |
| 5:0 | VOREG | R/W | Table 12. OREG Settings | | | | | | | |
| | | | DEC | BIN | HEX | V_{OREG} | DEC | BIN | HEX | V_{OREG} |
| | | | 0 | 000000 | 00 | 3.38 | 32 | 100000 | 20 | 4.02 |
| | | | 1 | 000001 | 01 | 3.40 | 33 | 100001 | 21 | 4.04 |
| | | | 2 | 000010 | 02 | 3.42 | 34 | 100010 | 22 | 4.06 |
| | | | 3 | 000011 | 03 | 3.44 | 35 | 100011 | 23 | 4.08 |
| | | | 4 | 000100 | 04 | 3.46 | 36 | 100100 | 24 | 4.10 |
| | | | 5 | 000101 | 05 | 3.48 | 37 | 100101 | 25 | 4.12 |
| | | | 6 | 000110 | 06 | 3.50 | 38 | 100110 | 26 | 4.14 |
| | | | 7 | 000111 | 07 | 3.52 | 39 | 100111 | 27 | 4.16 |
| | | | 8 | 001000 | 08 | 3.54 | 40 | 101000 | 28 | 4.18 |
| | | | 9 | 001001 | 09 | 3.56 | 41 | 101001 | 29 | 4.20 |
| | | | 10 | 001010 | 0A | 3.58 | 42 | 101010 | 2A | 4.22 |
| | | | 11 | 001011 | 0B | 3.60 | 43 | 101011 | 2B | 4.24 |
| | | | 12 | 001100 | 0C | 3.62 | 44 | 101100 | 2C | 4.26 |
| | | | 13 | 001101 | 0D | 3.64 | 45 | 101101 | 2D | 4.28 |
| | | | 14 | 001110 | 0E | 3.66 | 46 | 101110 | 2E | 4.30 |
| | | | 15 | 001111 | 0F | 3.68 | 47 | 101111 | 2F | 4.32 |
| | | | 16 | 010000 | 10 | 3.70 | 48 | 110000 | 30 | 4.34 |
| | | | 17 | 010001 | 11 | 3.72 | 49 | 110001 | 31 | 4.36 |
| | | | 18 | 010010 | 12 | 3.74 | 50 | 110010 | 32 | 4.38 |
| | | | 19 | 010011 | 13 | 3.76 | 51 | 110011 | 33 | 4.40 |
| | | | 20 | 010100 | 14 | 3.78 | 52 | 110100 | 34 | 4.42 |
| | | | 21 | 010101 | 15 | 3.80 | 53 | 110101 | 35 | 4.44 |
| | | | 22 | 010110 | 16 | 3.82 | 54 | 110110 | 36 | 4.44 |
| | | | 23 | 010111 | 17 | 3.84 | 55 | 110111 | 37 | 4.44 |
| | | | 24 | 011000 | 18 | 3.86 | 56 | 111000 | 38 | 4.44 |
| | | | 25 | 011001 | 19 | 3.88 | 57 | 111001 | 39 | 4.44 |
| | | | 26 | 011010 | 1A | 3.90 | 58 | 111010 | 3A | 4.44 |
| | | | 27 | 011011 | 1B | 3.92 | 59 | 111011 | 3B | 4.44 |
| | | | 28 | 011100 | 1C | 3.94 | 60 | 111100 | 3C | 4.44 |
| | | | 29 | 011101 | 1D | 3.96 | 61 | 111101 | 3D | 4.44 |
| 30 | 011110 | 1E | 3.98 | 62 | 111110 | 3E | 4.44 | | | |
| 31 | 011111 | 1F | 4.00 | 63 | 111111 | 3F | 4.44 | | | |

| FAULT_INTERRUPT Register Address: 05h | | | Default=0000 0000 (00h) | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--|-----------------|--|---|-----------|--|-----------|---|----------|---|---|----------|-----------------------------------|---|-----------|---------------------------------------|---|-------|-----------------------------|---|--------|---|---|----------|--|---|-----------|---------------------------------|---|-------|--|
| 7:0 | FAULT_INTERRUPT | R | <p>A 1 for a given bit indicates that a specific fault has occurred as described in the table below. Items in blue are transient conditions, whose bits are cleared when this register is read. The other interrupts herein are not cleared unless the underlying condition has been removed.</p> <p><i>See the Charging Status and Interrupt Reporting section for details.</i></p> <p>Table 13. Charger Interrupt Conditions</p> <table border="1"> <thead> <tr> <th>Bit #</th> <th>FLAG</th> <th>Interrupt</th> </tr> </thead> <tbody> <tr> <td>7</td> <td>TSD_FLAG</td> <td>Thermal shutdown ($T_J > 145^{\circ}\text{C}$).</td> </tr> <tr> <td>6</td> <td>OVP_FLAG</td> <td>VBUS OVP (over-voltage shutdown).</td> </tr> <tr> <td>5</td> <td>TREG_FLAG</td> <td>Charger thermal regulation is active.</td> </tr> <tr> <td>4</td> <td>TC_TO</td> <td>T32Sec timer has timed out.</td> </tr> <tr> <td>3</td> <td>DBP_TO</td> <td>Dead-Battery (DBP) timer (T30) has timed out.</td> </tr> <tr> <td>2</td> <td>OT_RECOV</td> <td>Die temperature has fallen below 120°C.</td> </tr> <tr> <td>1</td> <td>OVP_RECOV</td> <td>VBUS OVP recovery has occurred.</td> </tr> <tr> <td>0</td> <td>NOBAT</td> <td>Battery absence was detected either at VBUS POR or after Charge Termination.</td> </tr> </tbody> </table> | Bit # | FLAG | Interrupt | 7 | TSD_FLAG | Thermal shutdown ($T_J > 145^{\circ}\text{C}$). | 6 | OVP_FLAG | VBUS OVP (over-voltage shutdown). | 5 | TREG_FLAG | Charger thermal regulation is active. | 4 | TC_TO | T32Sec timer has timed out. | 3 | DBP_TO | Dead-Battery (DBP) timer (T30) has timed out. | 2 | OT_RECOV | Die temperature has fallen below 120°C . | 1 | OVP_RECOV | VBUS OVP recovery has occurred. | 0 | NOBAT | Battery absence was detected either at VBUS POR or after Charge Termination. |
| | | | Bit # | FLAG | Interrupt | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 7 | TSD_FLAG | Thermal shutdown ($T_J > 145^{\circ}\text{C}$). | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 6 | OVP_FLAG | VBUS OVP (over-voltage shutdown). | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 5 | TREG_FLAG | Charger thermal regulation is active. | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 4 | TC_TO | T32Sec timer has timed out. | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 3 | DBP_TO | Dead-Battery (DBP) timer (T30) has timed out. | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 2 | OT_RECOV | Die temperature has fallen below 120°C . | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1 | OVP_RECOV | VBUS OVP recovery has occurred. | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | NOBAT | Battery absence was detected either at VBUS POR or after Charge Termination. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| FAULT_MASK Register Address: 06h | | | Default=0000 0000 (00h) | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---------|---------------------------------|--|-------------|--|-----------|---|------------|--|---|------------|--|---|-------------|----------------------------------|---|---------|-----------------------------|---|----------|---|---|------------|--------------------------------|---|-------------|-------------------------|---|---------|---------------------------------|
| 7:0 | MASK | R/W | <p>A mask bit of 1 prevents an interrupt pulse from being generated on the STAT pin. The INTERRUPT (Reg01h[0]) bit and corresponding FAULT_INTERRUPT register bit are still written.</p> <p><i>See the Charging Status and Interrupt Reporting section for details.</i></p> <table border="1"> <thead> <tr> <th>Bit #</th> <th>FLAG</th> <th>Interrupt</th> </tr> </thead> <tbody> <tr> <td>7</td> <td>TSD_FLAG_M</td> <td>Mask thermal shutdown ($T_J > 145^{\circ}\text{C}$).</td> </tr> <tr> <td>6</td> <td>OVP_FLAG_M</td> <td>Mask VBUS OVP (over-voltage shutdown).</td> </tr> <tr> <td>5</td> <td>TREG_FLAG_M</td> <td>Mask charger thermal regulation.</td> </tr> <tr> <td>4</td> <td>TC_TO_M</td> <td>Mask T32Sec timer time out.</td> </tr> <tr> <td>3</td> <td>DBP_TO_M</td> <td>Mask Dead-Battery (DBP) timer (t30) time out.</td> </tr> <tr> <td>2</td> <td>OT_RECOV_M</td> <td>Mask Die temperature recovery.</td> </tr> <tr> <td>1</td> <td>OVP_RECOV_M</td> <td>Mask VBUS OVP recovery.</td> </tr> <tr> <td>0</td> <td>NOBAT_M</td> <td>Mask battery absence detection.</td> </tr> </tbody> </table> | Bit # | FLAG | Interrupt | 7 | TSD_FLAG_M | Mask thermal shutdown ($T_J > 145^{\circ}\text{C}$). | 6 | OVP_FLAG_M | Mask VBUS OVP (over-voltage shutdown). | 5 | TREG_FLAG_M | Mask charger thermal regulation. | 4 | TC_TO_M | Mask T32Sec timer time out. | 3 | DBP_TO_M | Mask Dead-Battery (DBP) timer (t30) time out. | 2 | OT_RECOV_M | Mask Die temperature recovery. | 1 | OVP_RECOV_M | Mask VBUS OVP recovery. | 0 | NOBAT_M | Mask battery absence detection. |
| | | | Bit # | FLAG | Interrupt | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 7 | TSD_FLAG_M | Mask thermal shutdown ($T_J > 145^{\circ}\text{C}$). | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 6 | OVP_FLAG_M | Mask VBUS OVP (over-voltage shutdown). | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 5 | TREG_FLAG_M | Mask charger thermal regulation. | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 4 | TC_TO_M | Mask T32Sec timer time out. | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 3 | DBP_TO_M | Mask Dead-Battery (DBP) timer (t30) time out. | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 2 | OT_RECOV_M | Mask Die temperature recovery. | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1 | OVP_RECOV_M | Mask VBUS OVP recovery. | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | NOBAT_M | Mask battery absence detection. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

STATUS_INTERRUPT **Default=0100 0000 (40h)** **Register Address: 07h**

| | | | <p>Items in blue are transient conditions, whose bits are cleared when this register is read. The other interrupts herein are not cleared unless the underlying condition has been removed. See the Charging Status and Interrupt Reporting section for details.</p> <p>Table 14. VBUS Interrupt Conditions</p> <table border="1"> <thead> <tr> <th>Bit #</th> <th>FLAG</th> <th>Interrupt Generated</th> </tr> </thead> <tbody> <tr> <td>7</td> <td>VBUS_CON</td> <td>1 when OVP > V_{BUS} > V_{IIN(MIN)}1 at VBUS POR from VBUS Insertion. 0 when VBUS is disconnected. VBUS_CON does not de-assert when a VBUS_OVP condition occurs after VBUS validation is successful.</td> </tr> <tr> <td>6</td> <td>POK_B</td> <td>State of the POK_B pin</td> </tr> <tr> <td>5</td> <td>VALIDATION FAIL</td> <td>1 indicates VBUS validation is attempted and failed. After a failure, VBUS validation is attempted every two seconds.</td> </tr> </tbody> </table> | Bit # | FLAG | Interrupt Generated | 7 | VBUS_CON | 1 when OVP > V _{BUS} > V _{IIN(MIN)} 1 at VBUS POR from VBUS Insertion. 0 when VBUS is disconnected. VBUS_CON does not de-assert when a VBUS_OVP condition occurs after VBUS validation is successful. | 6 | POK_B | State of the POK_B pin | 5 | VALIDATION FAIL | 1 indicates VBUS validation is attempted and failed. After a failure, VBUS validation is attempted every two seconds. |
|-------|----------------------|---|--|-------|------|---------------------|---------------|----------|---|---|----------------------|------------------------|---|-----------------|---|
| Bit # | FLAG | Interrupt Generated | | | | | | | | | | | | | |
| 7 | VBUS_CON | 1 when OVP > V _{BUS} > V _{IIN(MIN)} 1 at VBUS POR from VBUS Insertion. 0 when VBUS is disconnected. VBUS_CON does not de-assert when a VBUS_OVP condition occurs after VBUS validation is successful. | | | | | | | | | | | | | |
| 6 | POK_B | State of the POK_B pin | | | | | | | | | | | | | |
| 5 | VALIDATION FAIL | 1 indicates VBUS validation is attempted and failed. After a failure, VBUS validation is attempted every two seconds. | | | | | | | | | | | | | |
| 4 | Reserved | R | This bit returns 0 when read. | | | | | | | | | | | | |
| | | | <p>A mask bit of 1 prevents an interrupt pulse from being generated on the STAT pin. The INTERRUPT (Reg01h[0]) bit and corresponding VBUS_STAT bit are still written. See the Charging Status and Interrupt Reporting section for details.</p> <p>Table 15. VBUS Interrupt Mask Bits</p> <table border="1"> <thead> <tr> <th>Bit #</th> <th>Mask</th> </tr> </thead> <tbody> <tr> <td>3</td> <td>VBUS_CON MASK</td> </tr> <tr> <td>2</td> <td>POK_B MASK</td> </tr> <tr> <td>1</td> <td>VALIDATION FAIL MASK</td> </tr> </tbody> </table> | Bit # | Mask | 3 | VBUS_CON MASK | 2 | POK_B MASK | 1 | VALIDATION FAIL MASK | | | | |
| Bit # | Mask | | | | | | | | | | | | | | |
| 3 | VBUS_CON MASK | | | | | | | | | | | | | | |
| 2 | POK_B MASK | | | | | | | | | | | | | | |
| 1 | VALIDATION FAIL MASK | | | | | | | | | | | | | | |
| 3:1 | VBUS_MASK | R/W | | | | | | | | | | | | | |
| 0 | Reserved | R | This bit returns 0 when read. | | | | | | | | | | | | |

TMR_RST **Register Address: 08h** **Default=0000 0000 (00h)**

| | | | |
|-----|----------|---|---|
| 7 | TMR_RST | W | Setting this bit to 1 resets the t _{32s} timer, allowing the IC to continue charging under control of the I ² C host. This bit returns 0 when read. |
| 6:0 | Reserved | R | These bits return 0 when read. |

MONITOR0 **Register Address: 10h** **Default=1000 0010 (82h)**

| | | | |
|-----|-----------|---|--|
| 7 | ITERM_CMP | R | 0: I _{BAT} < I _{TERM} reference 1: I _{BAT} > I _{TERM} reference |
| 6 | VBUS_VBAT | R | 0: V _{BUS} < V _{BAT} 1: V _{BUS} > V _{BAT} |
| 5 | VSHORT | R | 0: V _{BAT} > V _{SHORT} or IC is not charging. 1: V _{BAT} < V _{SHORT} and IC is charging. |
| 4 | DIS_LEVEL | R | 0: DIS pin is LOW. This bit always reads 0 when VBUS is disconnected. 1: DIS pin is HIGH. |
| 3:2 | Reserved | R | This bit returns 0 when read. |
| 1 | ICHG | R | 0: ICHG loop is controlling the charge current. 1: ICHG loop is not limiting the charge current. |
| 0 | CV | R | 0: Charger is not in Constant Voltage (CV) Mode. Charger is either off or another loop (VBUS or ICHG) is limiting charge current. 1: Charger is on and in Constant Voltage (CV) Mode. |

PCB Layout Recommendations

Bypass capacitors should be placed as close to the IC as possible. All power and ground pins should be routed to their bypass capacitors using top copper. Copper area connecting to the IC should be maximized to improve thermal performance.

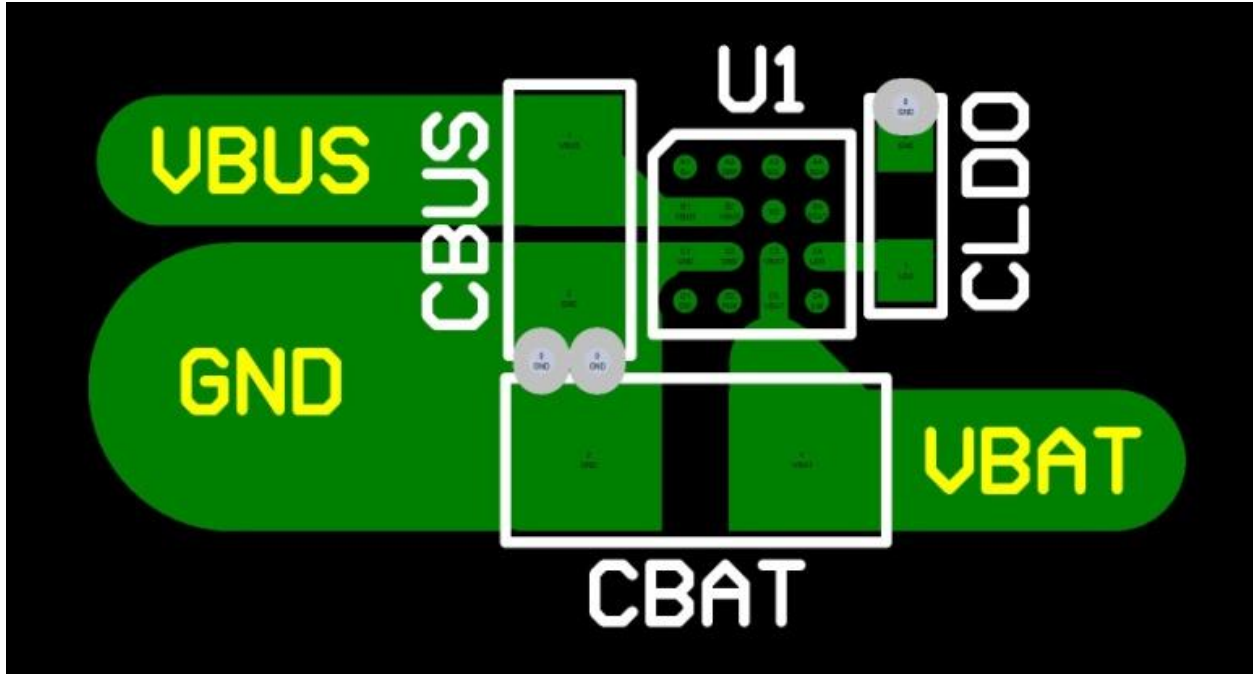


Figure 29. Recommended PCB Layout

Physical Dimensions

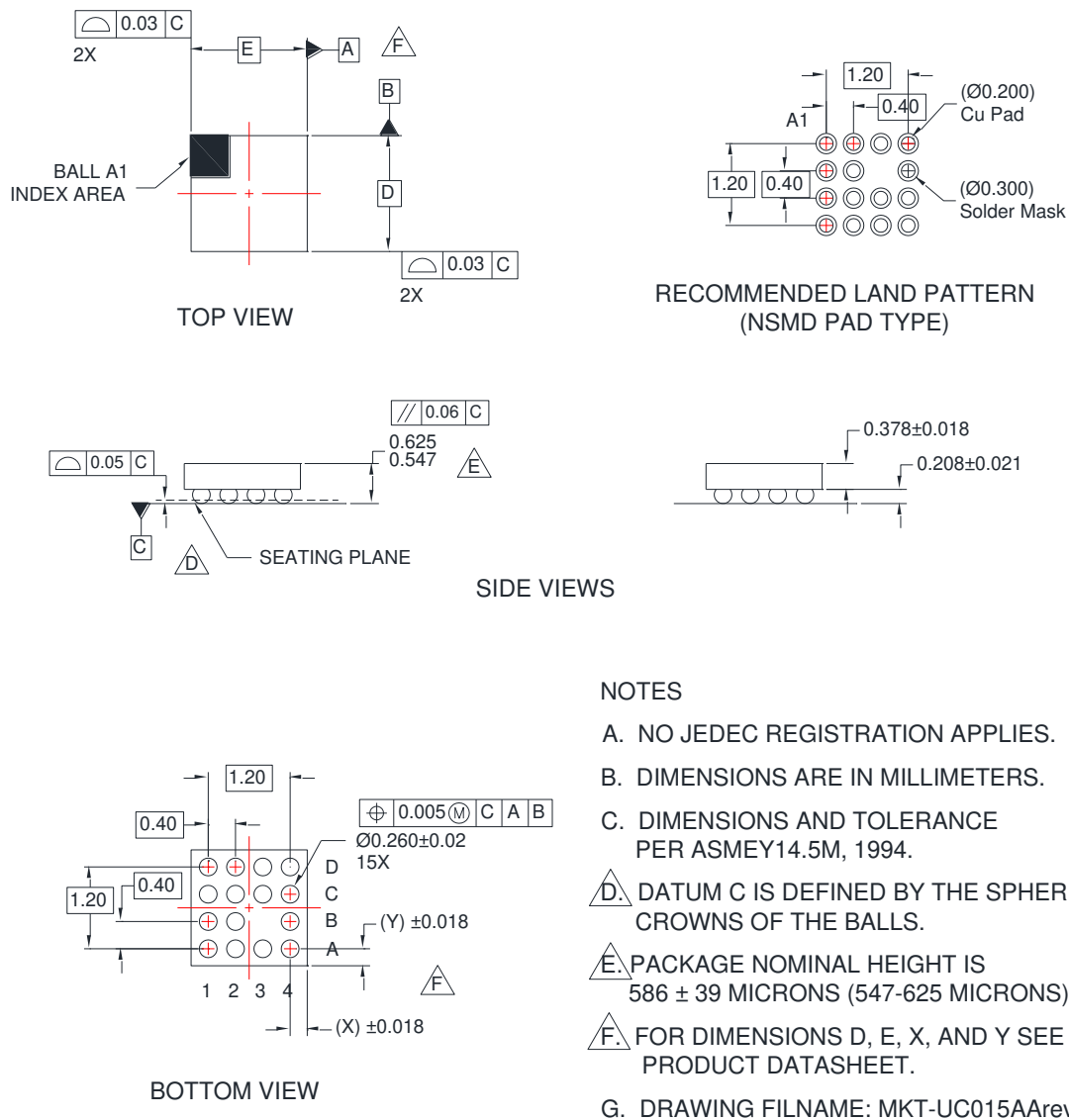


Figure 30. 15-Ball WLCSP, 0.4 mm Pitch, 250 µm Balls

Product-Specific Dimensions

| D | E | X | Y |
|--------------|---------------|-------|-------|
| 1.560 ±0.030 | 1.560 ± 0.030 | 0.180 | 0.180 |

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