



PSMN5R6-100YSF

NextPower 100 V, 6 mΩ N-channel MOSFET in LFPAK56 package

19 February 2018

Preliminary data sheet

1. General description

NextPower 100 V standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial & consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- Qualified to 175 °C
- Low $Q_G \times R_{DSon}$ FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{as})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LFPAK56 package
- Wave-solderable LFPAK56 package

3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- BLDC motor control
- USB-PD and mobile fast-charge adapters
- LED lighting
- Full-bridge and half-bridge applications
- Flyback and resonant topologies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V	
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ Fig. 2	-	-	120	A	
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Fig. 1	-	-	294	W	
T_j	junction temperature		-55	-	175	°C	
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ Fig. 10	-	4.5	5.6	mΩ	
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 100\text{ °C};$ Fig. 11	-	7.3	8.7	mΩ	
Dynamic characteristics							
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}; V_{DS} = 50\text{ V}; V_{GS} = 10\text{ V};$ Fig. 12 ; Fig. 13	-	13.5	-	nC	
$Q_{G(tot)}$	total gate charge		-	65.1	-	nC	

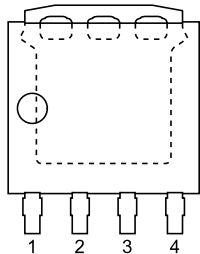
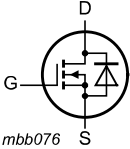
NextPower 100 V, 6 mΩ N-channel MOSFET in LFPAK56 package

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 41.8\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 10\text{ V}$; $T_{J(init)} = 25\text{ }^\circ\text{C}$; Fig. 4; Unclamped	[1]	-	440	mJ
Source-drain diode						
Q_r	recovered charge	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; Fig. 16	-	67.3	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFPAK56E; Power-SO8 (SOT1023)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN5R6-100YSF	LFPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LFPAK56); 4 leads; 1.27 mm pitch; 4.58 mm x 5.13 mm x 1.03 mm body	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN5R6-100YSF	5F6S10

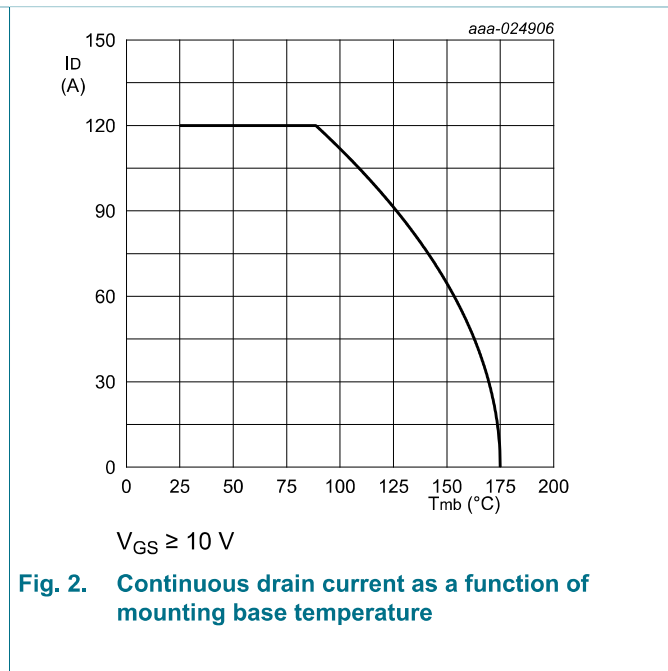
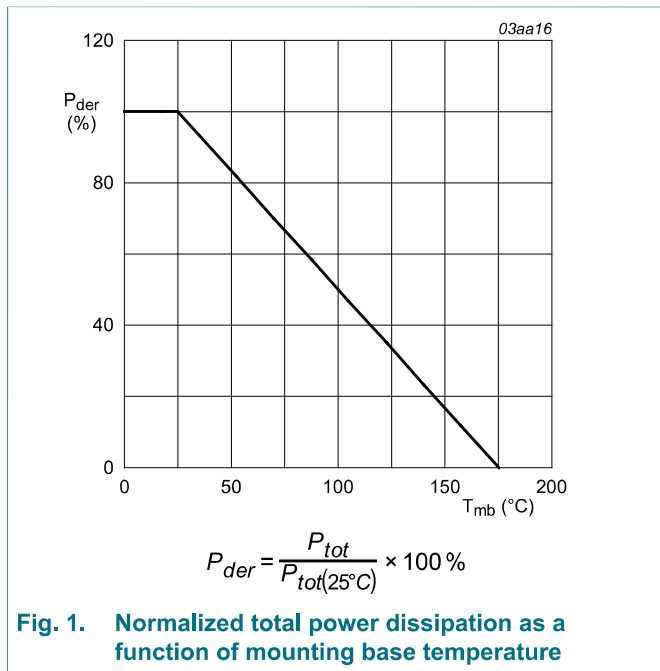
8. Limiting values

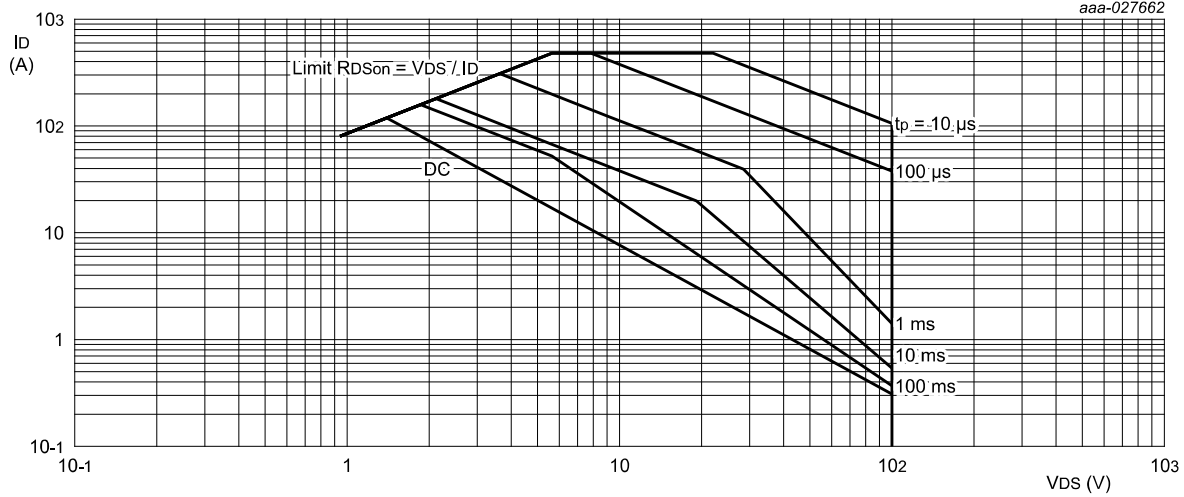
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	100	V
V _{DGR}	drain-gate voltage	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	100	V
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	294	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	-	120	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	-	112	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3	-	480	A
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	120	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	480	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 41.8 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; Fig. 4 ; Unclamped	[1]	-	440 mJ
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 100 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω	[1]	-	41.8 A

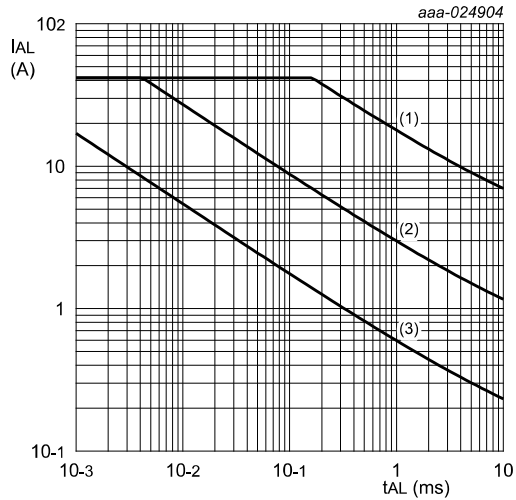
[1] Protected by 100% test





$T_{mb} = 25 \text{ }^\circ\text{C}$; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j(init)} = 25 \text{ }^\circ\text{C}$; (2) $T_{j(init)} = 150 \text{ }^\circ\text{C}$; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.45	0.51	K/W

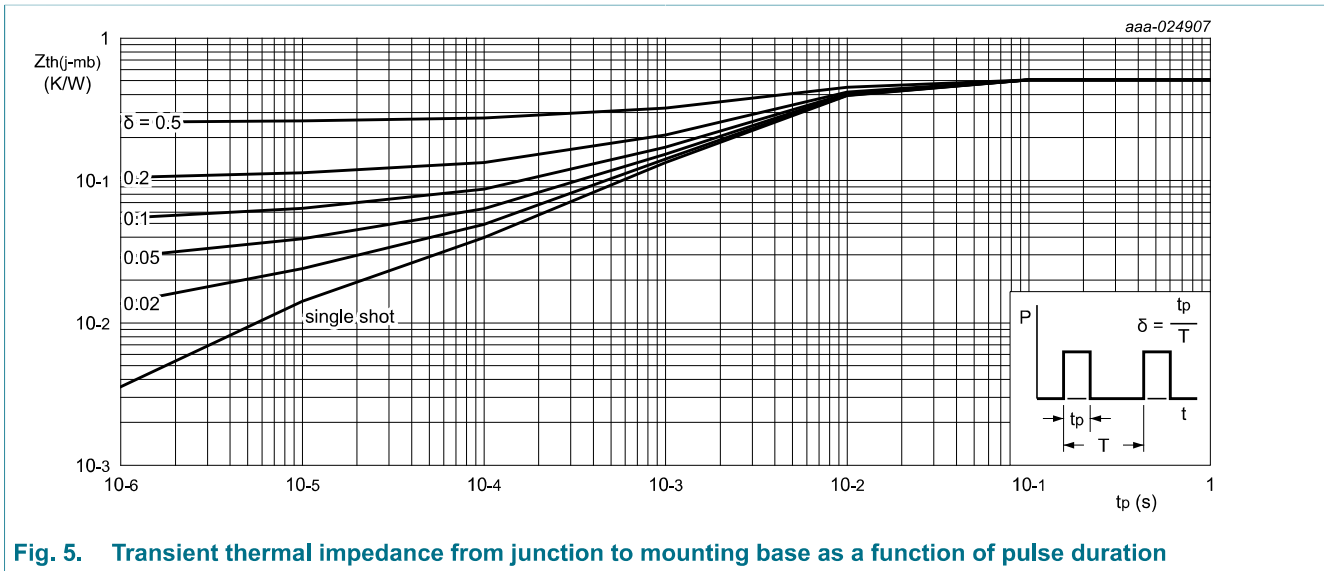


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$	-	3.6	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$	-	1.8	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 9}$	2	3.1	4	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 175 \text{ }^\circ C$	-	-8.8	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.03	5	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	5	100	nA
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	5	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C; \text{ Fig. 10}$	-	4.5	5.6	mΩ
		$V_{GS} = 7 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C; \text{ Fig. 10}$	-	5.1	7.9	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ C; \text{ Fig. 11}$	-	7.3	8.7	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C; \text{ Fig. 11}$	-	10.3	12.3	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	-	0.9	-	Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 12; Fig. 13	-	65.1	-	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V	-	32.2	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 12; Fig. 13	-	20.4	-	nC
Q _{GS(th)}	pre-threshold gate-source charge		-	12.5	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	7.9	-	nC
Q _{GD}	gate-drain charge		-	13.5	-	nC
V _{GS(pl)}	gate-source plateau voltage		I _D = 25 A; V _{DS} = 50 V; Fig. 12; Fig. 13	-	4.8	-
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 14	-	4616	-	pF
C _{oss}	output capacitance		-	805	-	pF
C _{rss}	reverse transfer capacitance		-	12	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _j = 25 °C	-	17.4	-	ns
t _r	rise time		-	16.3	-	ns
t _{d(off)}	turn-off delay time		-	35.1	-	ns
t _f	fall time		-	19.7	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 15	-	0.8	1.2	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; Fig. 16	-	51.4	-	ns
Q _r	recovered charge		-	67.3	-	nC

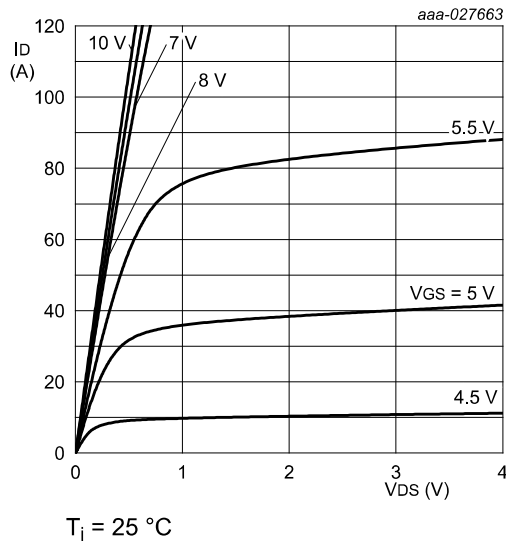


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

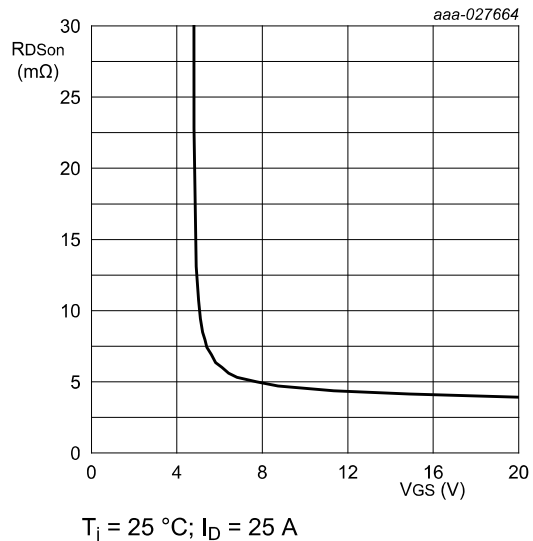


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

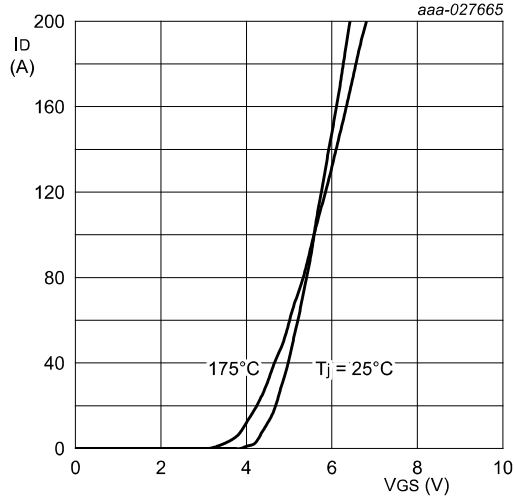


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

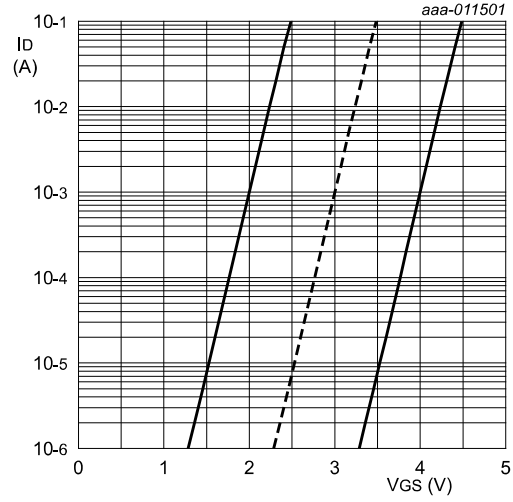


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

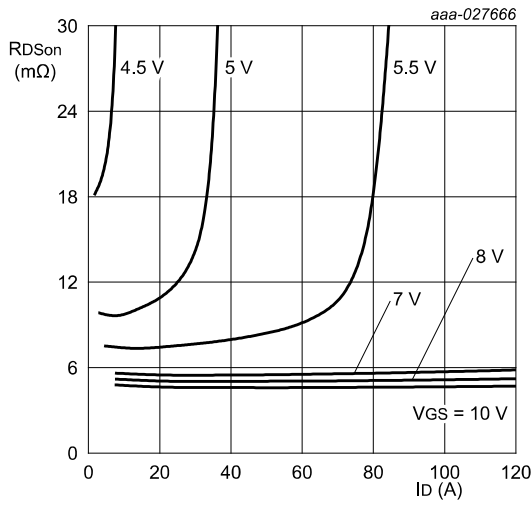
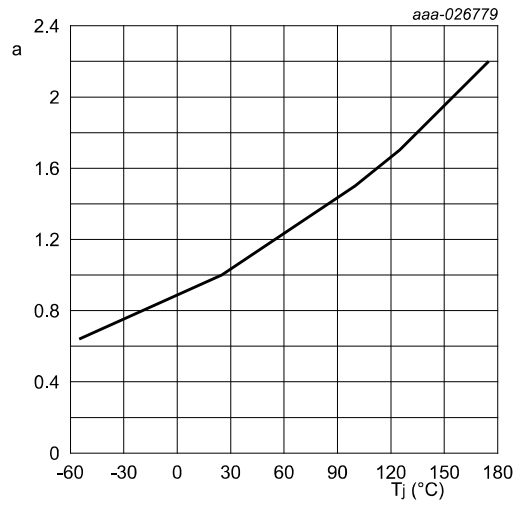
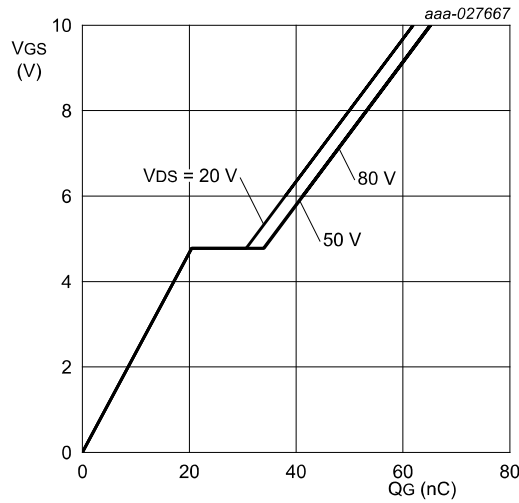


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

Fig. 12. Gate-source voltage as a function of gate charge; typical values

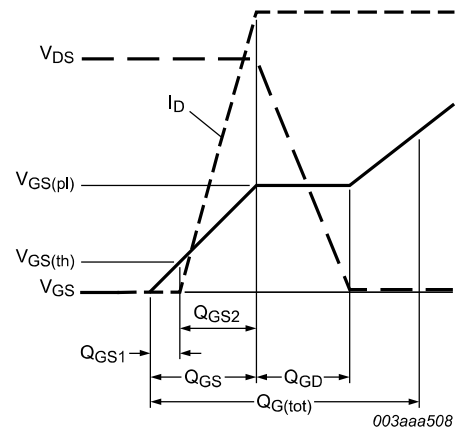
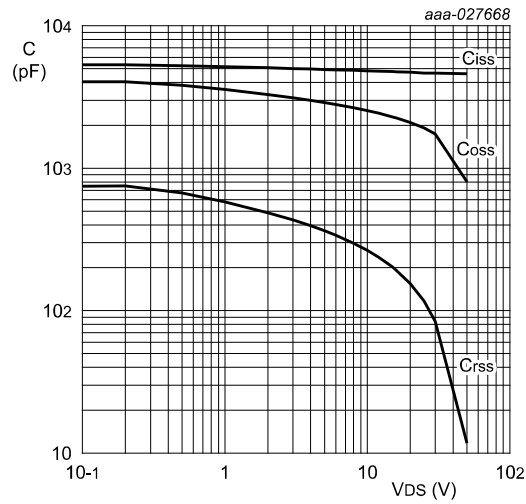
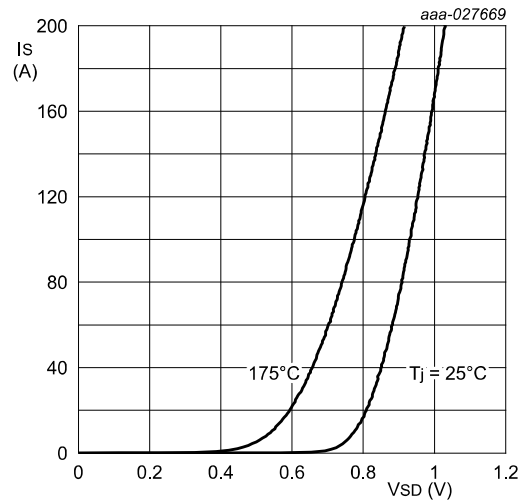


Fig. 13. Gate charge waveform definitions



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

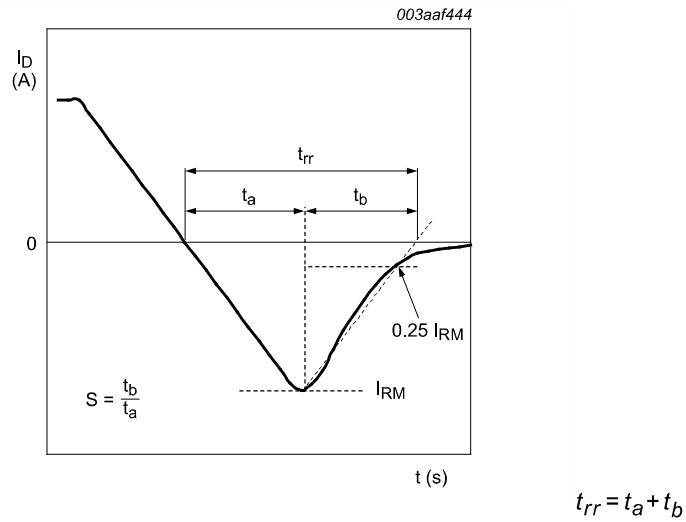


Fig. 16. Reverse recovery waveform definitions

11. Package outline

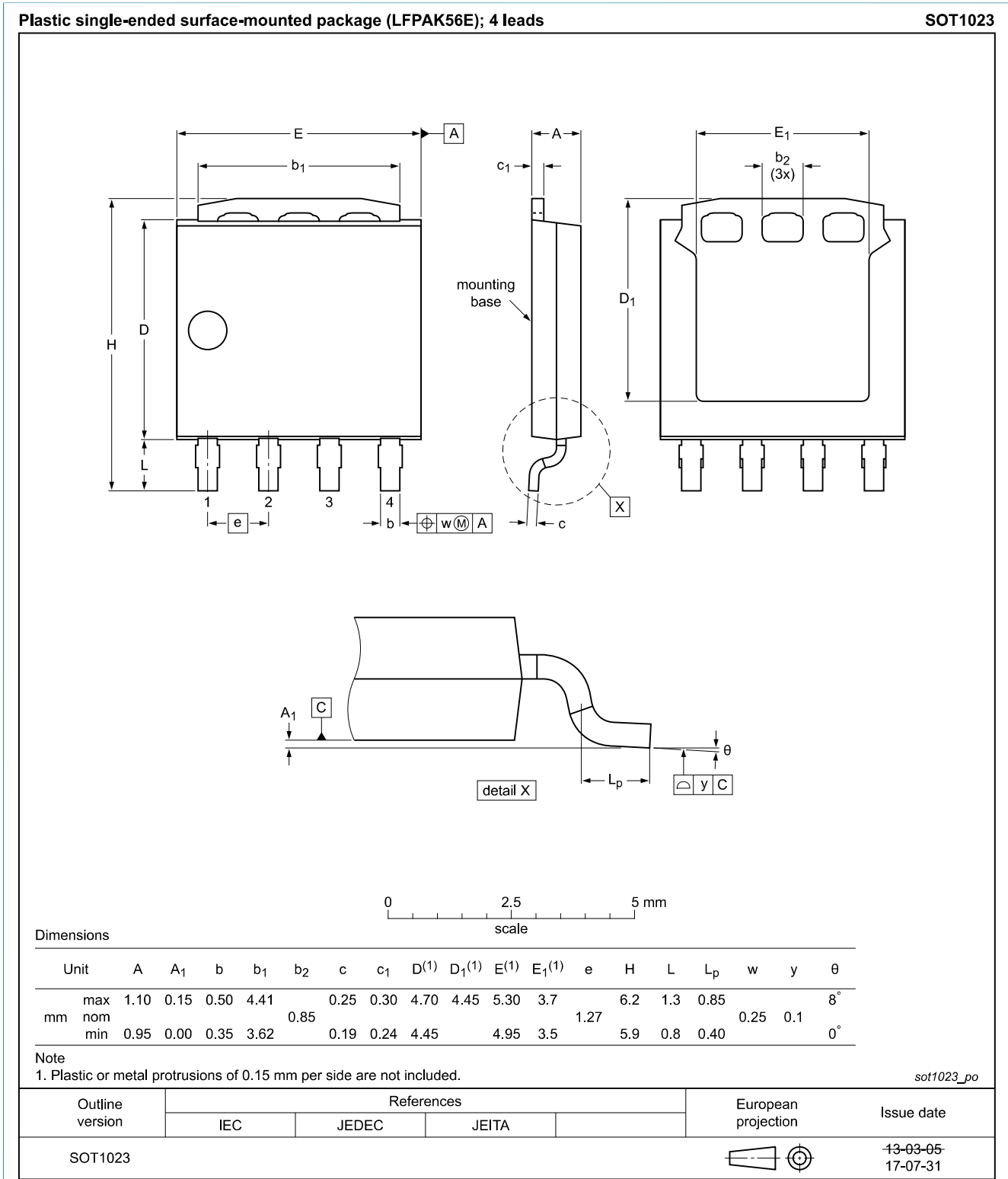


Fig. 17. Package outline LFPAK56E; Power-SO8 (SOT1023)

12. Soldering

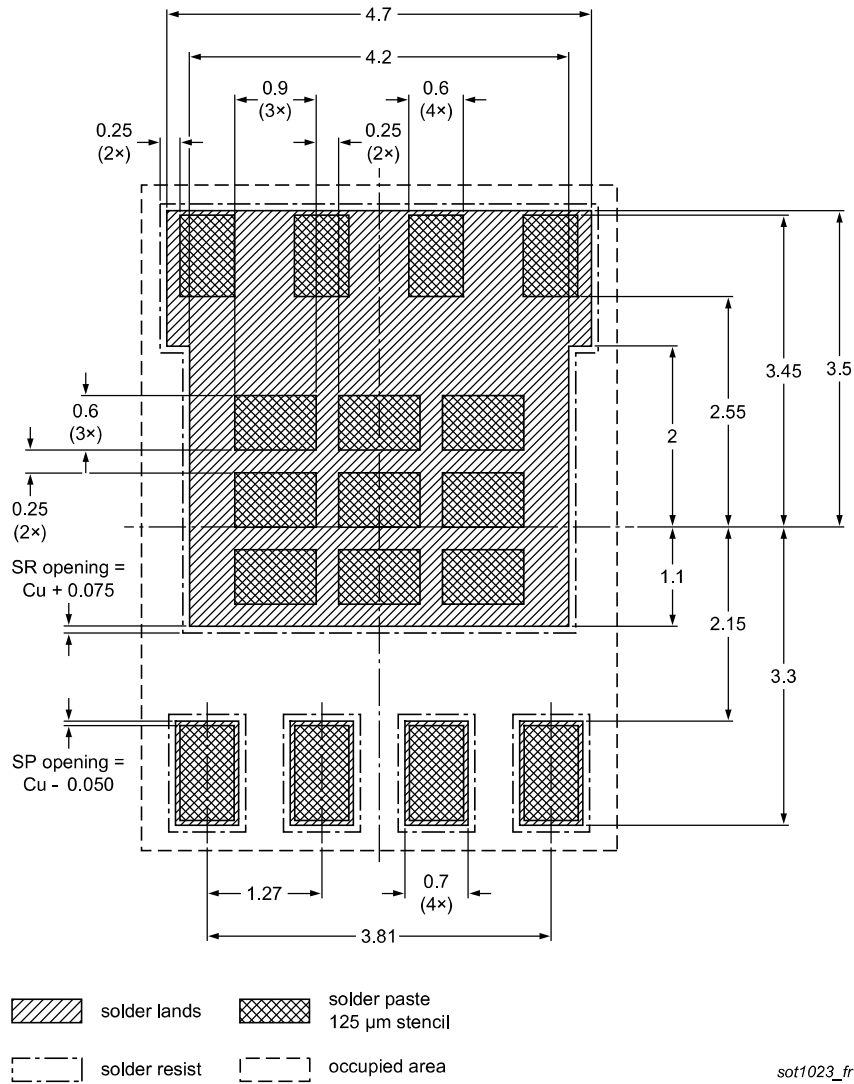


Fig. 18. Reflow soldering footprint for LFPAK56E; Power-SO8 (SOT1023)

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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14. Contents

1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Marking.....	2
8. Limiting values.....	2
9. Thermal characteristics.....	4
10. Characteristics.....	5
11. Package outline.....	10
12. Soldering.....	11
13. Legal information.....	12

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