Texas Instruments

TAS5508-5121K8EVM

Evaluation Module for the TAS5508B 8-Channel Digital Audio PWM Processor and the TAS5121 Digital Amplifier Power Output Stage

User's Guide

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 to 29.5 V and the output voltage range of 15 V to 20 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 75°C. The EVM is designed to operate properly with certain components above 75°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This manual describes the operation of the TAS5508–5121K8EVM evaluation module from Texas Instruments.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1 — Overview
- ❏ Chapter 2 — System Interfaces
- ❏ Chapter 3 — Protection

Information About Cautions and Warnings

This manual may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

The following table contains a list of data manuals that have detailed descriptions of the integrated circuits used in the design of the TAS5508−5121K8EVM. The data manuals can be obtained at the URL http://www.ti.com.

Part Number	Literature Number
TAS5508B	SLES162
TAS5121	SLES086
TLV272	SLOS351
SN74LVC1G00	SCES212
SN74LVC1G08	SCES217
SN74LVC2G08	SCES198
SN74LVC1G14	SCES218
SN74LV123A	SCLS393
SN74LVC125A	SCAS290
SN74LVC1G126A	SCES211
LM317M	SLVS297
TPS3801K33	SLVS219
TPS76733	SLVS208

Additional Documentation

TAS5508−5121K8EVM Application Report (SLEA034B)

PC Configuration Tool for TAS5508B (TAS5508 GUI ver.4.0 or later)

General Application Notes

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Chapter 1

Overview

The TAS5508−5121K8EVM PurePath Digital™ customer evaluation amplifier module demonstrates two audio integrated circuits, TAS5508B and TAS5121, from Texas Instruments (TI).

The TAS5508BPAG is a high-performance 32-bit (24-bit input) multichannel PurePath Digital pulse width modulator (PWM) based on Equibit™ technology, with a new fully symmetrical AD modulation scheme. It accepts an input sample rate from 32 kHz to 192 kHz. The device also has digital audio processing (DAP) that provides 48-bit signal processing, advanced performance, and a high level of system integration. The device has interfaces for headphone output and power supply volume control (PSVC).

The TAS5121DKD is a compact, high-power, digital amplifier power stage designed to drive a 4-Ω loudspeaker up to 100 W (10% THD+N). The TAS5121DKD contains integrated gate drivers, four matched and electrically isolated enhancement-mode N-channel power DMOS transistors, and protection/fault-reporting circuitry.

The DKD package has a PowerPAD™ on the top side for heat transfer through a heatsink. The heatsink in this design is for evaluation purpose only.

This EVM, together with a TI input-USB, is a complete 8-channel digital audio amplifier system, which includes digital input (S/PDIF), analog inputs, interface to PC, and DAP features, such as digital volume control, input and output mixers, auto mute, equalization, tone controls, loudness, dynamic range compression, and PSVC output. There are configuration options for stereo line level output, stereo headphone output, and power-stage failure protection.

This 7.1 system is designed for home-theater applications, such as A/V receivers, DVD minicomponent systems, home theater in a box (HTIB), DVD receivers, or plasma display panels (PDPs).

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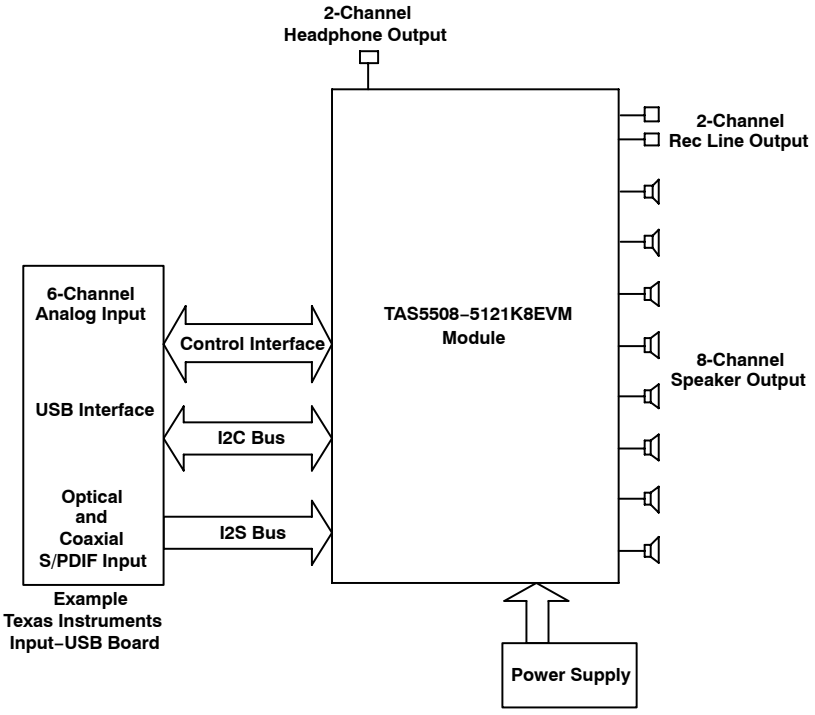
1.1 TAS5508–5121K8EVM Features

- 8-channel PurePath Digital evaluation module
- Stereo channel line output
- Stereo headphone output
- Self-contained protection system (short circuit and thermal)
- Standard I^2S and I^2C control connector for TI input board
- Double-sided plated-through PCB layout

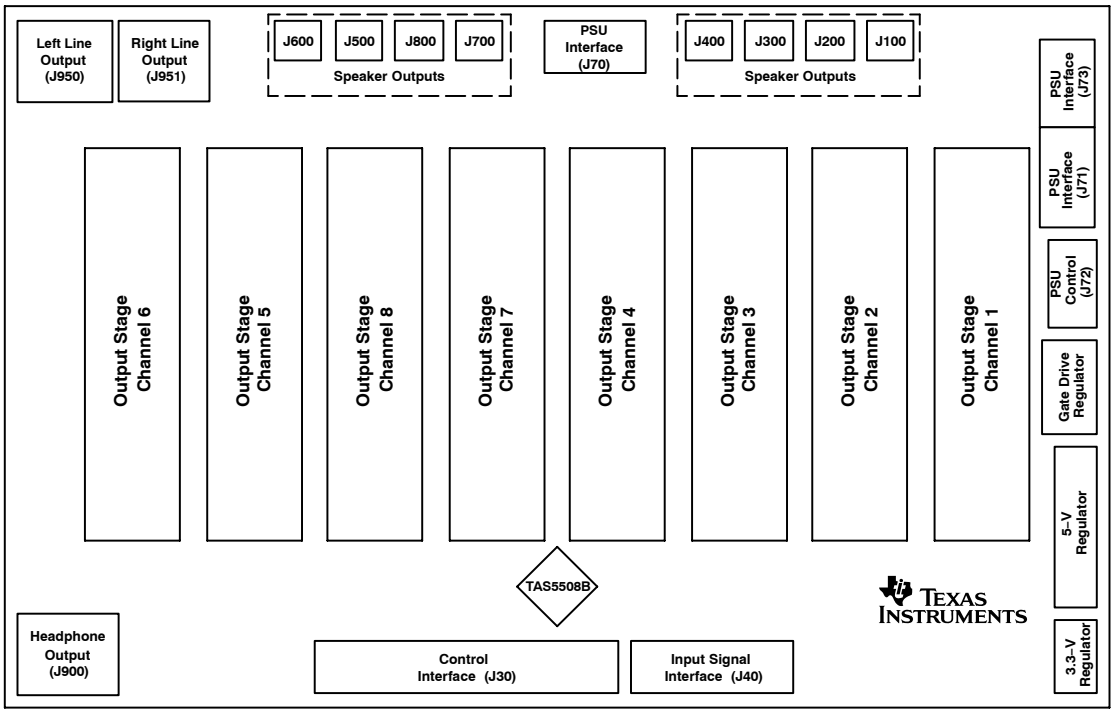
Figure 1–1. Integrated PurePath Digital ™ Amplifier System



1.2 PCB Key Map

The physical structure for the TAS5508−5121K8EVM is illustrated in Figure 1−2.

Figure 1−2. Physical Structure for TAS5508−5121K8EVM (Rough Outline)



Chapter 2

System Interfaces

This chapter describes the TAS5508–5121K8EVM board regarding power supplies and system interfaces.

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2.1 Power Supply (PSU) Interface (J70, J71, and J73)

The TAS5508−5121K8EVM module must be powered from external power supplies. High-end audio performance requires a stabilized power supply with low ripple voltage and low output impedance.

Note:

The length of the power supply cable must be minimized. Increasing length of PSU cable is equal to increasing the distortion for the amplifier at high output levels and low frequencies.

The maximum output-stage supply voltage depends of the speaker load resistance. Check the recommended maximum supply voltage in the TAS5121 data sheet (SLES086).

Table 2−1. Recommended Supply Voltages

Description	Voltage Limitations (4-Ω load)	Current Recommendations
System power supply	15 – 20 V	0.3 A
Output-stage power supply	0 – 30.5 V	6 A†

† The rated current corresponds to 2-channel full scale (80 W each), which most likely is adequate for a standard 8-channel amplifier design.

The recommended TAS5121 power-up sequence is shown in Figure 2−1. For proper TAS5121 operation, the $\overline{\text{RESET}}$ signal should be kept low during power up. $\overline{\text{RESET}}$ is pulled low during power up for 200 ms by the onboard reset generator (U73).

Figure 2−1. Recommended Power-Up Sequence

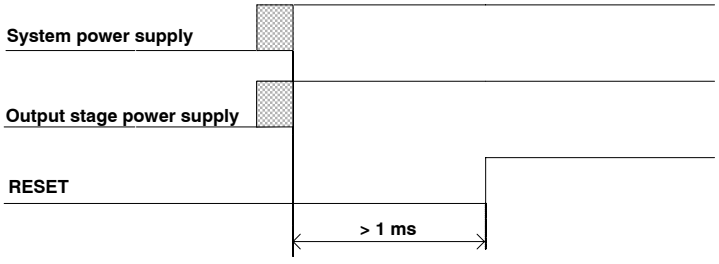
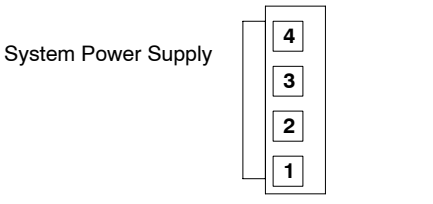


Figure 2−2. J71 and J70 Pin Numbers



(PCB connector top view)

Table 2–2. J71 Pin Description

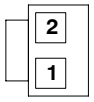
Pin No.	Net-Name at Schematics	Description
1	V-HBRIDGE	Output-stage power supply
2	–	System power supply
3	GND	Ground
4	GND	Ground

Table 2–3. J70 Pin Description

(Optional – Use to decrease of impedance to reach better performance)

Pin No.	Net-Name at Schematics	Description
1	V-HBRIDGE	Extra output-stage power supply
2	V-HBRIDGE	Extra output-stage power supply
3	GND	Extra ground
4	GND	Extra ground

Figure 2–3. J73 Pin Numbers



(PCB connector top view)

Table 2–4. J73 Pin Description

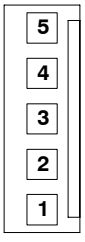
(Optional)

Pin No.	Net-Name at Schematics	Description
1	V-HBRIDGE	Extra output-stage power supply
2	V-HBRIDGE	Extra output-stage power supply

2.1.1 PSU Control Interface (J72)

This interface is used for onboard sensing of output supply voltage and for the power supply volume control (PSVC) signal.

Figure 2–4. J72 Pin Numbers



(PCB connector top view)

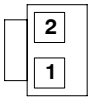
Table 2–5. J72 Pin Description

Pin No.	Net-Name at Schematics	Description
1	—	Reserved for future use
2	V-HBRIDGE	Sense of output power supply
3	GND	Ground
4	$\overline{\text{RESET}}$	System reset (bidirectional)
5	PSVC	Power-supply volume control signal

2.2 Loudspeaker Connectors (J100 . . . J800)

Both positive and negative speaker outputs are floating and may not be connected to ground (e.g., through an oscilloscope).

Figure 2–5. J100 . . . J800 Pin Numbers



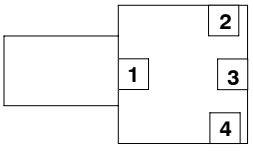
(PCB connector top view)

Table 2–6. J100 . . . J800 Pin Description

Pin No.	Net-Name at Schematics	Description
1	OUT–1	Speaker negative output
2	OUT–2	Speaker positive output

2.3 Line Out Connectors (J950 and J951)

Figure 2–6. J950 and J951 Pin Numbers



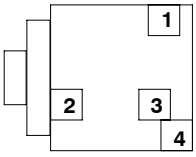
(PCB connector top view)

Table 2–7. J950 and J952 Pin Description

Pin No.	Net-Name at Schematics	Description
1	GND	Ground
2	OUT	Line out signal
3	OUT	Line out signal
4	OUT	Line out signal

2.4 Headphone Connector (J900)

Figure 2–7. J900 Pin Numbers



(PCB connector top view)

Table 2–8. J900 Pin Description

Pin No.	Net-Name at Schematics	Description
1	OUT–L	Left headphone output
2	GND	Ground
3	—	For future use
4	OUT–R	Right headphone output

2.5 Line Output Select (J50)

Figure 2–8. J50 Pin Numbers

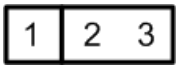


Table 2–9. J50 Pin Description

Pin No.	Description
1–2	Line outputs enabled
2–3	Line outputs disabled

2.6 Headphone Select (J32)

Figure 2–9. J32 Pin Numbers

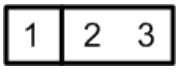


Table 2–10. J32 Pin Description

Pin No.	Description
1–2	Headphone enabled
2–3	Headphone disabled

2.7 Control Interface (J30)

This interface connects the TAS5508−5121K8EVM board to a TI input board.

Table 2−11. J30 Pin Description

Pin No.	Net-Name at Schematics	Description
1	GND	Ground
2	PSVC−MCPU	Power supply volume control from (mC) input board
3	GND	Ground
4	$\overline{\text{RESET}}$	System reset (bidirectional). Activate $\overline{\text{MUTE}}$ before $\overline{\text{RESET}}$ for quiet reset.
5	$\overline{\text{BKND−ERR}}$	Backend error (or soft reset) provides reduced click and pop reset, without resetting I^2C volume register settings.
6	$\overline{\text{MUTE}}$	Ramp volume from any setting to noiseless soft mute. Mute can also be activated by I^2C.
7	$\overline{\text{PDN}}$	Power down. The TAS5508B goes to a power-down state when activated.
8 9	RESERVED	
10	SDA	I^2C data clock
11	GND	Ground
12	SCL	I^2C bit clock
13 14	RESERVED	
15	CONF−SEL	Configuration select. Channel 5 and 6 speaker outputs active and line outputs inactive when high. Line outputs active and channel 5 and 6 speaker outputs inactive when low.
16	RESERVED	
17	GND	Ground
18 19	RESERVED	
20	$\overline{\text{SD1}}$	Shutdown error reporting for front left, front right, and center channels. Activated if the TAS5121 has high current or high temperature. See Chapter 3.
21	$\overline{\text{SD2}}$	Shutdown error reporting for rear left, rear right, surround left, surround right, and subwoofer channels. Activated if TAS5121 has high current or high temperature. See Chapter 3.
22	$\overline{\text{OTW}}$	Temperature warning. Activated if one or more TAS5121 has reached the temperature warning level.
23	RESERVED	
24	$\overline{\text{HP−SEL}}$	Headphone select. Headphone is active when low and inactive when high.
25 26	GND	Ground
27 28 29 30	RESERVED	
31 32	GND	Ground
33 34	+5V	5-V dc power supply (output)

2.8 Digital Audio Interface (J40)

The digital audio interface contains digital audio signal data (I^2S), clocks, etc. See the *TAS5508B Data Manual* (SLES162) for signal timing and details not explained in this document.

Table 2−12. J40 Pin Description

Pin No.	Net-Name at Schematics	Description
1	GND	Ground
2	MCLK	Master clock input. Low-jitter system clock for PWM generation and reclocking. Ground connection from source to the TAS5508B must be a low-impedance connection.
3	GND	Ground
4	SDIN1	I^2S data 1, channel 1 and 2
5	SDIN2	I^2S data 2, channel 3 and 4
6	SDIN3	I^2S data 3, channel 5 and 6
7	SDIN4	I^2S data 4, channel 7 and 8
8		Reserved
9		Reserved
10	GND	Ground
11	SCLK	I^2S bit clock
12	GND	Ground
13	LRCLK	I^2S left−right clock
14	GND	Ground
15		Reserved
16	GND	Ground

Chapter 3

Protection

This chapter describes the short-circuit protection and fault-reporting circuitry of the TAS5121 device.

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3.1 Short-Circuit Protection and Fault-Reporting Circuitry

The TAS5121 is a self-protecting device that provides device fault reporting (including high-temperature protection and short-circuit protection). The TAS5121 is configured in back-end auto-recovery mode and, therefore, resets automatically after all errors (M1, M2, and M3 is set low). This means that the device restarts itself after an error occasion and reports shortly through $\overline{SD1}$ and $\overline{SD2}$ error signals.

The shutdown report signals are separated into two wires, $\overline{SD1}$ and $\overline{SD2}$. $\overline{SD1}$ covers the primary information channels (front channels and center), where the $\overline{SD2}$ covers the secondary information channels (rear channels, surround/line out channels, and subwoofer). Therefore, a microprocessor can react differently on errors depending on primary or secondary channels faults, e.g., lowering the output level or shutting down the secondary channels on continues error reporting from one of those, where the primary channels continue.

3.2 Device Fault Reporting

The $\overline{\text{OTW}}$ and $\overline{\text{SD}}$ outputs from the TAS5121 indicate fault conditions. See the TAS5121 data sheet (SLES086) for a description of these pins.

The temperature warning signals at the TAS5508−5121K8EVM board are wired-OR to one temperature warning signal [$\overline{\text{OTW}}$ − pin 22 in control interface connector (J30)].

Shutdown signals are wired-OR into two shutdown signals [$\overline{\text{SD1}}$ and $\overline{\text{SD2}}$ − pin 20 and pin 21 in control interface connector (J30)]. See Table 3−1 for channel allocation.

Table 3−1. Channel Allocation

Description	Terminal	Shutdown Signal
Front left	J100	$\overline{\text{SD1}}$
Front right	J200	$\overline{\text{SD1}}$
Rear left	J300	$\overline{\text{SD2}}$
Rear right	J400	$\overline{\text{SD2}}$
Surround left (or line out left)	J500	$\overline{\text{SD2}}$
Surround right (or line out right)	J600	$\overline{\text{SD2}}$
Center	J700	$\overline{\text{SD1}}$
Subwoofer	J800	$\overline{\text{SD2}}$

The shutdown signals, together with the temperature warning signal, give chip state information as described in Table 3−2. Device fault reporting outputs are open-drain outputs.

Table 3−2. TAS5121 Warning/Error Signal Decoding

$\overline{\text{OTW}}$	$\overline{\text{SDx}}$	Device Condition
0	0	High-temperature error and/or high-current error
0	1	High-temperature warning
1	0	Undervoltage lockout or high-current error
1	1	Normal operation, no errors/warnings