

NTD4N60

Preferred Device

Advance Information

Power MOSFET 4 Amps, 600 Volts N-Channel DPAK

Designed for high voltage, high speed switching applications in power supplies, converters, power motor controls and bridge circuits.

Features

- Higher Current Rating
- Lower $R_{DS(on)}$
- Lower Capacitances
- Lower Total Gate Charge
- Tighter V_{SD} Specifications
- Avalanche Energy Specified
- Industry Standard DPAK Surface Mount Package

Typical Applications

- Switch Mode Power Supplies
- PWM Motor Controls
- Converters
- Bridge Circuits

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	600	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0\text{ M}\Omega$)	V_{DGR}	600	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
- Continuous	V_{GS}	± 20	
- Non-Repetitive ($t_p \leq 10\text{ ms}$)	V_{GSM}	± 40	
Drain - Continuous	I_D	4.0	Adc
- Continuous @ 100°C	I_D	3.0	
- Single Pulse ($t_p \leq 10\text{ }\mu\text{s}$)	I_{DM}	14	
Total Power Dissipation	P_D	96	Watts
Derate above 25°C		0.77	W/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$		1.75	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Single Drain-to-Source Avalanche Energy - Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 100\text{ V}$, $V_{GS} = 10\text{ Vdc}$, $I_L = 4\text{ A}$, $L = 10\text{ mH}$, $R_G = 25\text{ }\Omega$)	E_{AS}	80	mJ
Thermal Resistance			$^\circ\text{C/W}$
- Junction-to-Case	$R_{\theta JC}$	1.30	
- Junction-to-Ambient	$R_{\theta JA}$	100	
- Junction-to-Ambient (Note 1.)	$R_{\theta JA}$	71.4	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

1. When surface mounted to an FR4 board using the minimum recommended pad size.

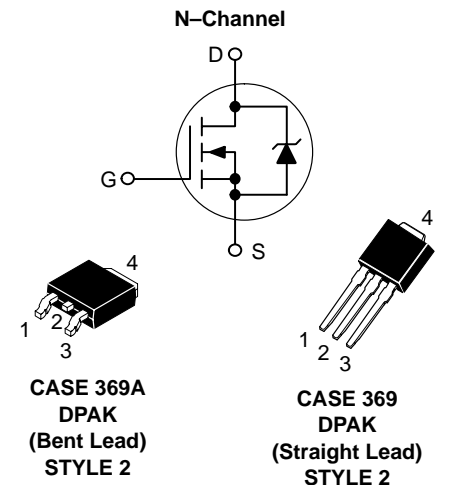
This document contains information on a new product. Specifications and information herein are subject to change without notice.



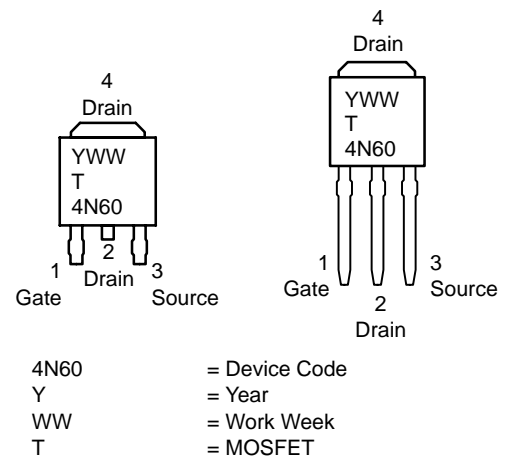
ON Semiconductor™

<http://onsemi.com>

4 AMPERES
600 VOLTS
 $R_{DS(on)} = 2400\text{ m}\Omega$



MARKING DIAGRAMS & PIN ASSIGNMENTS



ORDERING INFORMATION

Device	Package	Shipping
NTD4N60	DPAK	75 Units/Rail
NTD4N60-1	DPAK Straight Lead	75 Units/Rail
NTD4N60T4	DPAK	2500 Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

NTD4N60

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 0.25 mAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	600 –	– 700	– –	Vdc mV/°C
Zero Gate Voltage Collector Current (V _{DS} = 600 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 600 Vdc, V _{GS} = 0 Vdc, T _J = 125°C)	I _{DSS}	– –	– –	10 100	μAdc
Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0)	I _{GSS(f)} I _{GSS(r)}	– –	– –	100 100	nAdc

ON CHARACTERISTICS (Note 2.)

Gate Threshold Voltage I _D = 0.25 mA, V _{DS} = V _{GS} Temperature Coefficient (Negative)	V _{GS(th)}	2.0 –	2.7 6.0	4.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 2 Adc)	R _{DS(on)}	–	2100	2400	mOhm
Drain-to-Source On-Voltage (V _{GS} = 10 Vdc, I _D = 4 Adc) (V _{GS} = 10 Vdc, I _D = 2 Adc, T _J = 125°C)	V _{DS(on)}	– –	– –	11.5 10.5	Vdc
Forward Transconductance (V _{DS} = 15 Vdc, I _D = 2 Adc)	g _{FS}	0.7	3.8	–	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	–	540	760	pF
Output Capacitance		C _{oss}	–	125	180	
Transfer Capacitance		C _{rss}	–	8.0	20	

SWITCHING CHARACTERISTICS (Note 3.)

Turn-On Delay Time	(V _{DD} = 300 Vdc, I _D = 4 Adc, V _{GS} = 10 Vdc, R _G = 9.1 Ω)	t _{d(on)}	–	12	20	ns
Rise Time		t _r	–	7.0	10	
Turn-Off Delay Time		t _{d(off)}	–	19	40	
Fall Time		t _f	–	10	20	
Gate Charge	(V _{DS} = 480 Vdc, I _D = 4 Adc, V _{GS} = 10 Vdc)	Q _T	–	5.0	10	nC
		Q ₁	–	2.7	–	
		Q ₂	–	2.0	–	
		Q ₃	–	6.0	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

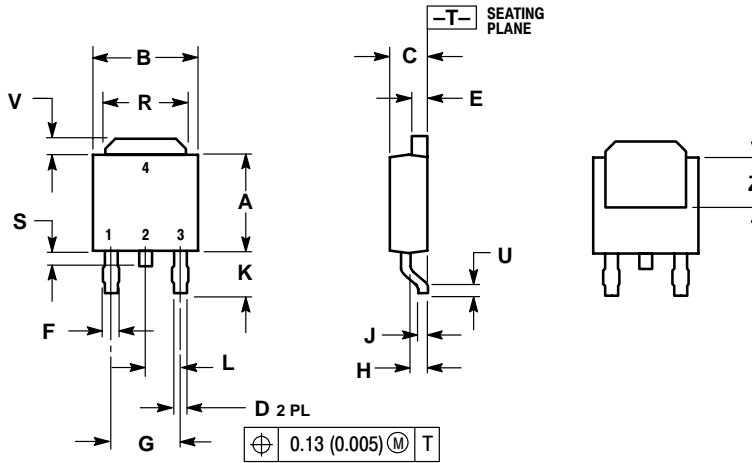
Forward On-Voltage (Note 2.)	(I _S = 4 Adc, V _{GS} = 0 Vdc) (I _S = 4 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	– –	0.86 0.75	1.0 –	Vdc
Reverse Recovery Time	(I _S = 4 Adc, V _{GS} = 0 Vdc, di _S /dt = 100 A/μs)	t _{rr}	–	655	–	ns
		t _a	–	103	–	
		t _b	–	552	–	
Reverse Recovery Stored Charge		Q _R	–	1.9	–	μC

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperature.

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PACKAGE DIMENSIONS

DPAK
CASE 369A-13
ISSUE AA



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

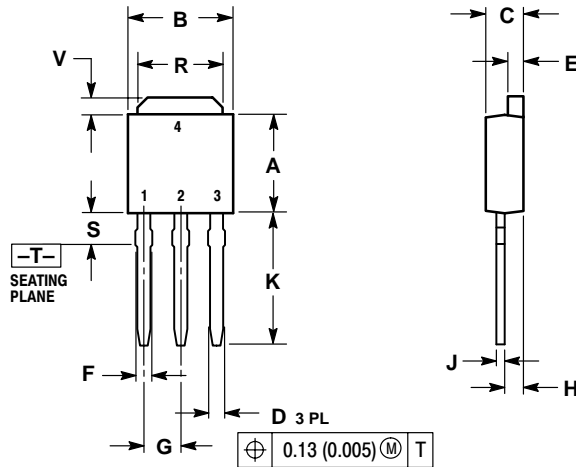
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	----	0.51	----
V	0.030	0.050	0.77	1.27
Z	0.138	----	3.51	----

- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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PACKAGE DIMENSIONS

DPAK CASE 369-07 ISSUE M




NOTES:

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DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
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G	0.090 BSC		2.29 BSC	
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K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

STYLE 2:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

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