

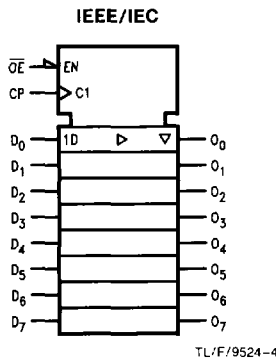
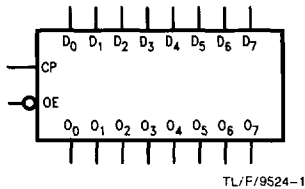
54F/74F374
Octal D-Type Flip-Flop with TRI-STATE® Outputs
General Description

The 'F374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops.

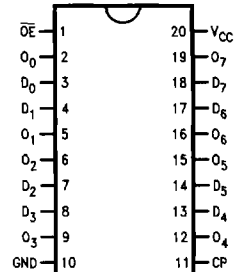
Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications

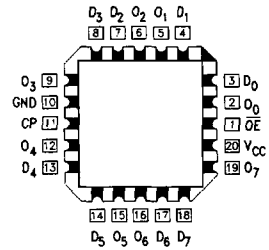
Ordering Code: See Section 5

Logic Symbols

Connection Diagrams

**Pin Assignment
for DIP, SOIC and Flatpak**



**Pin Assignment
for LCC and PCC**





Unit Loading/Fan Out: See Section 2 for U.L. definitions


Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0 - D_7	Data Inputs	1.0/1.0	20 μ A/ -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/ -0.6 mA
\overline{OE}	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
O_0 - O_7	TRI-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

Functional Description

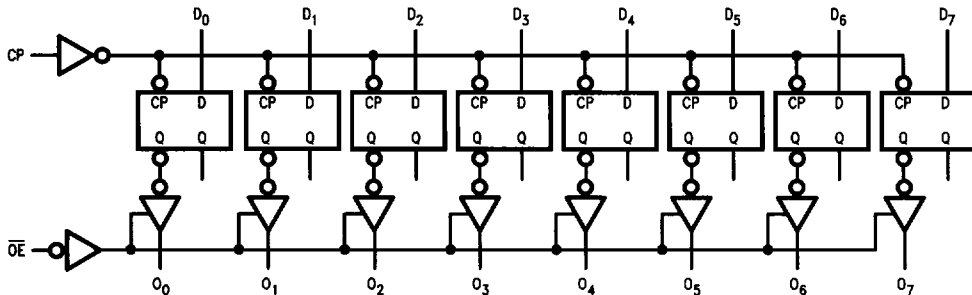
The 'F374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Truth Table

Inputs			Internal Register	Output
D_n	CP	\overline{OE}		O_n
H		L	H	H
L		L	L	L
X	X	H	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 = LOW-to-HIGH Clock Transition

Logic Diagram



TL/F/9524-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} 74F 5% V _{CC}	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}		0.5 0.5	V	Min	I _{OL} = 20 mA I _{OL} = 24 mA
I _{IH}	Input HIGH Current			20	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			100	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			-50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current		-60	-150	mA	Max	V _{OUT} = 0V
I _{CEX}	Output HIGH Leakage Current			250	μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = V _{CC}
I _{CCZ}	Power Supply Current		55	86	mA	Max	V _O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig No
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Clock Frequency	100	140		60		70	MHz	2-1	
t _{PLH}	Propagation Delay CP to O _n	4.0	6.5	8.5	4.0	10.5	4.0	10.0	ns	2-3
t _{PHL}		4.0	6.5	8.5	4.0	11.0	4.0	10.0		
t _{pZH}	Output Enable Time	2.0	9.0	11.5	2.0	14.0	2.0	12.5	ns	2-5
t _{pZL}		2.0	5.8	7.5	2.0	10.0	2.0	8.5		
t _{PHZ}	Output Disable Time	2.0	5.3	7.0	2.0	8.0	2.0	8.0	ns	2-5
t _{PLZ}		1.5	4.3	5.5	1.5	7.5	1.5	6.5		

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig No
		T _A = +25°C V _{CC} = +5.0V		T _A , V _{CC} = Mil		T _A , V _{CC} = Com			
		Min	Max	Min	Max	Min	Max		
t _s (H)	Setup Time, HIGH or LOW D _n to CP	2.0		2.5		2.0		ns	2-6
t _s (L)		2.0		2.0		2.0			
t _h (H)	Hold Time, HIGH or LOW D _n to CP	2.0		2.0		2.0		ns	2-4
t _h (L)		2.0		2.5		2.0			
t _w (H)	CP Pulse Width	7.0		7.0		7.0		ns	2-4
t _w (L)	HIGH or LOW	6.0		6.0		7.0			