Programmable Timing Control Hub™ for P4™ processor

Recommended Application:

ATI chipset, P4 system, Banias system

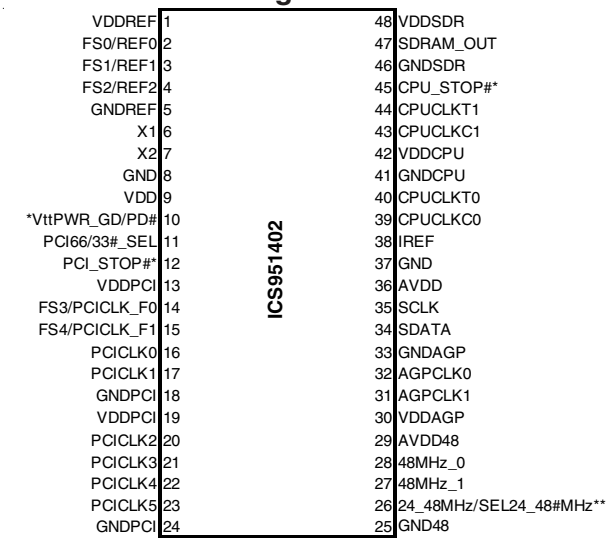
Output Features:

- 2 - Pairs of differential CPUCLKs (differential current mode)
- 1 - SDRAM @ 3.3V
- 8 - PCI @3.3V (selectable 33/66 MHz) (2 free-running)
- 2 - AGP @ 3.3V
- 2- 48MHz, @3.3V fixed.
- 1- 24/48MHz, @3.3V selectable by I^2C (Default is 24MHz)
- 3- REF @3.3V, 14.318MHz.

Features/Benefits:

- Support for Intel Banias power management features
- Programmable output frequency, divider ratios, output rise/ falltime, output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I^2C Index read/write and block read/write operations.
- Supports spread spectrum for EMI reduction; default is spread spectrum ON.

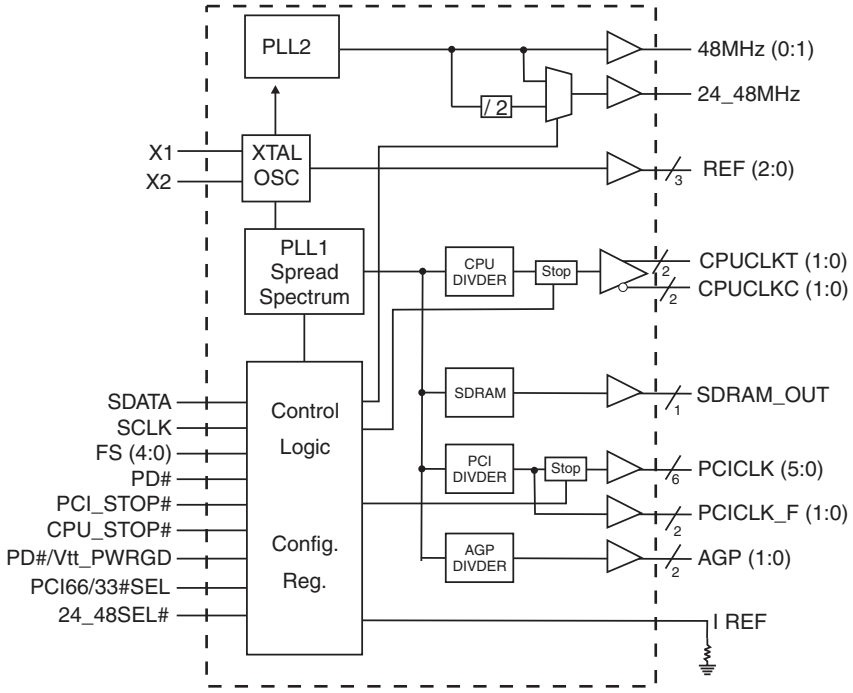
Pin Configuration



48-Pin TSSOP & SSOP

* These inputs have a 120K pull up to VDD.
** These inputs have a 120K pull down to GND.

Block Diagram



Skew Requirements

PCI-PCI	<±350ps
AGP-AGP	<±350ps
CPU-AGP	<±500ps
CPU-PCI	<±500ps
AGP-PCI AGP leading	<±1ns
CPU-SDRAM	<±1ns

Power Groups

VDDCPU = CPU
VDDPCI = PCICLK_F, PCICLK
VDDSD = SDRAM
AVDD48 = 48MHz, 24MHz, fixed PLL
AVDD = Analog Core PLL
VDDAGP= AGP
VDDREF = Xtal, REF

Pin Description

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
2	FS0/REF0	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
3	FS1/REF1	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
4	FS2/REF2	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
5	GNDREF	PWR	Ground pin for the REF outputs.
6	X1	IN	Crystal input, Nominally 14.318MHz.
7	X2	OUT	Crystal output, Nominally 14.318MHz
8	GND	PWR	Ground pin.
9	VDD	PWR	Power supply, nominal 3.3V
10	*VttPWR_GD/PD#	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active high input. / Asynchronous active low input pin used to power down the device into a low power state.
11	PCI66/33#_SEL	IN	Selects all PCI clock frequencies to be 33Mhz or 66Mhz. 0 = 33Mhz , 1 = 66Mhz
12	PCI_STOP#*	IN	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low
13	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
14	FS3/PCICLK_F0	I/O	Frequency select latch input pin / 3.3V PCI free running clock output.
15	FS4/PCICLK_F1	I/O	Frequency select latch input pin / 3.3V PCI free running clock output.
16	PCICLK0	OUT	PCI clock output.
17	PCICLK1	OUT	PCI clock output.
18	GNDPCI	PWR	Ground pin for the PCI outputs
19	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
20	PCICLK2	OUT	PCI clock output.
21	PCICLK3	OUT	PCI clock output.
22	PCICLK4	OUT	PCI clock output.
23	PCICLK5	OUT	PCI clock output.
24	GNDPCI	PWR	Ground pin for the PCI outputs
25	GND48	PWR	Ground pin for the 48MHz outputs
26	24_48MHz/SEL24_48#MHz**	I/O	24/48MHz clock output / Latched select input for 24/48MHz output. 0=48MHz, 1 = 24MHz.
27	48MHz_1	OUT	48MHz clock output.
28	48MHz_0	OUT	48MHz clock output.
29	AVDD48	PWR	Analog power for 48MHz outputs and fixed PLL core, nominal 3.3V
30	VDDAGP	PWR	Power supply for AGP clocks, nominal 3.3V
31	AGPCLK1	OUT	AGP clock output
32	AGPCLK0	OUT	AGP clock output
33	GNDAGP	PWR	Ground pin for the AGP outputs
34	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
35	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
36	AVDD	PWR	3.3V Analog Power pin for Core PLL
37	GND	PWR	Ground pin.
38	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
39	CPUCLKC0	OUT	Complementary clock of differential pair CPU outputs. This clock is 180 degrees out of phase with the SDRAM clock.
40	CPUCLKT0	OUT	True clock of differential pair CPU outputs. This clock is in phase with the SDRAM clock
41	GNDCPU	PWR	Ground pin for the CPU outputs
42	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
43	CPUCLKC1	OUT	Complementary clock of differential pair CPU outputs. This clock is 180 degrees out of phase with the SDRAM clock.
44	CPUCLKT1	OUT	True clock of differential pair CPU outputs. This clock is in phase with the SDRAM clock
45	CPU_STOP#*	IN	Stops all CPUCLK besides the free running clocks
46	GNDSDR	PWR	Ground pin for the SDRAM outputs.
47	SDRAM_OUT	OUT	SDRAM seed clock output for external buffer
48	VDDSDR	PWR	Supply for SDRAM clocks, nominal 3.3V.

Table 1: Clock Power Management Truth Table

Byte 6 Bit 6	Byte 6 Bit 7	PD#	CPU_ STOP	Stoppable CPU (Not free-run)	Non-stop CPU (Free-run)	Note
0	0	0	0	IREF x 2	IREF x 2	Non Tri-state Mode
0	0	0	1	IREF x 2	IREF x 2	
0	0	1	0	IREF x 6	RUN	
0	0	1	1	RUN	RUN	
0	1	0	0	Hi Z	IREF x 2	CPU_stop# Tri-state Mode
0	1	0	1	Hi Z	IREF x 2	
0	1	1	0	Hi Z	RUN	
0	1	1	1	RUN	RUN	
1	0	0	0	Hi Z	Hi Z	PD# & Tri-state Mode
1	0	0	1	Hi Z	Hi Z	
1	0	1	0	IREFx6	RUN	
1	0	1	1	RUN	RUN	
1	1	0	0	Hi Z	Hi Z	PD# & CPU_stop# Tri-state Mode
1	1	0	1	Hi Z	Hi Z	
1	1	1	0	HI Z	RUN	
1	1	1	1	RUN	RUN	

General I²C serial interface information for the ICS951402

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N	X Byte	
		ACK
O		
O		O
O		O
		O
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address D2(H)			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address D3(H)			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
	X Byte		Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

*See notes on the following page.

0660—05/05/05

Serial Configuration Command Bitmap

FS4	FS3	FS2	FS1	FS0	CPU MHz	SDRAM MHz	3V66 MHz	PCI MHz	REF MHz	USB/DOT MHz	With Spread Enabled...
0	0	0	0	0	100.00	100.00	66.67	33.33	14.318	48.008	SpreaD OFF OR Center spread +/-0.3%
0	0	0	0	1	133.34	133.34	66.67	33.33	14.318	48.008	
0	0	0	1	0	200.01	200.01	66.67	33.33	14.318	48.008	
0	0	0	1	1	166.65	166.65	66.66	33.33	14.318	48.008	
0	0	1	0	0	100.00	133.34	66.67	33.33	14.318	48.008	
0	0	1	0	1	133.34	100.00	66.67	33.33	14.318	48.008	
0	0	1	1	0	133.16	166.45	66.58	33.29	14.318	48.008	
0	0	1	1	1	166.45	133.16	66.58	33.29	14.318	48.008	
0	1	0	0	0	105.00	105.00	70.00	35.00	14.318	48.008	
0	1	0	0	1	140.00	140.00	70.00	35.00	14.318	48.008	
0	1	0	1	0	66.67	66.67	66.67	33.33	14.318	48.008	
0	1	0	1	1	175.00	175.00	70.00	35.00	14.318	48.008	
0	1	1	0	0	109.99	109.99	73.33	36.66	14.318	48.008	
0	1	1	0	1	146.65	146.65	73.33	36.66	14.318	48.008	
0	1	1	1	0	210.00	210.00	70.00	35.00	14.318	48.008	
0	1	1	1	1	183.27	183.27	73.31	36.65	14.318	48.008	
1	0	0	0	0	99.51	99.51	66.34	33.17	14.318	48.008	Down Spread -0.6%
1	0	0	0	1	132.68	132.68	66.34	33.17	14.318	48.008	
1	0	0	1	0	199.02	199.02	66.34	33.17	14.318	48.008	
1	0	0	1	1	165.85	165.85	66.34	33.17	14.318	48.008	
1	0	1	0	0	99.51	132.68	66.34	33.17	14.318	48.008	
1	0	1	0	1	132.68	99.51	66.34	33.17	14.318	48.008	
1	0	1	1	0	132.59	165.73	66.29	33.15	14.318	48.008	
1	0	1	1	1	165.73	132.59	66.29	33.15	14.318	48.008	
1	1	0	0	0	99.39	99.39	66.26	33.13	14.318	48.008	Down Spread -0.8%
1	1	0	0	1	132.51	132.51	66.26	33.13	14.318	48.008	
1	1	0	1	0	198.77	198.77	66.26	33.13	14.318	48.008	
1	1	0	1	1	165.64	165.64	66.25	33.13	14.318	48.008	
1	1	1	0	0	99.39	132.51	66.26	33.13	14.318	48.008	
1	1	1	0	1	132.51	99.39	66.26	33.13	14.318	48.008	
1	1	1	1	0	132.36	165.45	66.18	33.09	14.318	48.008	
1	1	1	1	1	165.45	132.36	66.18	33.09	14.318	48.008	

I²C Table: Reserved Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved	Reserved	RW	-	-	1
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved	Reserved	RW	-	-	1
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	Reserved	Reserved	RW	-	-	1
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

I²C Table: Reserved Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved	Reserved	RW	-	-	1
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved	Reserved	RW	-	-	1
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	Reserved	Reserved	RW	-	-	1
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

I²C Table: Reserved Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved	Reserved	RW	-	-	1
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved	Reserved	RW	-	-	1
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	Reserved	Reserved	RW	-	-	1
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

I²C Table: Reserved Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved	Reserved	RW	-	-	1
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved	Reserved	RW	-	-	1
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	Reserved	Reserved	RW	-	-	1
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

I²C Table: Functionality and Frequency Select Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	FS3	Freq Select Bit 7	RW	See Frequency Table		0
Bit 6	-	FS2	Freq Select Bit 6	RW			0
Bit 5	-	FS1	Freq Select Bit 5	RW			0
Bit 4	-	FS0	Freq Select Bit 4	RW			0
Bit 3	-	FS Source	Frequency H/W or IIC Select	RW	Latch Input	IIC	0
Bit 2	-	FS4	Freq Select Bit 2	RW	See Frequency Table		0
Bit 1	-	SS_EN	SPREAD Enable	RW	OFF	ON	1
Bit 0	-	All Outputs	Output Control	RW	Normal	Tri-state	0

Note: If Byte4 bit1 = 0 then FS4=0

I²C Table: Output Control and Read Back Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	31	AGP1	Output Control	RW	Disable	Enable	1
Bit 6	32	AGP0	Output Control	RW	Disable	Enable	1
Bit 5	26	24_48#SEL	24 or 48 Select	RW	48MHz	24MHz	X
Bit 4	-	FS4RB	FS4 Read back	R	-	-	X
Bit 3	-	FS3RB	FS3 Read back	R	-	-	X
Bit 2	-	FS2RB	FS2 Read back	R	-	-	X
Bit 1	-	FS1RB	FS1 Read back	R	-	-	X
Bit 0	-	FS0RB	FS0 Read back	R	-	-	X

I²C Table: Output Control Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	CPU_STOP#	CPU Stop Status	RW	See Table 1: Truth Table on page 3		1
Bit 6	-	PD#	PD# Status	RW			1
Bit 5	-	PCI_F0	Free-run Control	RW	Free	Not free	0
Bit 4	-	PCI_F1	Free-run Control	RW	Free	Not free	0
Bit 3	-	CPUT/C_0	Free-run Control	RW	Free	Not free	1
Bit 2	-	CPUT/C_1	Free-run Control	RW	Free	Not free	1
Bit 1	40,39	CPUT/C_0	Output Control	RW	Disable	Enable	1
Bit 0	44,43	CPUT/C_1	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	15	PCICLK_F1	Output Control	RW	Disable	Enable	1
Bit 6	14	PCICLK_F0	Output Control	RW	Disable	Enable	1
Bit 5	23	PCICLK5	Output Control	RW	Disable	Enable	1
Bit 4	22	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 3	21	PCICLK3	Output Control	RW	Disable	Enable	1
Bit 2	20	PCICLK2	Output Control	RW	Disable	Enable	1
Bit 1	17	PCICLK1	Output Control	RW	Disable	Enable	1
Bit 0	16	PCICLK0	Output Control	RW	Disable	Enable	1

I²C Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	1
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

I²C Table: Watchdog Timer Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WD7	These bits represent X*293ms the watchdog timer will wait before it goes to alarm mode. Default is 16 X 293ms =4.688 seconds	RW	-	-	0
Bit 6	-	WD6		RW	-	-	0
Bit 5	-	WD5		RW	-	-	0
Bit 4	-	WD4		RW	-	-	1
Bit 3	-	WD3		RW	-	-	0
Bit 2	-	WD2		RW	-	-	0
Bit 1	-	WD1		RW	-	-	0
Bit 0	-	WD0		RW	-	-	0

I²C Table: WD Timer Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/NEN	M/N Programming Enable	RW	Latched Inputs	IIC Prog. B (11:17)	0
Bit 6	-	WDEN	Watchdog Enable	RW	Disable	Enable	0
Bit 5	-	WDStatus	WD Status Control	RW	OFF	ON	0
Bit 4	-	WD SF4	Writing to these bit will configure the safe frequency as Byte 0 Bit (6:0)	RW	-	-	1
Bit 3	-	WD SF3		RW	-	-	0
Bit 2	-	WD SF2		RW	-	-	0
Bit 1	-	WD SF1		RW	-	-	0
Bit 0	-	WD SF0		RW	-	-	0

Note: If Byte4 bit1 = 0 then FS4=0

I²C Table: VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Bit 8	RW	-	-	X
Bit 6	-	M Div6	The decimal representation of M Div (6:0) is equal to reference divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
Bit 5	-	M Div5		RW	-	-	X
Bit 4	-	M Div4		RW	-	-	X
Bit 3	-	M Div3		RW	-	-	X
Bit 2	-	M Div2		RW	-	-	X
Bit 1	-	M Div1		RW	-	-	X
Bit 0	-	M Div0		RW	-	-	X

I²C Table: VCO Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	The decimal representation of N Div (8:0) is equal to VCO divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
Bit 6	-	N Div6		RW	-	-	X
Bit 5	-	N Div5		RW	-	-	X
Bit 4	-	N Div4		RW	-	-	X
Bit 3	-	N Div3		RW	-	-	X
Bit 2	-	N Div2		RW	-	-	X
Bit 1	-	N Div1		RW	-	-	X
Bit 0	-	N Div0		RW	-	-	X

I²C Table: Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	These Spread Spectrum bits will program the spread percentage. It is recommended to use ICS Spread % table for spread programming.	RW	-	-	X
Bit 6	-	SSP6		RW	-	-	X
Bit 5	-	SSP5		RW	-	-	X
Bit 4	-	SSP4		RW	-	-	X
Bit 3	-	SSP3		RW	-	-	X
Bit 2	-	SSP2		RW	-	-	X
Bit 1	-	SSP1		RW	-	-	X
Bit 0	-	SSP0		RW	-	-	X

I²C Table: Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	X
Bit 6	-	Reserved	Reserved	R	-	-	X
Bit 5	-	Reserved	Reserved	R	-	-	X
Bit 4	-	SSP12	It is recommended to use ICS Spread % table for spread programming.	RW	-	-	X
Bit 3	-	SSP11		RW	-	-	X
Bit 2	-	SSP10		RW	-	-	X
Bit 1	-	SSP9		RW	-	-	X
Bit 0	-	SSP8		RW	-	-	X

I²C Table: Output Divider Control Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SD Div3	SDRAM divider ratio can be configured via these 4 bits individually.	RW	See Table 2: Divider Ratio Combination Table		X
Bit 6	-	SD Div2		RW			X
Bit 5	-	SD Div1		RW			X
Bit 4	-	SD Div0		RW			X
Bit 3	-	CPU Div3	CPU divider ratio can be configured via these 4 bits individually.	RW	See Table 2: Divider Ratio Combination Table		X
Bit 2	-	CPU Div2		RW			X
Bit 1	-	CPU Div1		RW			X
Bit 0	-	CPU Div0		RW			X

Table 2: CPU, SDRAM, AGP and PCI66 Divider Ratio Combination Table

	Divider (3:2)								
Divider (1:0)	Bit	00		01		10		11	MSB
			1		2		4		8
	00	0000	2	0100	4	1000	8	1100	16
	01	0001	3	0101	6	1001	12	1101	24
	10	0010	5	0110	10	1010	20	1110	40
	11	0011	7	0111	14	1011	28	1111	56
	LSB	Address	Div	Address	Div	Address	Div	Address	Div

Table 3: PCI33 Divider Ratio Combination Table

	Divider (3:2)								
Divider (1:0)	Bit	00		01		10		11	MSB
			1		2		4		8
	00	0000	4	0100	8	1000	16	1100	32
	01	0001	3	0101	6	1001	12	1101	24
	10	0010	5	0110	10	1010	20	1110	40
	11	0011	7	0111	14	1011	28	1111	56
	LSB	Address	Div	Address	Div	Address	Div	Address	Div

I²C Table: Output Divider Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	AGP Div3	AGP divider ratio can be configured via these 4 bits individually	RW	See Table 2: Divider Ratio Combination Table		X
Bit 6	-	AGP Div2		RW			X
Bit 5	-	AGP Div1		RW			X
Bit 4	-	AGP Div0		RW			X
Bit 3	-	Reserved	Reserved	RW	-	-	X
Bit 2	-	Reserved	Reserved	RW	-	-	X
Bit 1	-	Reserved	Reserved	RW	-	-	X
Bit 0	-	Reserved	Reserved	RW	-	-	X

I²C Table: Output Divider Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	AGPINV	AGP Phase Invert	RW	Default	Inverse	X
Bit 6	-	Reserved	Reserved	RW	-	-	X
Bit 5	-	SDINV	SDRAM Phase Invert	RW	Default	Inverse	X
Bit 4	-	CPUINV	CPU Phase Invert	RW	Default	Inverse	X
Bit 3	-	PCIDiv3	PCI divider ratio can be configured via these 4 bits individually	RW	See Table 2 & 3: Divider Ratio Combination Table		X
Bit 2	-	PCIDiv3		RW			X
Bit 1	-	PCIDiv3		RW			X
Bit 0	-	PCIDiv3		RW			X

I²C Table: Group Skew Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	CPUSkw3	CPUT Skew Control	RW	See 2-bit Skew Control at table 4		1
Bit 6	-	CPUSkw2		RW			0
Bit 5	-	SDSkw3	SDRAM Skew Control	RW	See 2-bit Skew Control at table 4		0
Bit 4	-	SDSkw2		RW			1
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	Reserved	Reserved	RW	-	-	1
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

Table 4: Skew Specification on Output Mode

Bit3	Bit2	Bit1	Bit0	Skew in ps
0	0	X	X	500
0	1	X	X	750
1	0	X	X	1000
1	1	X	X	1250

I²C Table: Group Skew Control Register

Byte 19	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	AGPSkw3	AGP Skew Control	RW	See 2-bit Skew Control at table 4		0
Bit 2	-	AGPSkw2		RW			0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Group Skew Control Register

Byte 20	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCISkw3	PCI_F [1:0] Skew Control	RW	See 2-bit Skew Control at table 4		0
Bit 6	-	PCISkw2		RW			0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	PCISkw1	PCI [5:0] Skew Control	RW	See 2-bit Skew Control at table 4		0
Bit 2	-	PCISkw0		RW			0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Slew Rate Control Register

Byte 21	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	24_48Slw1	24_48 Slew Rate Control	RW	-	-	0
Bit 6	-	24_48Slw0		RW	-	-	0
Bit 5	-	AGPSlw1	AGP Slew Rate Control	RW	-	-	0
Bit 4	-	AGPSlw0		RW	-	-	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	REFSlw1	REF Slew Rate Control	RW	-	-	0
Bit 0	-	REFSlw0		RW	-	-	0

I²C Table: Slew Rate Control Register

Byte 22	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SDSlw1	SDRAM Slew Rate Control	RW	-	-	0
Bit 6	-	SDSlw0		RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	PCISlw1	PCI_F Slew Rate Control	RW	-	-	0
Bit 2	-	PCISlw0		RW	-	-	0
Bit 1	-	PCISlw1	PCI Slew Rate Control	RW	-	-	0
Bit 0	-	PCISlw0		RW	-	-	0

I²C Table: Output Control Register

Byte 23	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	-	-	-	X
Bit 6	27	48MHz_1	Output Control	RW	Disable	Enable	1
Bit 5	47	SDRAM	Output Control	RW	Disable	Enable	1
Bit 4	28	48MHz_0	Output Control	RW	Disable	Enable	1
Bit 3	26	24_48MHz	Output Control	RW	Disable	Enable	1
Bit 2	4	REF2	Output Control	RW	Disable	Enable	1
Bit 1	3	REF1	Output Control	RW	Disable	Enable	1
Bit 0	2	REF0	Output Control	RW	Disable	Enable	1

I²C Table: Reserved Control Register

Byte 24	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Reserved Control Register

Byte 25	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

Absolute Maximum Ratings

Core Supply Voltage . . . . . 4.6 V
I/O Supply Voltage 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C
Case Temperature . . . . . 115°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} +0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			
Operating Supply Current	$I_{DD3.3OP}$	C_L = Full load; Select @ 100 MHz	229	230	360	mA
	$I_{DD3.3OP}$	C_L =Full load; Select @ 133 MHz	220	233	360	mA
Powerdown Current	$I_{DD3.3PD}$	IREF=5 mA		38.1	45	mA
Input Frequency	F_i	V_{DD} = 3.3 V		14.32		MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Clk Stabilization[1,2]	T_{STAB}	From PowerUp or deassertion of PowerDown to 1st clock.		1	1.8	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		10	ns
	t_{PHZ},t_{PLZ}	Output disable delay (all outputs)	1		10	ns

[1]Guaranteed by design, not 100% tested in production.

[2]See timing diagrams for buffered and un-buffered timing requirements.

Electrical Characteristics - CPU (0.7V Select)

T_A = 0 - 70C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.4	
Voltage High	VHigh	Statistical measurement on single ended signal using	660	710	850	mV
Voltage Low	VLow		-150	0	150	
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV
Min Voltage	Vuds		-450			
Crossing Voltage (abs)	Vcross(abs)		250		550	mV
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175	240	700	ps
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175	242	700	ps
Rise Time Variation	d-t_r				125	ps
Fall Time Variation	d-t_f				125	ps
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45	51	55	%
Skew	t_{sk3}	V_T = 50%		50	100	ps
Jitter, Cycle to cycle	$t_{jcyc-cyc}$[1]	V_T = 50%		76	150	ps

[1]Guaranteed by design, not 100% tested in production.

[2] I_{OWT} can be varied and is selectable thru the MULTSEL pin.

Electrical Characteristics - AGP

T_A = 0 - 70C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			66.66		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}$*(0.5)	12	33	55	W
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.38	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.45	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	54.4	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		243	250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V 3V66		139	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - VCH, 48MHz DOT, 48MHz, USB

T_A = 0 - 70C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			48		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20	48	60	W
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-29		-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	29		27	mA
48DOT Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	0.6	1	ns
48DOT Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	0.8	1	ns
VCH 48 USB Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.2	2	ns
VCH 48 USB Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.3	2	ns
48 DOT Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	52.8	55	%
VCH 48 USB Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	53.5	55	%
48 DOT Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		183	350	ps
USB to DOT Skew	t_{sk1}[1]	V_T = 1.5 V (0 OR 180 degrees)		0.43	1	ns
VCH Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		223	350	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} =V_{DDL} 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2A}[1]	$V_O = V_{DD}*(0.5)$	10		20	Ω
Output Impedance	R_{DSN2A}[1]	$V_O = V_{DD}*(0.5)$	10		20	Ω
Output High Voltage	V_{OH2A}	I_{OH} = -28 mA	2.4			V
Output Low Voltage	V_{OL2A}	I_{OL} = 19 mA			0.4	V
Output High Current	I_{OH2A}	V_{OH} = 2.0 V			-42	mA
Output Low Current	I_{OL2A}	V_{OL} = 0.8 V	33			mA
Rise Time	t_{r2A}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2.0	ns
Fall Time	t_{f2A}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t2A}[1]	V_T = 1.5 V	45		55	%
Jitter[1]	$t_{cyc-cyc}$	V_T = 1.5 V			250.0	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20	48	60	W
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-29		-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	29		27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.25	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.15	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	53	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			1000	ps

[1]Guaranteed by design, not 100% tested in production.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

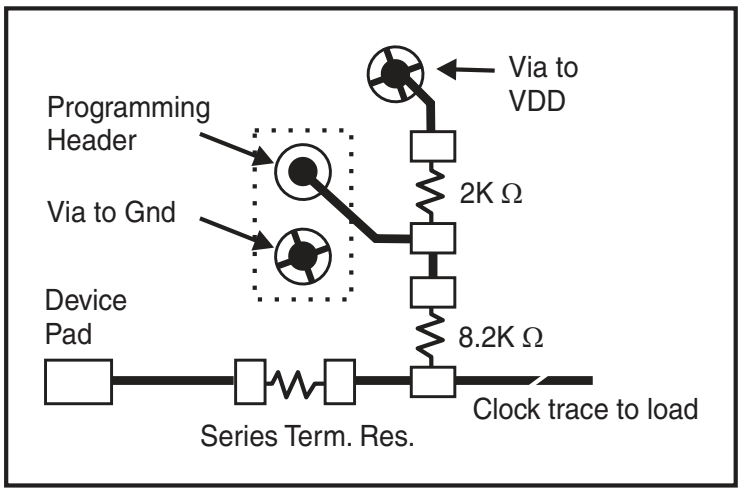
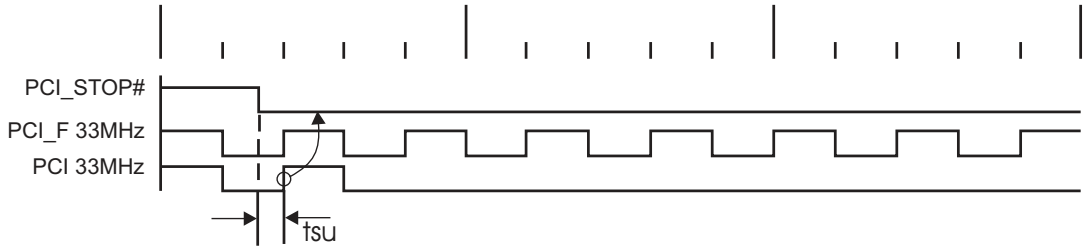


Fig. 1

PCI_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the PCI_STOP# signal will be the following. All PCI and stoppable PCI_F clocks will latch low in their next high to low transition. The PCI_STOP# setup time tsu is 10 ns, for transitions to be recognized by the next rising edge.

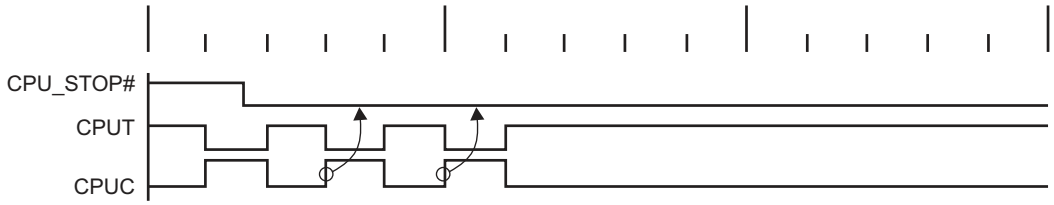
Assertion of PCI_STOP# Waveforms

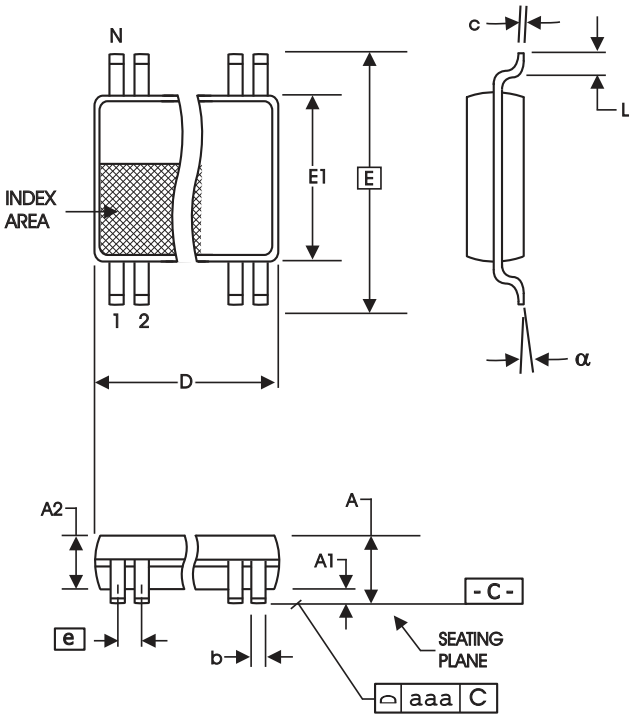


CPU_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the CPU_STOP# pin is all CPU outputs that are set in the I^2C configuration to be stoppable via assertion of CPU_STOP# are to be stopped after their next transition following the two CPU clock edge sampling as shown. The final state of the stopped CPU signals is CPUT=High and CPUC=Low. There is to be no change to the output drive current values. The CPUT will be driven high with a current value equal to (MULTSEL0) X (I REF), the CPUC signal will not be driven.

Assertion of CPU_STOP# Waveforms





6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

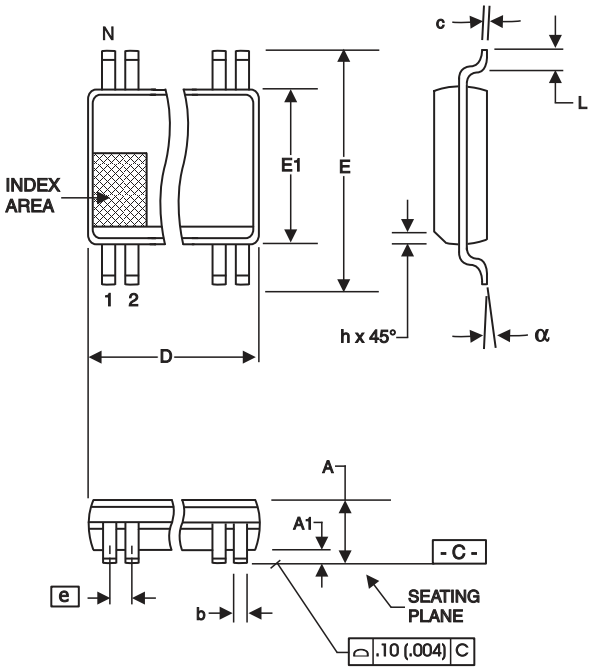
ICS951402yGLF-T

Example:

ICS XXXX y G LF- T

- **Designation for tape and reel packaging**
- **Annealed Lead Free (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0660—05/05/05



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS951402yFLF-T

Example:

ICS XXXX y F LF- T

- **Designation for tape and reel packaging**
- **Annealed Lead Free (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0660—05/05/05

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